Multicore DSPs for High-Performance Video Coding

Delivering high density, low power and cost efficiency

Video processing demands are on the rise from a wide variety of applications:

- The latest tablets and TVs support 4K resolution (surpassing 1080p resolution)
- Broadcast television cameras are capturing higher-fidelity images (up to 12b per pixel)
- The new video encoding standard, HEVC (or H.265), offers unsurpassed compression but requires significantly more processing than the current H.264 standard

The rapid move to these new standards and higher formats require programmable implementations as time to market is critical and the delay to build dedicated hardware could mean missing critical market windows. In addition, changes are still coming on all these fronts so programmable systems add the crucial ability to provide field upgrades as the industry moves to these new formats.

Texas Instruments' multicore processors offer the high-performance processing capabilities that these applications require, with full programmability in a cost- and power-optimized package. In production now is TI's TMS320C6678 DSP, based on the KeyStone architecture, which is available on standard form factor PCIe cards for video processing offload in existing servers (see Figure 1). Also sampling is TI's 66AK2H12 System-on-Chip (SoC), based on the latest KeyStone II architecture (see Figure 2 on the following page). The 66AK2H12 adds a quad ARM® Cortex™-A15 MPCore™ processor cluster to eight TMS320C66x TI DSPs and allows for new, optimized server architectures to be designed for this market.

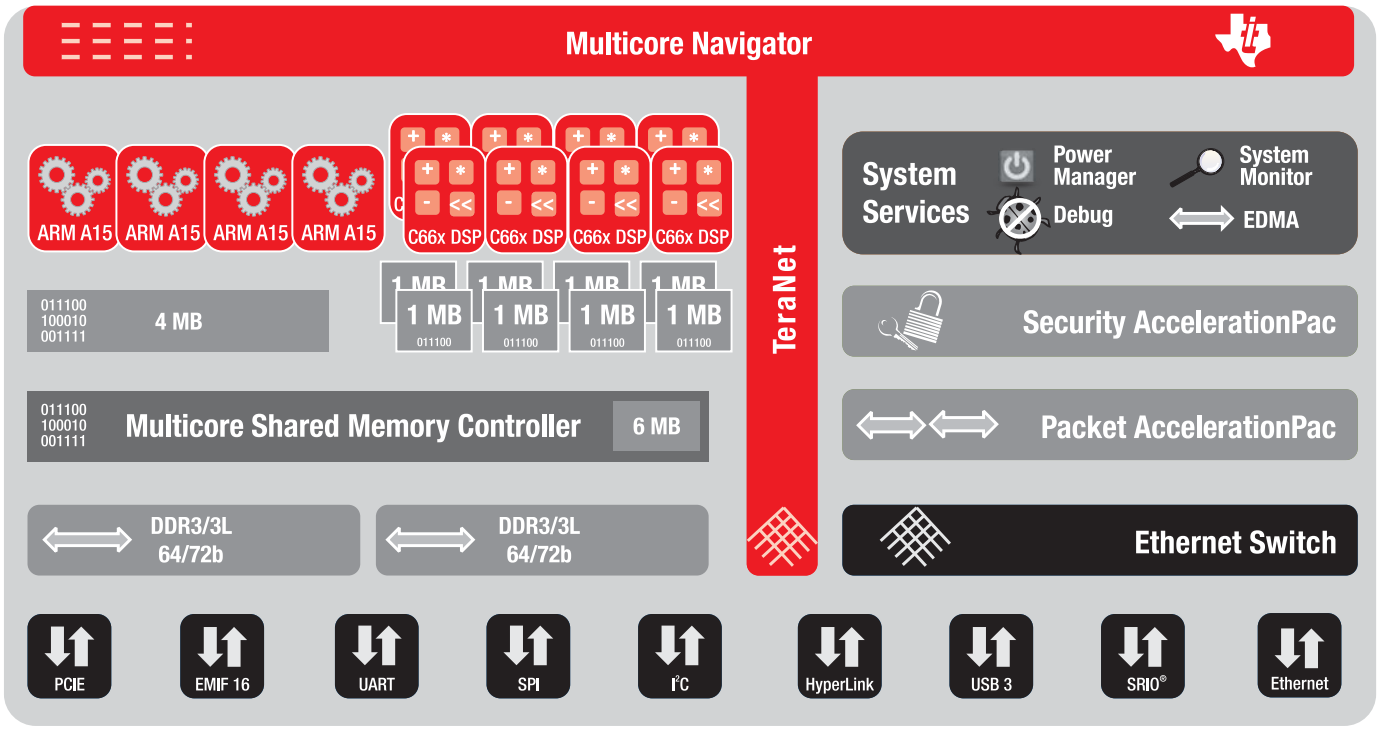
▲ *Figure 1. Advantech DSPC-8681 full-length PCIe card with eight C6678 DSPs*

Key Features

- C6678 – Highest DSP performance – fastest multicore fixed- and floating-point DSP
  - Under 10W
  - 8 C66x DSP cores, 1.25GHz, 160 GFLOPS, 320 GMACS
  - Available on PCIe cards (quad and octal solutions)
- 66AK2H12 – First truly infrastructure-class device with quad Cortex-A15 processors
  - Under 16W
  - Four Cortex-A15 RISC cores, 1.4GHz, with NEON SIMD and VFPv4 floating-point units
  - Eight C66x DSP cores, 1.2GHz, 160 GFLOPS, 320 GMACS
  - Hardware virtualization and ARM Trustzone
- KeyStone II architecture
  - Multicore Navigator – brings single-core programming simplicity to multicore SoCs with 16,000 atomic hardware queues
  - TeraNet – On-chip crossbar switch fabric, multi-terabit/s data throughput
  - Multicore Shared Memory Controller for fast DDR access
  - 64-bit DDR3 (2 for 66AK2H SoC) with ECC support
- High-speed interfaces
  - 10GigE Switch (66AK2H SoC)
  - GigE Switch with on-board packet accelerator and network co-processor
  - PCIe Gen 2, 2 lanes
  - RapidIO® Gen 2, 4 lanes
  - HyperLink 50 Gbps SerDes (2× on 66AK2H12 SoC)
- Low power
  - C6678 DSP nominal 10W
  - 66AK2H12 SoC nominal 15W
  - Dynamic power monitoring
  - SmartReflex™ technology

Making video infrastructure development simple, flexible and slashing time to market

There are a number of challenges facing the video infrastructure market ranging from simply supporting the vast amount of video traffic to supporting the latest and greatest video encoding/decoding standards. The biggest challenge currently is the need to support the



▲ *Figure 2. TI's KeyStone 66AK2H12 SoC*

new High Efficiency Video Coding (HEVC or H.265) standard. The standard is still currently under definition but is expected to be ratified very soon. HEVC improves data compression by up to 50% over the current state-of-the-art and with the increasing amount of high-definition (HD) video traffic, this is a huge benefit. In addition to providing flexibility in the network, there is also the issue of encoding data at the camera. When video is being captured at a live event, it also needs to be compressed and sent back to the studio for editing prior to broadcasting and often times the requirements are higher for this than for normal transmission as the broadcasters would like to keep the quality as high as possible prior to editing. A key benefit of TI's multicore product line is the ability to support large-scale deployments as found in data centers as well as the ability to support high-end camera systems in the field. This allows a wide range of products to be developed quickly, leveraging the KeyStone architecture to scale from smaller to larger-scale systems.

TI provides a Multicore Video Software Development Kit (MCSDK-Video) to get developers going quickly with optimized coding implementations (see Figure 3). Using the MCSDK-Video and either standalone evaluation modules, or off-the-shelf PCIe cards, such as Advantech's lightning DSP cards, differentiated systems can be quickly created that are both flexible and cost/power conscious. Figure 4, on the following page, shows the performance capabilities of the DSPC-8682 PCIe card as well as the DSPA-8901.

Codec Support	
Video codecs	JPEG 2000, AVC-Intra 50/100, H.265, H.264 10-bit 4:2:2, H.263, MPEG-4, MPEG-2 4:2:2, JPEG, VC1, SVC, Sorenson Spark encoders and decoders
Audio codecs	AAC, AACv2, AC3, MP3, WMA8, WMA9 encoders and decoders
Voice codecs	G.711, G.718, G.722, G.722.1, G.723, G.726, G.728, G.729AB, G.729G, GSM-ARM w/ EFR, GSM-FR, EVRC-B, WBAMR

▲ *Figure 3. Optimized codec support*

Get Started Quickly with TI Software Tools and Optimized Codecs

- Multicore Software Development Kit (MCSDK) with Video Infrastructure Demos
  - MCSDK
    - Robust software development environment for rapid development
    - Provides I/O drivers for all high-speed interfaces
    - Includes the network development kit for GigE support
    - Available on both Linux™ and Windows®
    - Extensive online training
  - Video Demos
    - Optimized video codecs including MPEG-4, H.264, JPEG 2000 and more
    - Framework to launch codecs on stand-alone evaluation modules and on Advantech PCIe cards
    - Supports encode, decode and transcode modes
    - Includes examples of graphics and text overlay, frame-rate conversion and spatial resizing
    - Runs in single-core, multicore, and multi-device modes

66AK2H12 SoC offers new architecture possibilities

The integration of the quad Cortex-A15 cluster in TI's 66AK2H12 SoC allows efficient systems to be built without the need for a separate host processor. With full support of Linux (both commercial and open) the 66AK2H12 SoC allows existing code to be ported simply and easily to the new SoC. The processing power of the DSPs can then be easily accessed using standard multicore programming protocols such as OpenMP and OpenCL, both of which are supported on TI processors. In addition, the quad Cortex-A15 clusters can run full networking and protocol stacks taking advantage of the on-board network coprocessors. With the large number of high-speed interfaces the 66AK2H12 SoC not only supports traditional server architectures and Advanced TCA designs, but new architectures optimized for video processing could also be easily developed.

For more information about TI's KeyStone-based DSPs and SoCs, please visit **www.ti.com/multicore**.

Multimedia Application	System Solution Density (# of channels)	
	PCIe card 8 C6678 DSPs	ATCA card 20 C6678 DSPs
Mobile Voice Applications AMR encode + decode, 12.2Kbps	11,000	27,500
Mobile Video Applications H.264 BP encode + decode, CIF, 30 fps	240	600
Content Delivery Network H.264 BP encode + decode, SD, 30 fps	120	300
HD Conferencing MCU, MRFP H.264 BP encode + decode, 1080p30	12	30
HD Broadcast AVC-Intra 100, 10-bit, 4:2:2, 60 fps	5	12

▲ *Figure 4. Performance capabilities of the TI-based PCIe and ATCA cards*

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