Tutorial: PREESM - Dataflow Programming of Multicore DSPs

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http://preesm.sourceforge.net/website

- Eclipse-based Tool
- Written in Java and Xtend
- Using
  - Eclipse Modeling Framework,
  - Eclipse Graphiti,
  - Eclipse CDT
- Compatible and tested on Linux and Windows
- Release 2.0.0 on sept 2014
• Started in 2007
• In collaboration with Texas Instruments France
• 16 contributors
• Academic collaborations
  – LAAS
  – University of Maryland
  – ENIS
  – Abo Akademi
• Preesm offers Editors
  – Algorithm
  – Architecture
  – Scenario

• And can run a Workflow
  – Transformations of models
PREESEM Workflow
PREESM Workflow
PREESM Workflow
PREESM Workflow
• A workflow runs typically within a few tens of seconds
• Algorithm: typically 10-1500 actors
• Architecture: typically 1-20 cores
Examples for the tutorial

**Algorithms**

Sobel filter: edge detection
Stereo matching: disparity map

**Architectures**

Intel i7 quad-core
TI Shannon (C6678)
Rapid prototyping process

1. Architecture modeling
2. Algorithm modeling
3. Scenario selection
4. Workflow composition
5. Workflow execution
Algorithm modeling

PiSDF

Parameterized
Dynamism

Interfaced
Hierarchy & Composition

Synchronous Data-Flow

Actors & Fifos
Algorithm examples

Sobel filter
Stereo matching
S-LAM
System-Level Architecture Model

Processing elements
Communication nodes
Intel i7 quad-core
TI Shannon (C6678)
Scenario selection

Link between *algorithm* & *architecture*

- Execution times
- Execution constraints
- Simulation information

Enables separation of concerns
Sobel filter on Intel i7 quad-core

Read

1

190000 cycles

Size

= 101376

core1

Size

= 101376
Rapid prototyping tasks

Scheduling
Code generation
Memory optimization
Visualization tools

…
2 workflows

Scheduling

Scheduling + code generation

Algorithm

Hierarchy flattening

Single-rate transformation

Mapping & scheduling

Architecture
Let’s complicate things

Small application on CPU

What about more realistic cases?

Execution on DSP (C6678)
Stereo matching algorithm
Rapid prototyping for multicore DSPs

High-level modeling of **parallelism**

**Automatic** mapping

**Automatic** scheduling

**Automatic** code generation

**Advanced** memory optimization

**Bridges** to UML MARTE, SDF3 & Orcc
Research tool

New models & features
Regular enhancements

Incoming features

Parameter-dependent timings
Distributed memory management
Bridge to DIF from Univ. of Maryland
GUI enhancements (workflow scripts)
...

PREESM is constantly improving
Thank you for your attention

Hierarchical Algorithm Model → Scenario → Multi-Core Scheduling → Deployment

Multi-core Heterogeneous Model

Simulation

Static Code Generation

preesm.sourceforge.net/website/  Twitter: @PreesmProject
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