Application Report
SCAA056 –December 2001

Interfacing Between LVPECL, LVDS, and CML

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ABSTRACT

This application note describes various methods of interfacing between different logic levels. It focuses on interconnection between LVPECL (low voltage positive-referenced emitter coupled logic), CML (current mode logic), and LVDS (low voltage differential signals). Although there are various methods to interconnect between these signal levels, this report mainly focuses on three interfaces: LVPECL to LVPECL, LVPECL to CML, and LVDS to LVDS. Both dc- and ac-coupling are discussed where applicable.

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1 Introduction

As the speed of data transmission approaches the gigabit range, the supply voltage continues to shrink. Many applications are moving toward 3-V, 2.5-V, 1.8-V, and even to 1.2-V power supplies. There are many issues to consider when running at high-speed applications. These issues include EMI (electromagnetic interference), signal reflection, power consumption, capacitive and inductive crosstalk, signal swing, and transient switching noise. Depending on the application, there are advantages of using one signal level over the other.

2 LVPECL to LVPECL

2.1 DC-Coupling From LVPECL to LVPECL

LVPECL stems from ECL (emitter coupled logic) but uses a positive rather than a negative supply voltage. It also uses 3.3 V rather than the 5 V that has been dominant for some time.

For example PECL, is used in high-speed backplanes and point-to-point serial and parallel data communication. The proper termination for PECL outputs is 50 Ω to (V_{CC} - 2 V). Since in real applications a (V_{CC} – 2 V) supply is not readily available, the 50-Ω termination resistor is normally replaced by a Thevenin equivalent network composed of two resistors (R1 and R2) as shown in Figure 1. This Thevenin termination is referred to as dc-coupling. The values of R1 and R2 are chosen such that:

Their parallel combination is equal to Zo = 50 Ω, that is: $\frac{R1 \times R2}{R1 + R2} = Zo = 50\,\Omega$ (1)

Looking at point B in Figure 1, the ratio of R2 to the sum of R1 and R2 should equal the ratio of (V_{CC} - 2) to V_{CC}, that is: $\frac{R2}{R1 + R2} = \frac{(Vcc - 2V)}{Vcc} \rightarrow\rightarrow\rightarrow$ (2)

Results: For 3.3-V supply, the values are: R1 ≅ 127 Ω and R2 = 82.5 Ω

Detail derivation:

Solving these equations results in the exact values of R1 and R2.

Solving equation 1 for (R1+R2) by cross-multiplying yields: $(R1 + R2) = \frac{R1 \times R2}{50\ \Omega}$

Then solving the equation 2 for (R1+R2) yields: $(R1 + R2) = \frac{Vcc \times R2}{(Vcc - 2)}$

Setting these two quantities equal gives: $\frac{R1 \times R2}{50} = \frac{Vcc \times R2}{(Vcc - 2)}$

Solving for R1 from the last equalities by cross-multiplying yields: $\frac{R1 \times R2}{1} = \frac{50 \times Vcc \times R2}{(Vcc - 2)}$, and 50 x V_{CC} x R2 = R1 x R2(V_{CC} – 2). Dividing both equations by R2 gives: 50 x V_{CC} = R1(V_{CC} – 2), and R1 becomes: $R1 = \frac{50 \times Vcc}{(Vcc - 2)}$. Now, solving equation 2 for R2 and substituting the above value for R1 yields (from equation 2) $\frac{R2}{R1 + R2} = \frac{(Vcc - 2)}{Vcc}$. Cross-multiplying yields

R2 x V_{CC} = R1 x V_{CC} – 2R1 + R2 x V_{CC} – 2R2 ⇒

$R2 \times V_{CC} - R2 \times V_{CC} + 2R2 = R1 \times V_{CC} - 2R1$. Rearranging produces

$\Rightarrow R2(V_{CC} - V_{CC} + 2) = R1(V_{CC} - 2) \Rightarrow R2 = R1\frac{(Vcc - 2)}{2}$. Substituting the value of R1 in this equation produces: $\Rightarrow R2 = \frac{50 \times Vcc}{(Vcc - 2)} \text{ x } \frac{(Vcc - 2)}{2} \Rightarrow R2 = 25\ V_{CC}$

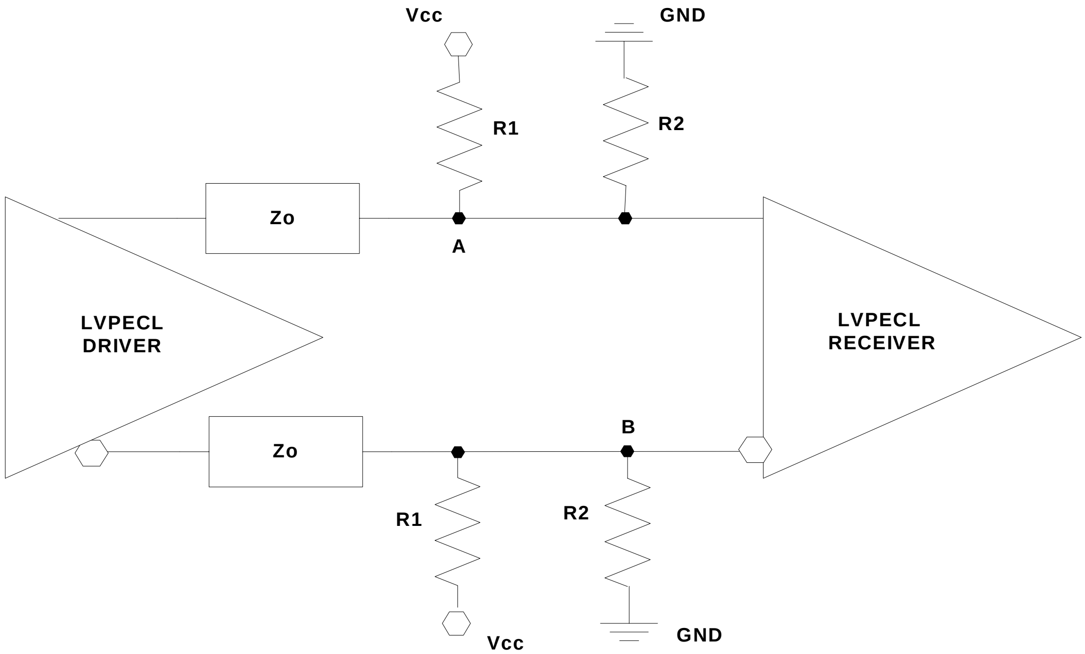

Figure 1. DC-Coupling Between LVPECL and LVPECL

2.2 AC-Coupling of LVPECL Outputs to a 50-Ω Termination

AC-coupling of PECL outputs could be achieved as shown in Figure 2. There are some points worth mentioning:

- The PECL outputs should be dc-biased prior to the ac-coupling through a resistor, R-bias, as shown in Figure 2.
- The dc bias voltage of the PECL inputs should be set to (V_{CC} - 1.3 V) through the proper selection of R2 and R3.
- The parallel combination of R2 and R3 should match the characteristic impedance, Zo of the transmission line.
- Using a resistor, Rx across the differential output pair, should optimize power consumption.

Results: R3 ≅ 3.3 kΩ, R2 ≅ 2.2 kΩ, and R-bias ≅ 140 Ω to 240 Ω

Detail derivation:

The following calculations are based on TI's CDC111 and CDCVF111 specifications.

Now we need to calculate the resistor values in Figure 2.

Let us begin by finding $R_{bias} = \frac{Vcc - 1.3}{I_{DC}}$, if we assume a dc source current of 14.2 mA (worst case), and 8.2 mA (best case) then respectively.

Next step is to find R2 and R3 by assuming Rx ≅ 104 Ω. From Figure 2 we need to match Zo with the parallel combination of R2, R3 and $\frac{Rx}{2}$.

R2 || R3 || $\frac{Rx}{2}$ ≅ Zo ≅ 50 Ω, and $\frac{R3}{R2+R3} = \frac{(Vcc-1.3)}{Vcc}$. For a 3.3-V supply we have $\frac{R3}{R2+R3} = \frac{2}{3.3}$, cross-multiplying and collecting terms yields, R2 = 0.65 R3

Now we use the first equation to solve R3:

$\frac{1}{R2} + \frac{1}{R3} + \frac{1}{52} = \frac{1}{50}$. Rearranging yields $\frac{R2 + R3}{R2 \text{ x } R3} = \frac{1}{1300}$. Now cross-multiplying and substituting R2 = 0.65 R3 in the last equation we can solve for R3 and R2.

$1300R2 + 1300R3 = R2R3 \Rightarrow \frac{1300(1.65R3)}{0.65R3} = \frac{(0.65R3)R3}{0.65R3} \Rightarrow$ R3 ≅ 3.3 kΩ, and R2 ≅ 2.2 kΩ.

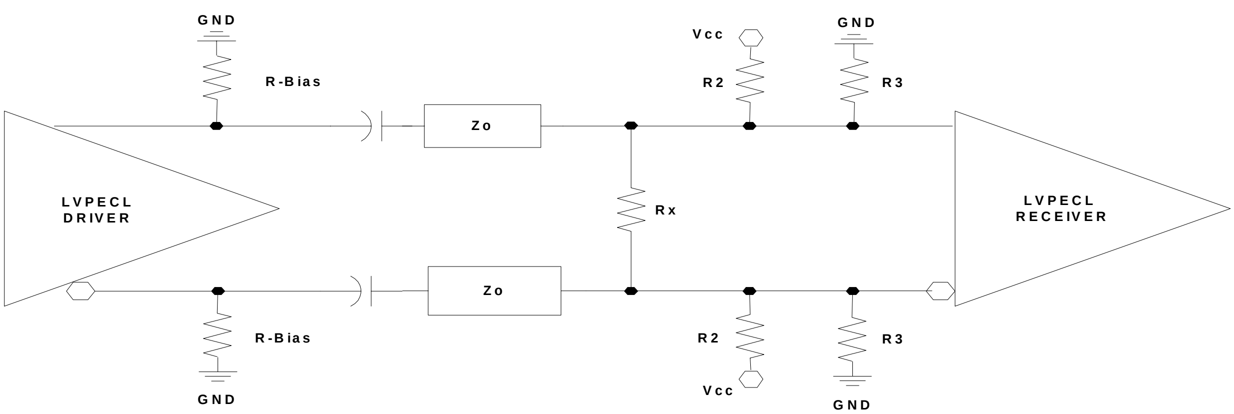

Figure 2. AC-Coupling Between LVPECL and LVPECL

3 LVPECL to CML

CML Is similar to ECL and the only difference is the voltage swing (800 mV for ECL versus 400 mV for CML) and the bias termination (in ECL case).

Interfacing from LVPECL to CML can be accomplished through ac- or dc-coupling.

3.1 DC-Coupling Between LVPECL and CML

In order to interface between LVPECL and CML, a level shifting resistive network as shown in Figure 3 is needed to adjust both the LVPECL outputs and the CML input.

Next we need to find the values for R1, R2, and R3 that are needed to level shift the LVPECL output to meet the CML input. To simplify the calculation let us use Figure 3.

Looking from point A we see: $\frac{R2}{R2 + R1//(R3+50)} = \frac{(Vcc-2)}{Vcc} \rightarrow\rightarrow\rightarrow$ Equation 1

R1 || R2 || (R3+50) $\cong$ 50 $\rightarrow\rightarrow\rightarrow$ Equation 2

Looking at point B, we can use the node voltage method and equate the two currents as:
$\frac{Vcc-VB}{50} = \frac{VB-(Vcc-1.3)}{R3} \rightarrow\rightarrow\rightarrow$ Equation 3

Results: R1 = 208 Ω, R2 = 82.5 Ω, and R3 = 275 Ω

Detail derivation:

Substituting the value for VB =(Vcc - 0.2 V) in this equation we have:

$$\frac{Vcc-Vcc+0.2}{50} = \frac{Vcc-0.2-Vcc+1.3}{R3} \Rightarrow \frac{0.2}{50} = \frac{1.1}{R3} \Rightarrow \text{R3} = \frac{50 \text{ x } 1.1}{0.2} = 275\ \Omega$$

Substituting R3 = 275 Ω in equation 2 we have, R1 || R2 || (275 + 50) $\cong$ 50

$$\Rightarrow \frac{1}{R1} + \frac{1}{R2} + \frac{1}{325} = \frac{1}{50} \Rightarrow \frac{1}{R1} + \frac{1}{R2} = \frac{1}{50} - \frac{1}{325} \Rightarrow \frac{\text{R1} + \text{R2}}{\text{R1 x R2}} = \frac{11}{650} \Rightarrow R1R2 = \frac{650}{11}(R1+R2) \rightarrow \text{(I)}$$

Now we need to solve equation 1 for the same quantity (R1+R2) and set them equal. Assuming a 3.3-V supply and substituting R3 = 275 in equation 1 we have:
$\frac{(\text{Vcc} - 2)}{1} = \frac{\text{Vcc x R2}}{\text{R2 + R1//(325)}} \Rightarrow \frac{1.3}{1} = \frac{\text{3.3 x R2}}{\text{R2 + (325 x R1)/(R1 + 325)}}$; multiplying the right side by (R1+325) $\Rightarrow \frac{1.3}{1} = \frac{\text{3.3R2 x (R1 + 325)}}{\text{R2R1 + 325R2 + 325R1}}$. Cross-multiplying gives 3.3R2R1 + 3.3(325)R2 = 1.3R1R2 + (1.3)(325)R1, collecting terms and solving for the quantity R1R2 yields $\Rightarrow R1R2 = \frac{422.5R1 - 650R2}{2}$. Setting this equation equal to (I) above, yields
$\Rightarrow \frac{650R1}{11} + \frac{650R2}{11} = \frac{422.5R1}{2} - \frac{650R2}{2} \Rightarrow 384.091R2 = 152.16R1 \Rightarrow$ R1 = 2.524 x R2.

Substituting this value in either equation 1 or 2, we can solve for R1 and R2. We choose to use $R1R2 = \frac{650}{11}(R1+R2) \rightarrow \text{(I)} \Rightarrow \text{2.52R2 x R2} = \frac{650}{11}(3.52)\text{R2}$, dividing both sides by (2.52 R2) yields R2 = 82.5 Ω, and R1 = 2.524 x R2 = 208 Ω.

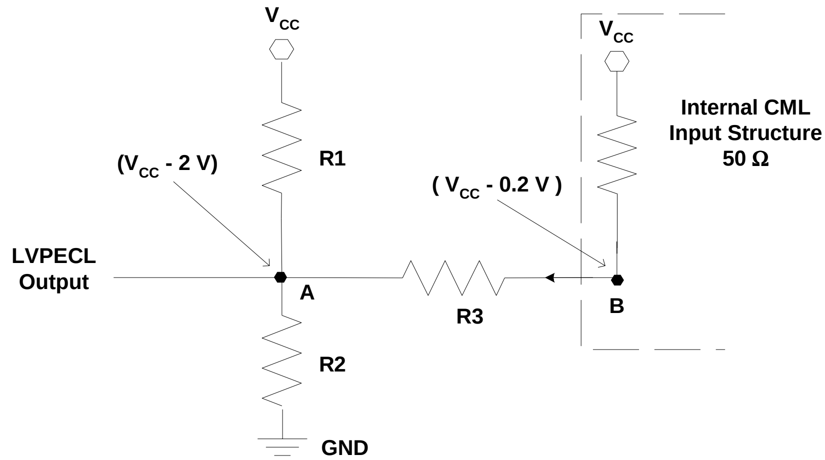

Figure 3. Single-Ended Representation of Figure 4

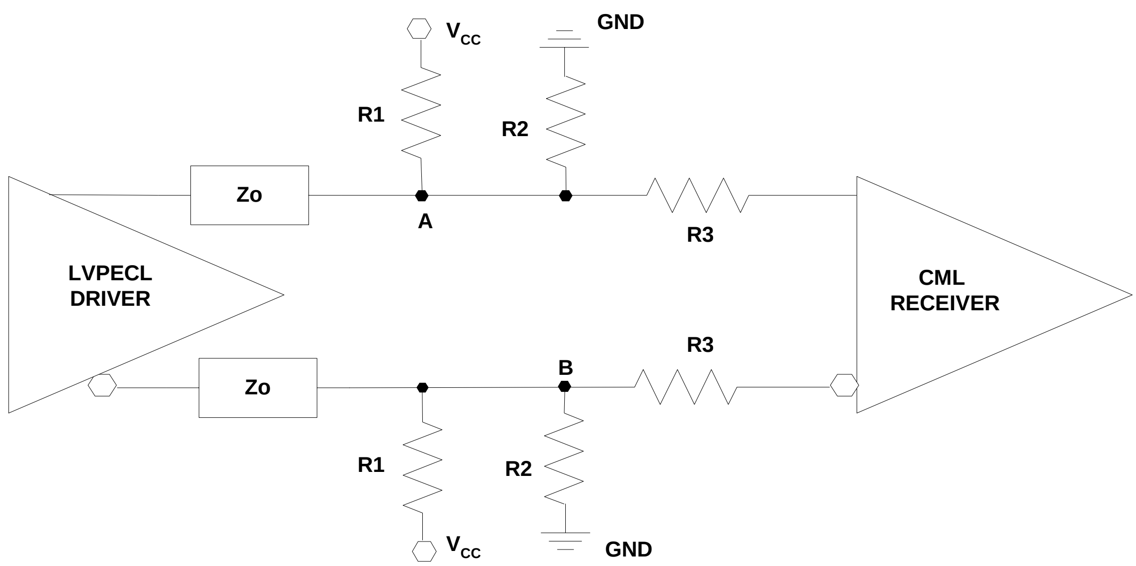

Figure 4. DC-Coupling Between LVPECL and CML

3.2 AC-Coupling Between LVPECL and CML

Figure 5 below is one example of an ac-coupling between a LVPECL driver and a CML receiver. As indicated in this Figure, there are two resistors, R-bias and Ra. The first resistor is required to dc-bias the LVPECL outputs prior to ac-coupling. The value of R-bias ranges from 140 Ω to 240 Ω as found previously in section 2.2. On the other hand, Ra is optional and may or may not be required. In the case where the differential LVPECL output is larger than what the CML receiver can tolerate, then Ra can be used to attenuate the LVPECL output such that it meets the input voltage required for the CML receiver.

For example, if the LVPECL output has 645-mV swing and the CML receiver can only accept 400 mV, then we need an attenuation factor of 0.62. Attenuation = $\frac{50}{Ra + 50}$.

Then, Ra ≅ 30 Ω is required to attenuate the LVPECL output from 650 mV to 400 mV in order to meet the 400-mV CML receiver input.

As another example, if the LVPECL output swing is 750 mV and the required CML receiver input is 400 mV, we would need an attenuation factor of 0.68, which requires Ra ≅ 23 Ω.

As a final note regarding all the ac-coupling schemes discussed thus far, the value of the coupling capacitors that are required is in the range of 400 pF to 3 nF (depending on operating frequency). The derivation of the exact value of these ac-coupling capacitors is not discussed in this report.

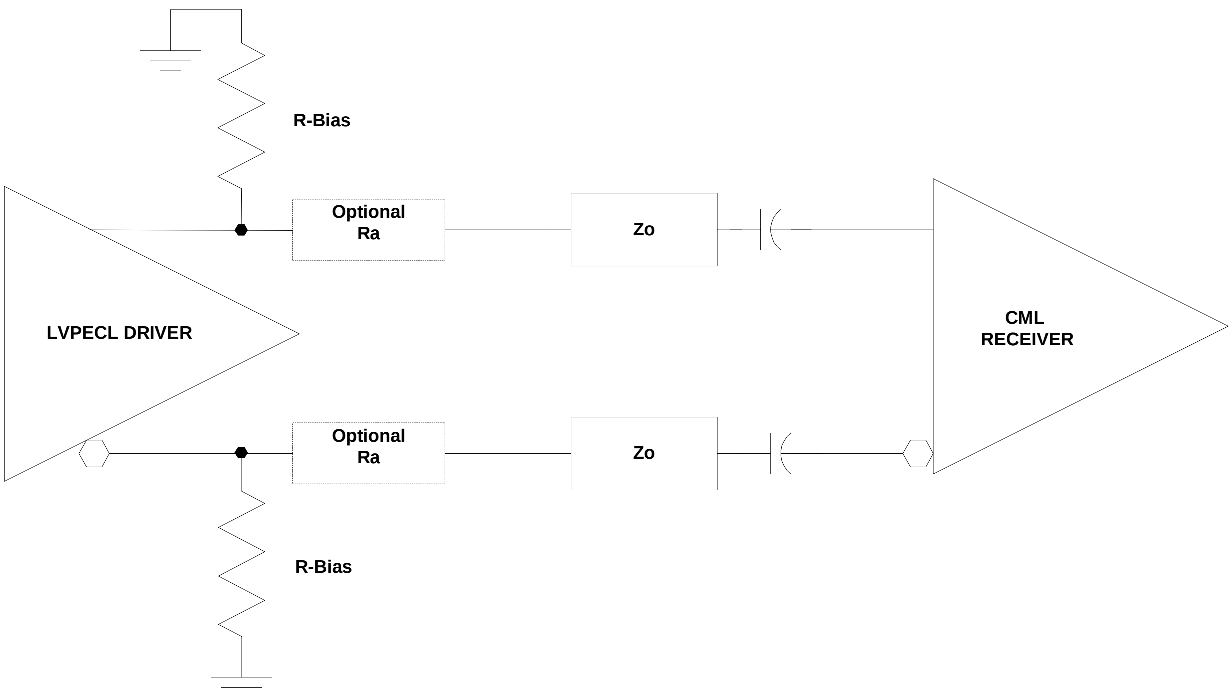

Figure 5. AC-Coupling Between LVPECL and CML

4 LVDS to LVDS

LVDS is suitable for point-to-point where power consumption is of most concern (due to small signal swing.

Some examples where LVDS is being used are wireless base stations, ATM switches, printers, copy machines, and flat-panel displays in automotive applications and notebook PCs.

The interface between LVDS to LVDS is a 100-Ω resistor across the differential output pair (such as TI's SN65LVDS33, SN65LVDS32) as shown in Figure 6. Some LVDS receivers (such as TI's SN65LVDT33) have a 100-Ω on-chip termination; in this case there is no need for any additional components and the interface is just a direct connection between the LVDS driver and the LVDS receiver.

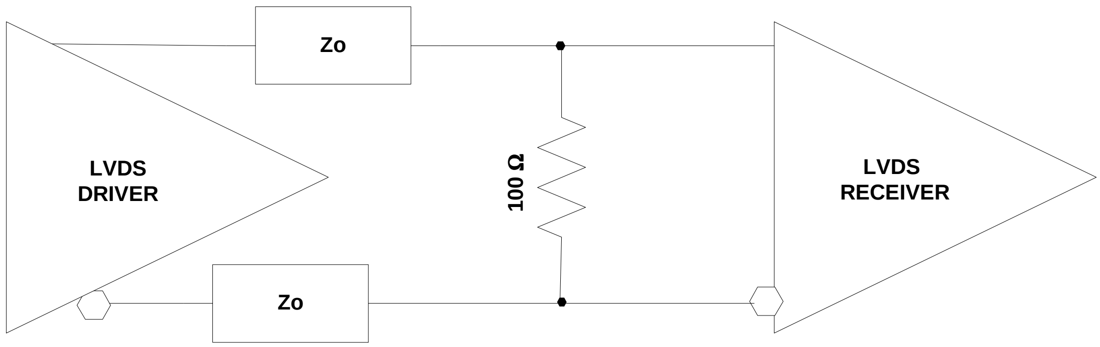

Figure 6. Interface Between LVDS and LVDS Without On-Chip Termination

5 References

1. *Interfacing Differential Logic With LVDS Receivers* application report, Texas Instruments literature number SLLA101
2. *Clock Distribution Circuits (CDC)* CDC data book, Texas Instruments literature number SCAD004
3. *Output Jitter of CDC111/CDCVF111 in Networking* application report, Texas Instruments, literature number SCAA051
4. *Comparing Bus Solutions* application report, Texas Instruments literature number SLLA067

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