TEXAS INSTRUMENTS

TPS763-Q1, TPS76301-Q1, TPS76316-Q1, TPS76318-Q1
TPS76325-Q1, TPS76330-Q1, TPS76333-Q1, TPS76350-Q1

SGLS247B – SEPTEMBER 2011 – REVISED MARCH 2016

TPS763xx-Q1 Low-Power, 150-mA, Low-Dropout Linear Regulators

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 1C
  - Device CDM ESD Classification Level C3
- 150-mA Low-Dropout Regulator
- Output Voltage: 5 V,3.3 V, 3 V, 2.5 V, 1.8 V, 1.6 V, and Variable
- Dropout Voltage, Typically 300 mV at 150 mA
- Thermal Protection
- Overcurrent Limitation
- Less Than 2-µA Quiescent Current in Shutdown Mode
- –40°C to 125°C Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package

2 Applications

- RF: VCOs, Receivers, ADCs
- Cellular phones
- Bluetooth®
- Battery-Powered Systems

3 Description

The TPS763xx-Q1 family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in a 5-pin, small outline integrated-circuit SOT-23 package, the TPS763xx-Q1 series devices are ideal for cost-sensitive designs and for applications where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual pnp pass transistor to be replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is low—typically 300 mV at 150 mA of load current (TPS76333-Q1)—and is directly proportional to the load current. Since the PMOS pass element is a voltage-driven device, the quiescent current is low (140 µA maximum) and is stable over the entire range of output load current (0 mA to 150 mA). Intended for use in portable systems such as laptops and cellular phones, the low-dropout voltage feature and low-power operation result in a significant increase in system battery operating life.

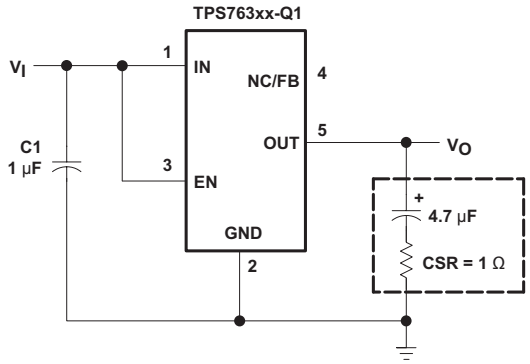
The TPS763xx-Q1 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 µA maximum at T_J = 25°C.The TPS763xx-Q1 is offered in 1.6-V,1.8-V, 2.5-V, 3-V, 3.3-V, and 5-V fixed-voltage versions and in a variable version (programmable over the range of 1.5 V to 6.5 V).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS763xx-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Note: TPS76316-Q1, TPS76318-Q1, TPS76325-Q1, TPS76301-Q1 TPS76333-Q1, TPS76350-Q1 (fixed-voltage options)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2011) to Revision B **Page**

- Removed 3.8 V, 2.8 V, and 2.7 V output voltage versions from the data sheet ... 1
- Removed the TPS76327-Q1, TPS76328-Q1, and TPS76338-Q1 parts from the data sheet ... 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Dissipation Ratings* ... 6

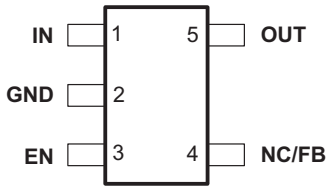
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5 Voltage Options

VOLTAGE	PART NUMBER	SYMBOL
Variable	TPS76301QDBVRQ1	BAN
1.6 V	TPS76316QDBVRQ1	BAD
1.8 V	TPS76318QDBVRQ1	BAP
2.5 V	TPS76325QDBVRQ1	BAQ
3 V	TPS76330QDBVRQ1	BAT
3.3 V	TPS76333QDBVRQ1	BAU
5 V	TPS76350QDBVRQ1	BAW

6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	—	Enable input
FB	4	I	Feedback voltage (TPS76301-Q1 only)
GND	2	—	Ground
IN	1	I	Input supply voltage
NC	4	—	No connection (fixed-voltage option only)
OUT	5	O	Regulated output voltage.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage	–0.3	10	V
Voltage at EN			V
Voltage on OUT, FB			V
Peak output current	Internally limited		
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_I	2.7		10	V
Continuous output current, I_O	0		150	mA
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS763xx-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.83	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 4.7$ µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76301-Q1	3.25 V > VI ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA, T_J = 25°C	0.98V_O	V_O	1.02V_O	V
			3.25 V > VI ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA,	0.97V_O	V_O	1.03V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA, T_J = 25°C	0.98V_O	V_O	1.02V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA,	0.97V_O	V_O	1.03V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA, T_J = 25°C	0.975V_O	V_O	1.025V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA,	0.9625V_O	V_O	1.0375V_O	
		TPS76316-Q1	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.568	1.6	1.632	V
			V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.56	1.6	1.64	
			V_I 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.536	1.6	1.664	
		TPS76318-Q1	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.764	1.8	1.836	V
			V_I = 2.7 V, 1 mA < I_O < 75 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 3.25 V, 1 mA < I_O < 100 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.755	1.8	1.845	
			V_I = 3.25 V, 1 mA < I_O < 150 mA	1.733	1.8	1.867	
		TPS76325-Q1	I_O = 1 mA to 100 mA, T_J = 25°C	2.45	2.5	2.55	V
			I_O = 1 mA to 100 mA	2.425	2.5	2.575	
			I_O = 1 mA to 150 mA,, T_J = 25°C	2.438	2.5	2.562	
			I_O = 1 mA to 150 mA	2.407	2.5	2.593	
		TPS76330-Q1	I_O = 1 mA to 100 mA, T_J = 25°C	2.94	3	3.06	V
			I_O = 1 mA to 100 mA	2.91	3	3.09	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.925	3	3.075	
			I_O = 1 mA to 150 mA	2.888	3	3.112	
		TPS76333-Q1	I_O = 1 mA to 100 mA, T_J = 25°C	3.234	3.3	3.366	V
			I_O = 1 mA to 100 mA	3.201	3.3	3.399	
			I_O = 1 mA to 150 mA, T_J = 25°C	3.218	3.3	3.382	
			I_O = 1 mA to 150 mA	3.177	3.3	3.423	
		TPS76350-Q1	I_O = 1 mA to 100 mA, T_J = 25°C	4.875	5	5.125	V
			I_O = 1 mA to 100 mA	4.825	5	5.175	
			I_O = 1 mA to 150 mA, T_J = 25°C	4.750	5	5.15	
			I_O = 1 mA to 150 mA	4.80	5	5.2	
$I_{(Q)}$	Quiescent current (GND) terminal current)		I_O = 0 mA to 150 mA, T_J = 25°C(1)		85	100	µA
			I_O = 0 mA to 150 mA, see			140	
	Standby current		EN < 0.5 V, T_J = 25°C		0.5	1	µA
			EN < 0.5 V			2	
Vn	Output noise voltage		BW = 300 Hz to 50 kHz, Co = 10 µF, T_J = 25°C(2)		140		µV
PSRR	Ripple rejection		f = 1 kHz, Co = 10 µF, T_J = 25°C(2)		60		dB
	Current limit		T_J = 25°C, see(3)	0.5	0.8	1.5	A
	Output voltage line regulation (ΔVO/VO), (see (3))		V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V, T_J = 25°C		0.04	0.07	%/V
			V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V			0.1	
V_{IH}	EN high level input		See(2)		1.4	2	V
V_{IL}	EN low level input		See(2)	0.5	1.2		
I_I	EN input current		EN = 0 V		–0.01	–0.5	µa
			EN = IN		–0.01	–0.5	

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater.
(2) Test condition includes: output voltage V_O = 0 V (for variable device FB is shorted to V_O) and pulse duration = 10 ms.
(3) If VO < 2.5 V and V_{Imax} = 10 V, V_{Imin} = 3.5 V:

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Electrical Characteristics (continued)

over operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, $C_o = 4.7$ µF (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	TPS76325-Q1	I_O = 0 mA, T_J = 25°C		0.2		mV
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		120	150	
			I_O = 50 mA			200	
			I_O = 75 mA, T_J = 25°C		180	225	
			I_O = 75 mA			300	
			I_O = 100 mA, T_J = 25°C		240	300	
			I_O = 100 mA			400	
			I_O = 150 mA, T_J = 25°C		360	450	
			I_O = 150 mA			600	
		TPS76333-Q1	I_O = 0 mA, T_J = 25°C		0.2		mV
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		100	125	
			I_O = 50 mA			166	
			I_O = 75 mA, T_J = 25°C		150	188	
			I_O = 75 mA			250	
			I_O = 100 mA, T_J = 25°C		200	250	
			I_O = 100 mA			333	
			I_O = 150 mA, T_J = 25°C		300	375	
			I_O = 150 mA			500	
		TPS76350-Q1	I_O = 0 mA, T_J = 25°C		0.2		mV
			I_O = 1 mA, T_J = 25°C		2		
			I_O = 50 mA, T_J = 25°C		60	75	
			I_O = 50 mA			100	
			I_O = 75 mA, T_J = 25°C		90	113	
			I_O = 75 mA			150	
			I_O = 100 mA, T_J = 25°C		120	150	
			I_O = 100 mA			200	
			I_O = 150 mA, T_J = 25°C		180	225	
			I_O = 150 mA			300	

7.6 Typical Characteristics

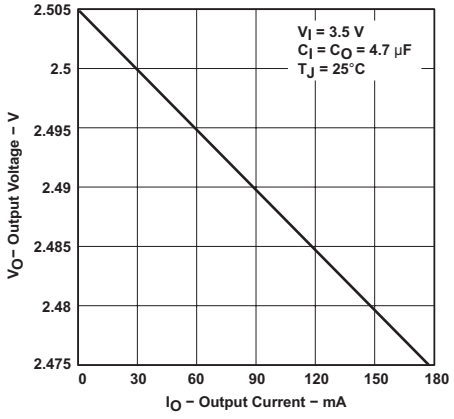


Figure 1. TPS76325-Q1 Output Voltage vs Output Current

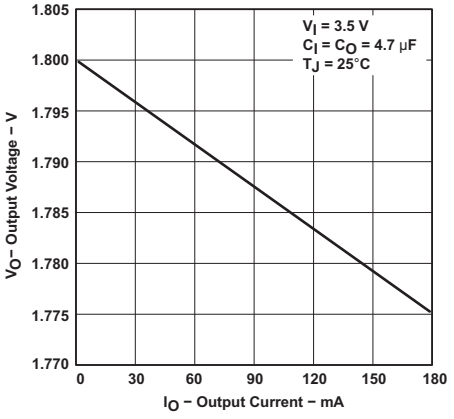


Figure 2. TPS76318-Q1 Output Voltage vs Output Current

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Typical Characteristics (continued)

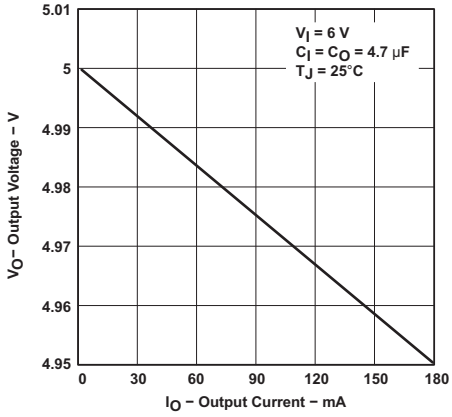


Figure 3. TPS76350-Q1 Output Voltage vs Output Current

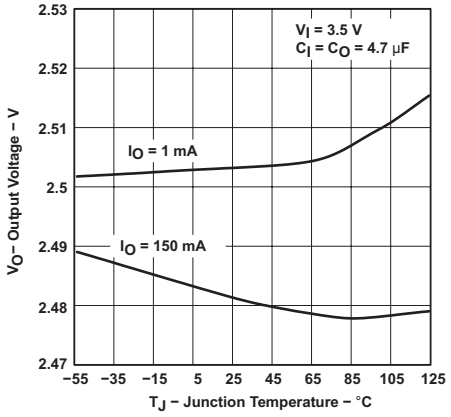


Figure 4. TPS76325-Q1 Output Voltage vs Free-Air Temperature

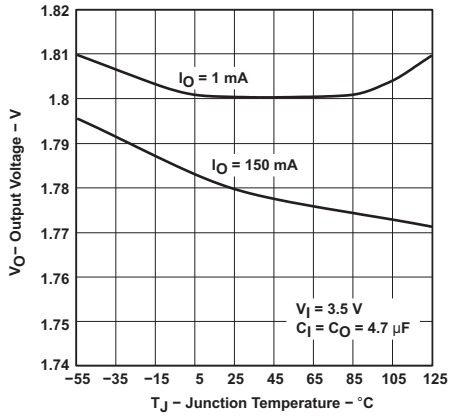


Figure 5. TPS76318-Q1 Output Voltage vs Free-Air Temperature

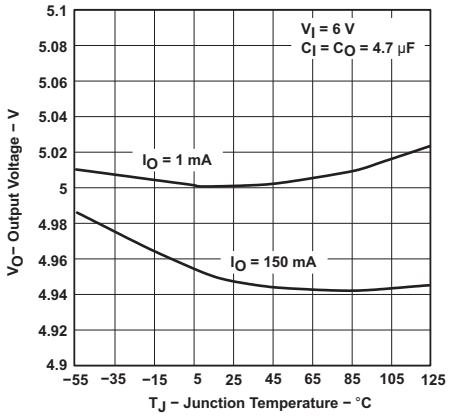


Figure 6. TPS76350-Q1 Output Voltage vs Free-Air Temperature

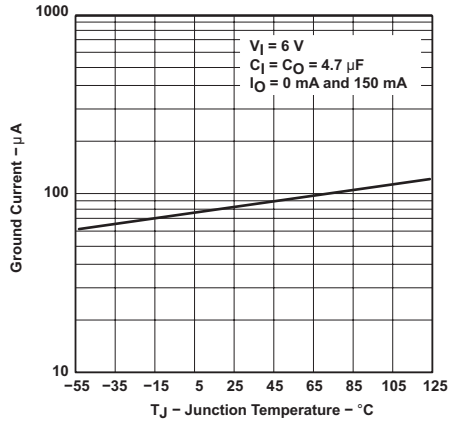


Figure 7. TPS76350-Q1 Ground Current vs Free-Air Temperature

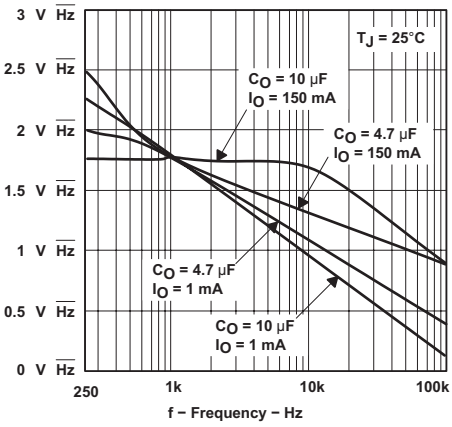


Figure 8. Output Noise vs Frequency

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Typical Characteristics (continued)

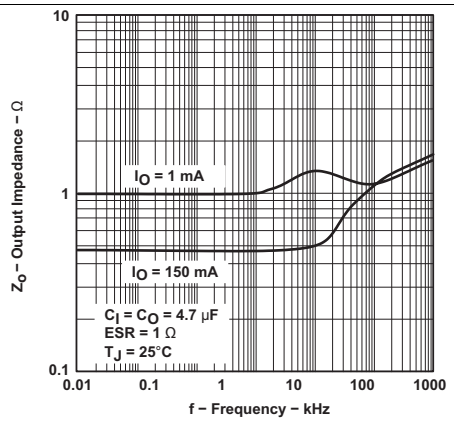


Figure 9. Output Impedance vs Frequency

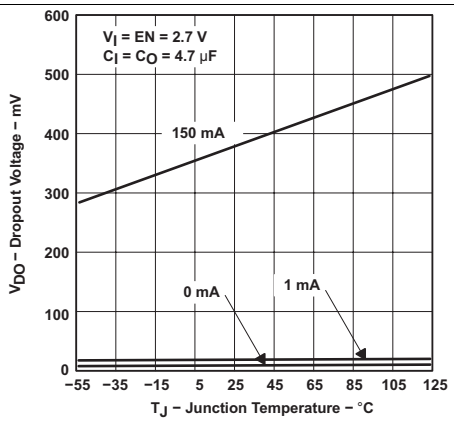


Figure 10. TYPS76325-Q1 Dropout Voltage vs Free-Air Temperature

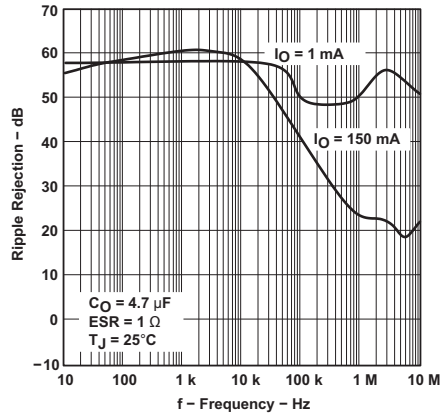


Figure 11. TPS76325-Q1 Ripple Rejection vs Frequency

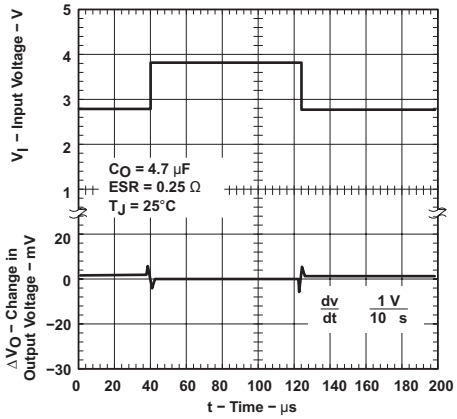


Figure 12. TPS76318-Q1 Line Transient Response

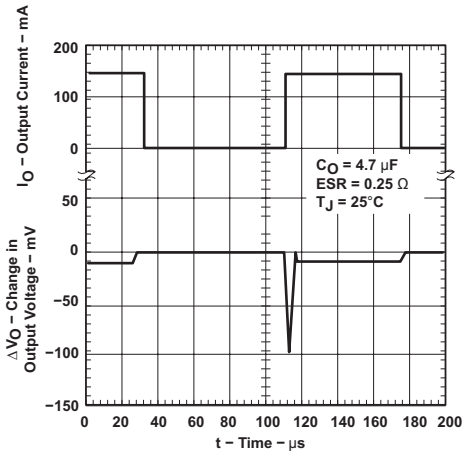


Figure 13. TPS76318-Q1 Load Transient Response

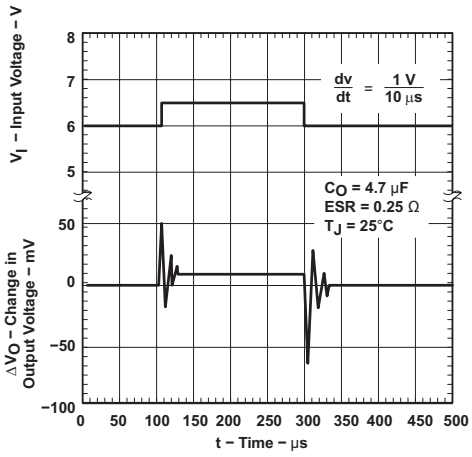


Figure 14. TPS76350-Q1 Line Transient Response

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Typical Characteristics (continued)

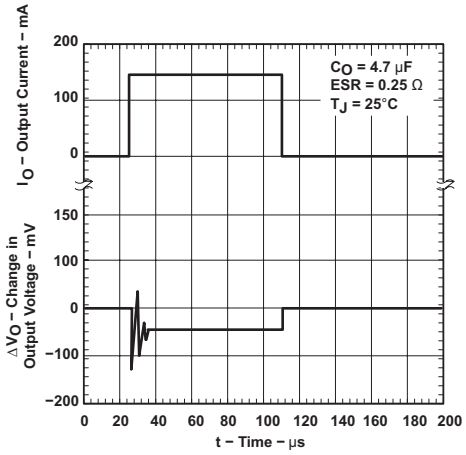


Figure 15. TPS76350-Q1 Load Transient Response

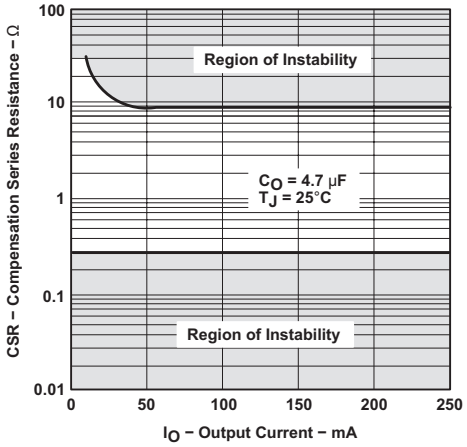


Figure 16. Typical Regions of Stability Compensation Series Resistance (CSR) vs Output Current

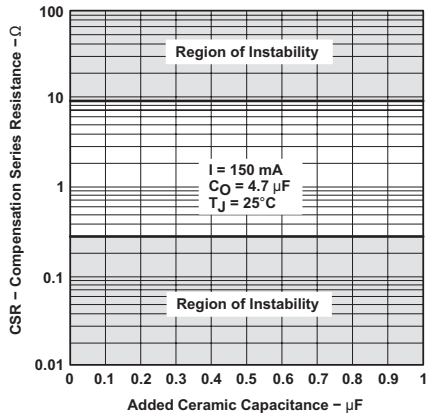


Figure 17. Typical Regions of Stability Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

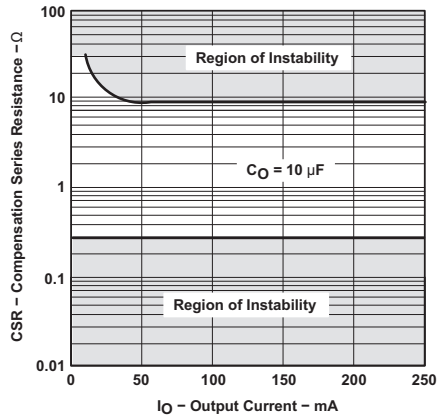


Figure 18. Typical Regions of Stability Compensation Series Resistance (CSR) vs Output Current

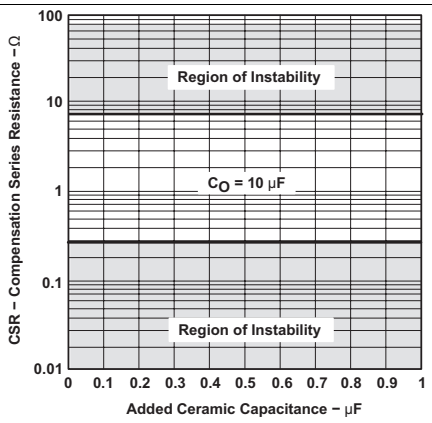


Figure 19. Typical Regions of Stability Compensation Series Resistance (CSR) vs Added Ceramic

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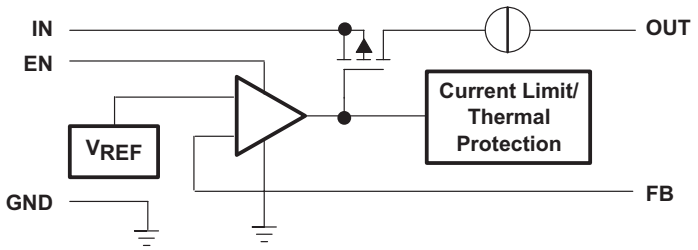
8 Detailed Description

8.1 Overview

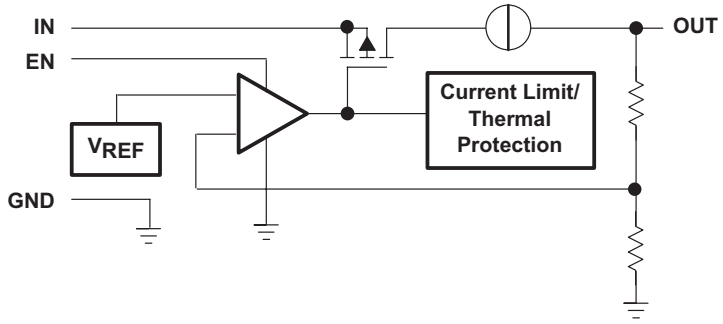
The TPS763xx-Q1 low-dropout (LDO) regulators are new families of regulators which have been optimized for use in battery-operated equipment and feature low dropout voltages, low quiescent current (140 µA), and an enable input to reduce supply currents to less than 2 µA when the regulator is turned off.

8.2 Functional Block Diagram

TPS76301-Q1



TPS76316/18/25/30/33/50-Q1



8.3 Feature Description

8.3.1 Regulator Protection

The TPS763xx-Q1 pass element has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

The TPS763xx-Q1 also features internal current limiting and thermal protection. During normal operation, the TPS763xx-Q1 limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, the regulator operation resumes.

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8.4 Device Functional Modes

8.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

8.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

8.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < VIN < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165°C$ (1)

(1) Approximate value for thermal shutdown

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS763xx-Q1 low-dropout (LDO) regulators are new families of regulators which have been optimized for use in battery-operated equipment and feature low dropout voltages, low quiescent current (140 µA), and an enable input to reduce supply currents to less than 2 µA when the regulator is turned off.

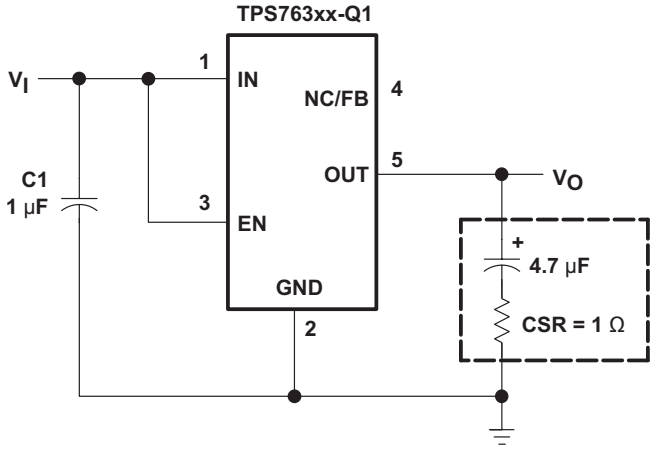
The TPS763xx-Q1 uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP pass element LDO designs. The PMOS pass element is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS763xx-Q1 is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

A logic low on the enable input, EN shuts off the output and reduces the supply current to less than 2 µA. EN should be tied high in applications where the shutdown feature is not used.

9.2 Typical Application

A typical application circuit is shown in Figure 20.



Note: TPS76316-Q1, TPS76318-Q1, TPS76325-Q1, TPS76301-Q1 TPS76333-Q1, TPS76350-Q1 (fixed-voltage options)

Figure 20. Typical Application Circuit

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Typical Application (continued)

9.2.1 Design Requirements

Table 2 lists the design requirements.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENTS
Input voltage	2.7 to 10 V
Output voltage	2.5 to 6.45 V
Output current	0 to 150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 External Capacitor Requirements

Although not required, a 0.047 µF or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763xx-Q1, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS763xx-Q1 requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 0.3 Ω and 10 Ω. Capacitor values of 4.7 µF or larger are acceptable, provided the ESR is less than 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7-µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above.

Table 3. Capacitor Selection

PART NO.	MFR.	VALUE	MAX ESR	SIZE (H × L × W)
T494B475K016AS	KEMET	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	SPRAGUE	10 µF	1.5 Ω	1.3 × 7.0 × 2.7
695D106x003562T	SPRAGUE	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6.0 × 3.2

9.2.2.2 Output Voltage Programming

The output voltage of the TPS76301-Q1 adjustable regulator is programmed using an external resistor divided as shown in figure 21. The output voltage is calculated using Equation 1.

$V_O = 0.995 \times VREF \times (1 + R1/R2)$

where

- V_{REF} = 1.192 V typical (the internal reference voltage)
- 0.995 is a constant used to center the load regulator (1%) (1)

Resistors R1 and R2 should be chosen for approximately 7-µA divider current. Lower value resistors can be used, but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using Equation 2.

$$\text{Line Reg.}\,(\text{mV}) = (\%/\text{V}) \times \frac{V_O (V_{Imax} - (V_O + 1)}{100} \times 1000 \quad (2)$$

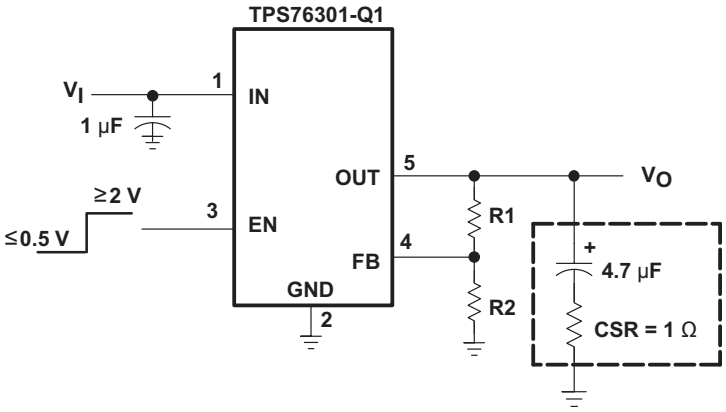


Figure 21. TPS76301-Q1 Adjustable LDO Regulator Programming

Table 4. Output Voltage Programming Guide

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)(1)	
	R1	R2
2.5	187	169
3.3	301	169
3.6	348	169
4	402	169
5	549	169
6.45	750	169

(1) 1% values shown.

9.2.3 Application Curves

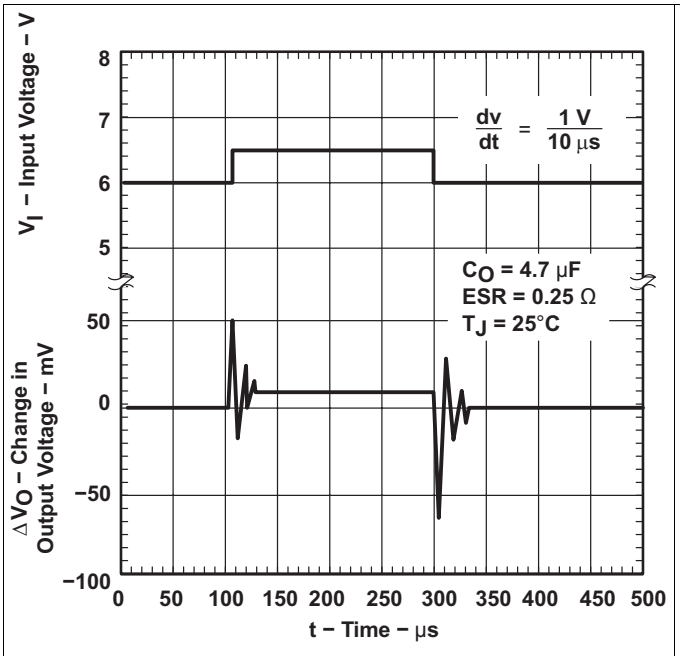


Figure 22. TPS76350-Q1 Line Transient Response

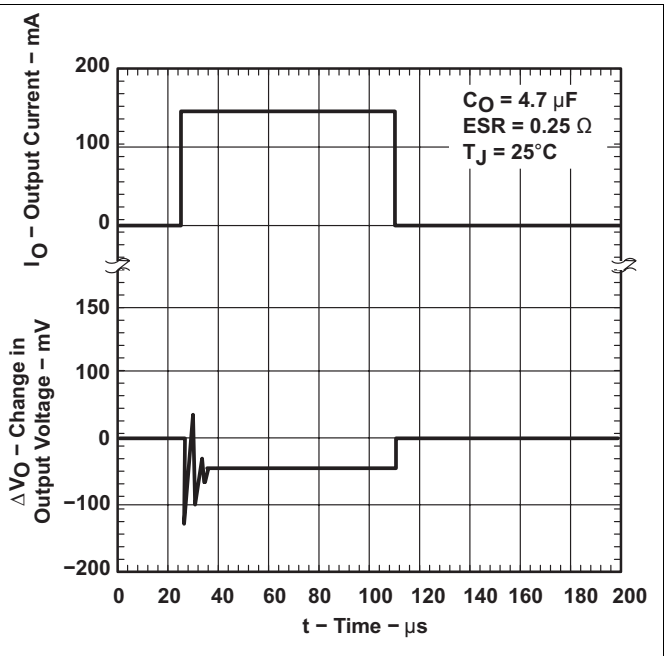


Figure 23. TPS76350-Q1 Load Transient Response

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10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 10 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. Although not required, a 0.047-µF or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763xx-Q1, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

11 Layout

11.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

11.2 Layout Example

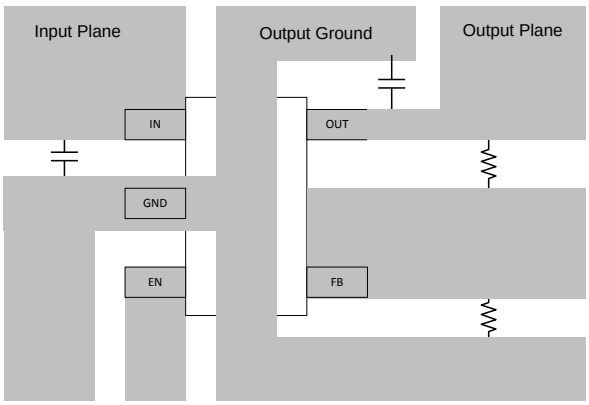


Figure 24. Recommended Layout

11.3 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$ and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3.

$$P_{D(max)} = T_{J(max)} – T_A / R_{\theta JA} \quad (3)$$

where

- $T_{J(max)}$ is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see *Thermal Information*
- T_A is the ambient temperature

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Power Dissipation and Junction Temperature (continued)

Use Equation 4 to calculate the regulator dissipation.

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

TPS793xx-Q1 Ultralow-Noise, High-PSRR, Fast RF 200-mA Low-Dropout Linear Regulators, SGLS162

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS763-Q1	Click here	Click here	Click here	Click here	Click here
TPS76301-Q1	Click here	Click here	Click here	Click here	Click here
TPS76316-Q1	Click here	Click here	Click here	Click here	Click here
TPS76318-Q1	Click here	Click here	Click here	Click here	Click here
TPS76325-Q1	Click here	Click here	Click here	Click here	Click here
TPS76330-Q1	Click here	Click here	Click here	Click here	Click here
TPS76333-Q1	Click here	Click here	Click here	Click here	Click here
TPS76350-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76301QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAN	
TPS76301QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAN	Samples
TPS76316QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAO	Samples
TPS76318QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAP	
TPS76318QDBVRQ1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAP	
TPS76325QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAQ	
TPS76330QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAT	
TPS76333QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAU	
TPS76333QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAU	Samples
TPS76350QDBVRG4Q1	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAW	
TPS76350QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS763-Q1 :

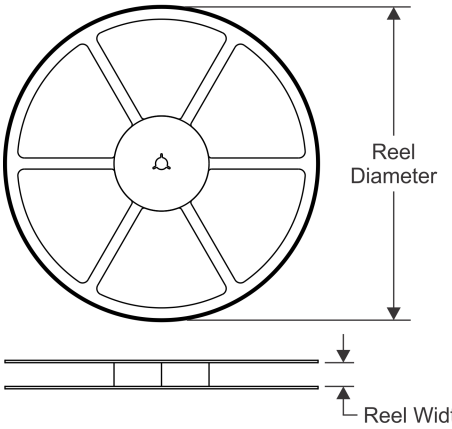
- Catalog : TPS763

NOTE: Qualified Version Definitions:

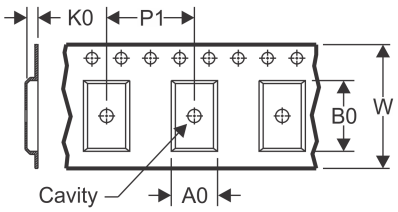
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

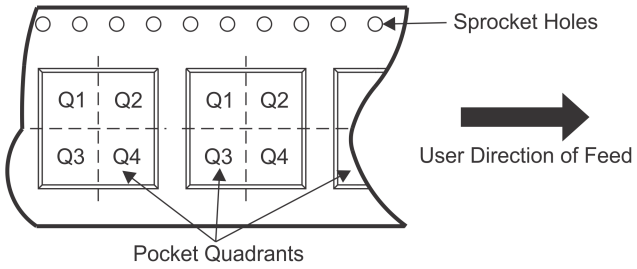


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

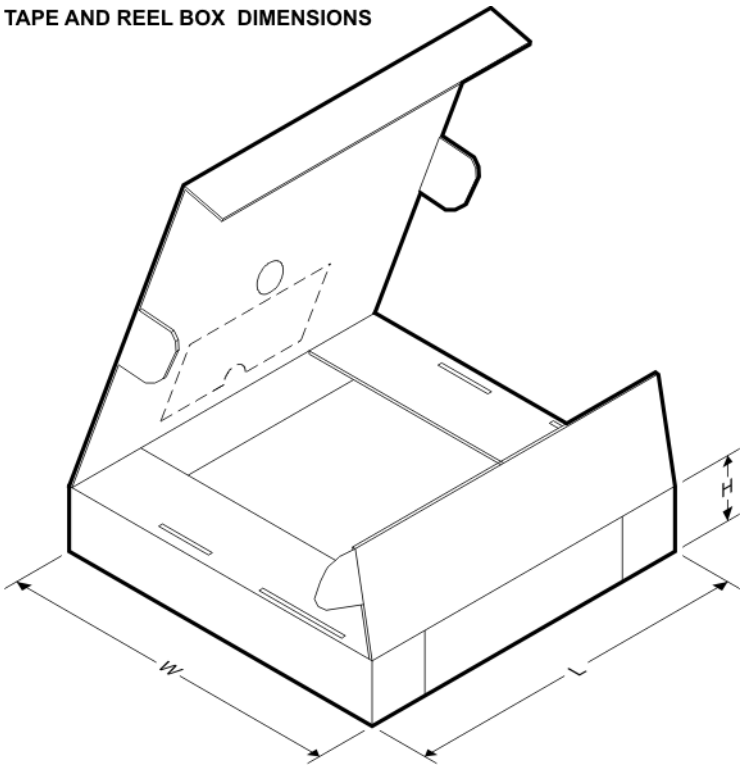
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76301QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76301QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76316QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76318QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76318QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76325QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76330QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76333QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76333QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76350QDBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS76350QDBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

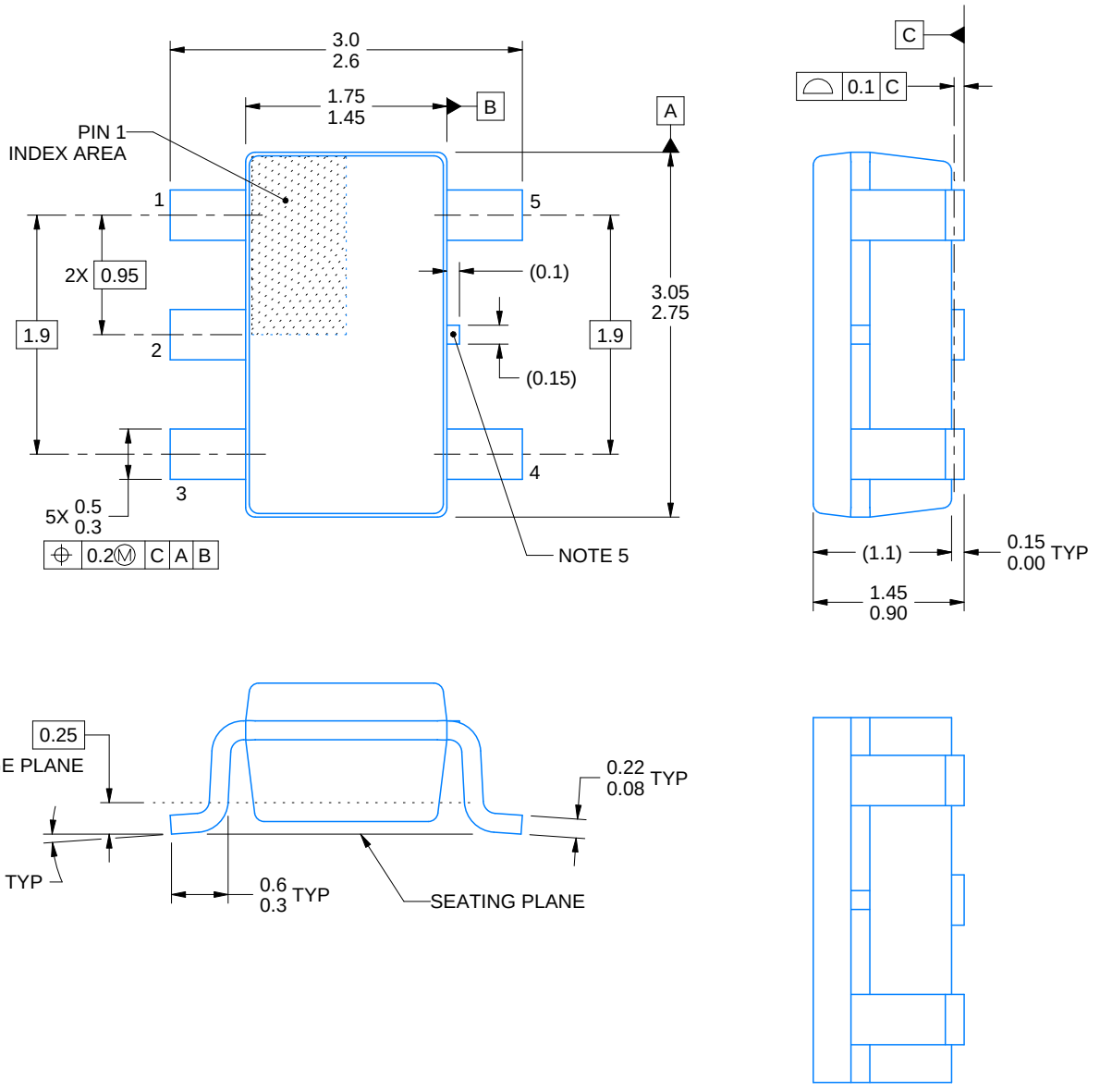
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76301QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76301QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76316QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76318QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76318QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76325QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76330QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76333QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76333QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76350QDBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS76350QDBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

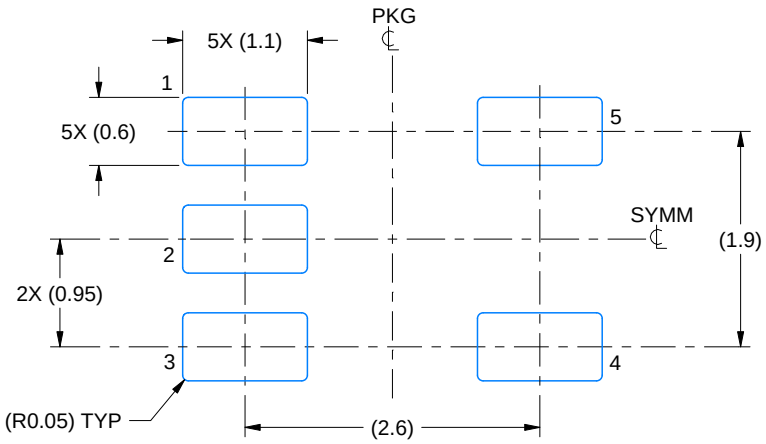


ALTERNATIVE PACKAGE SINGULATION VIEW

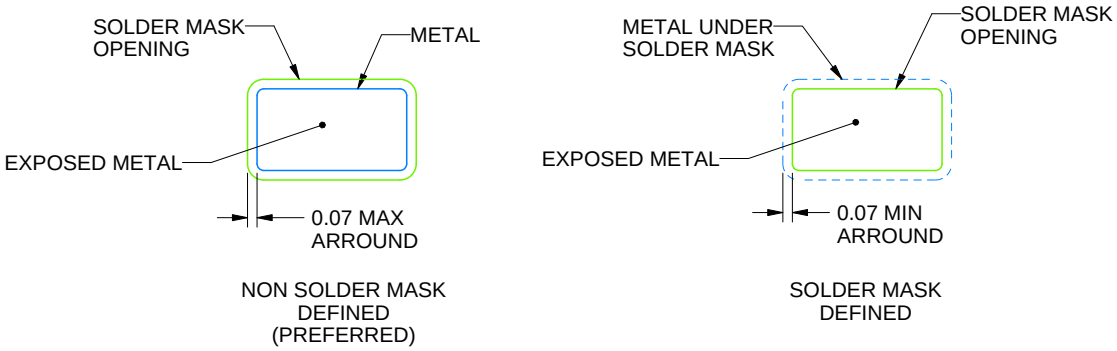
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

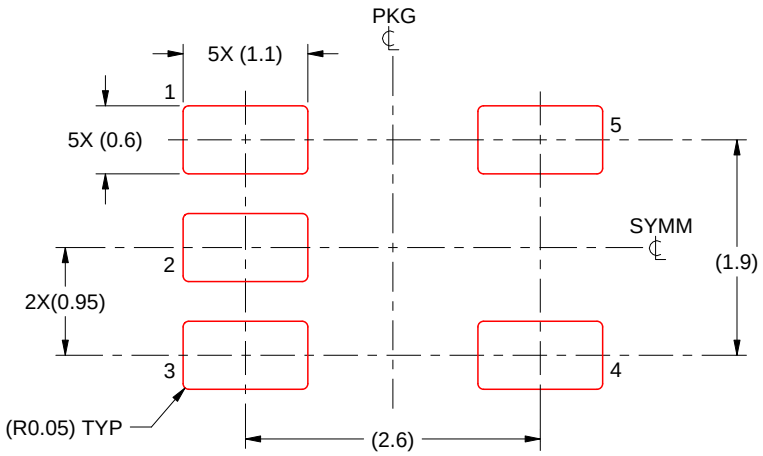


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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