Chapter 1
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Battery Backup System

The battery backup system can operate a real-time clock (RTC_B module) and retain some bytes in a backup RAM from a backup source when the primary supply fails. The battery backup system also includes a simple charging circuitry to charge capacitors connected to the backup supply. This chapter describes the battery backup system.

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The full user's guide can be downloaded from http://www.ti.com/lit/pdf/slau208.

Topic **Page**

1.1 Battery Backup Introduction

The battery backup system features include:

- Automatic and manual switching to the backup supply
- Backup-supplied backup subsystem that can contain:
  - Backup-supplied real-time clock with 32-kHz crystal oscillator (see the RTC_B chapter and Clock System chapter)
  - Backup-supplied backup RAM (see the Backup RAM chapter)
- Resistive charger for backup capacitors

NOTE: Operation without separate battery backup supply

If there is no separate battery backup supply in the system, connect the VBAT pin to DVCC and set bit BAKDIS=1.

1.2 Battery Backup Operation

The battery backup system supplies a subsystem from a secondary supply (VBAT) if the primary supply (DVCC) fails. The backup-supplied subsystem usually contains a real-time clock module (together with the required LF-crystal oscillator) and a backup RAM. These modules are described in their respective User's Guide chapters.

The high-side SVS (SVSH) that is located in the PMM module and supervises the primary supply (DVCC) controls the switching between primary and secondary supply.

NOTE: Restrictions

When the lowest high-side SVS level (00b) is used to monitor the primary supply, the temperature range is restricted to 0°C to 85°C.

Figure 1-1 shows an overview of the battery backup switch.

The secondary supply VBAT powers the backup-supplied subsystem

- at power on
- if bit BAKDIS = 0 in the BAKCTL register and
  - if the primary supply drops below the configured high-side SVS level
  - if the high-side SVS (SVSH) is disabled
  - during LPMx.5
  - if bit BAKSW=1 in the BAKCTL register

The primary supply DVCC powers the backup-supplied subsystem

- if the primary supply rises above the power-on level of the high-side SVS level
- if the primary supply remains above the configured high-side SVS level
- if bit BAKDIS = 1 in the BAKCTL register

If the backup-supplied subsystem is powered by the secondary supply VBAT, the access and control to modules located in the subsystem is restricted:

- The data stored in the backup RAM is retained but cannot be accessed.
- The RTC, if enabled, together with the 32-kHz crystal oscillator continue to operate but the time and date information cannot be accessed.
- Changes to the LF crystal oscillator setting in the clock system do not take effect.

If the backup-supplied subsystem is powered by the primary supply DVCC and LOCKBAK = 0, the modules located in the subsystem can be access and controlled normally.

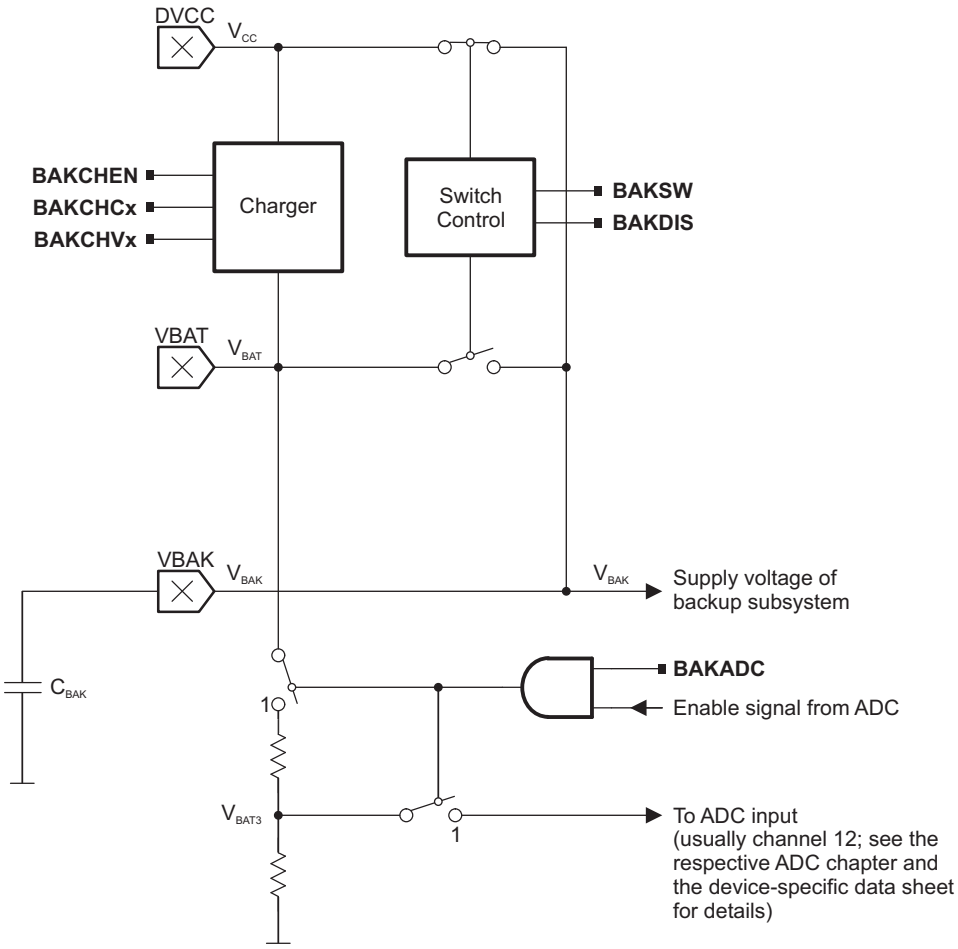

Figure 1-1. Battery Backup Switch Overview

NOTE: C_{BAK} shown in Figure 1-1 is used to ensure proper decoupling during a switchover event. See the device-specific data sheet for recommended values. This capacitance should not be confused with an external capacitor that may be placed on VBAT to maintain charge during backup operation in the application.

1.2.1 Activate Access to Backup-Supplied Subsystem

If the backup-supplied subsystem is powered by the secondary supply VBAT the LOCKBAK bit is automatically set. While LOCKBAK=1 it is impossible to access to the information stored in the backup-supplied subsystem. After its supply switched back to the primary supply do the following steps to get access to it :

1. Initialize the configuration registers of the real-time clock module exactly the same way as they were configured before the switch to the secondary supply.
2. Clear the LOCKBAK bit in the BAKCTL register.
3. Check the LOCKBAK bit.
   If LOCKBAK = 0, continue with the next step.
   If LOCKBAK = 1, the supply for the backup-supplied subsystem has not settled yet. Continue with step 2.
4. Enable RTC interrupts.
5. The enabled RTC interrupts will now be serviced as normal interrupts.

1.2.2 Manual Switching

The backup-supplied subsystem is always powered from the secondary supply VBAT if the bit BAKSW in the Battery Backup Control register BAKCTL is set to 1. A POR resets the BAKSW bit, and the system returns to automatic switch control.

1.2.3 Disable Switching

If the bit BAKDIS in the Battery Backup Control register BAKCTL is set to 1, the battery backup system is disabled and the backup-supplied subsystem is always powered from the primary supply DVCC. A POR resets the BAKDIS bit, and the system returns to automatic switch control.

1.2.4 Measuring the Supplies

With an integrated ADC, the primary and secondary supplies can be measured. Select the channel of the ADC that is reserved to measure the supply voltage of the device. This is usually ADC channel 12; see the respective ADC chapter and the device-specific data sheet for details.

If BAKADC = 0, VBAT measurement is disabled.

If BAKADC = 1, the secondary supply VBAT is measured.

The resistive dividers are connected to the supplies only during the sampling phase of the ADC.

1.2.5 LPMx.5 and Backup Operation

During LPMx.5 (LPM3.5 or LPM4.5), the backup subsystem is always supplied from the backup battery, except when switching is completely disabled by setting the BAKDIS bit.

If using a capacitor to source the backup supply, the device can wake up regularly from LPMx.5, recharge the capacitor, and return to LPMx.5. The time interval must be designed such that the remaining charge on the capacitor is always sufficient to bridge the worst-case backup time (that is, the time without any primary supply).

1.2.6 Resistive Charger

Together with the battery backup switch, a resistive charging circuit is implemented to charge capacitors connected to the backup supply. A simplified block diagram of the charger is shown in Figure 1-2. The charger is enabled by writing the correct password (069h) into the upper byte of BAKCHCTL, together with BAKCHEN = 1, selecting a charging resistor with BAKCHCx ≠ 00b, and a charge end voltage with BAKCHVx ≠ 00b. Writing to the charger control register with an incorrect password disables the charger, and all control register bits are reset to 0.

If V_{CC} is selected as charge end voltage with BACKCHVx = 01b (or if V_{CC} < 2.7 V with BACKCHVx = 10b), an attached capacitor is charged to V_{CC} with $V_{BAT}(t) \approx V_{CC} \times (1 - \exp(-t/RC)$, with R being the selected charging resistor and C being the capacitor attached to pin VBAT (this is **not** C_{BAK}).

If a charge end voltage of 2.7 V is selected (BACKCHVx = 10b) and V_{CC} > 2.7 V, then an attached capacitor is charged with $V_{BAT}(t) \approx V_{CC} \times (1 - \exp(-t/RC)$ (same as above) but as soon as V_{BAT} reaches approximately 2.7 V, the charging process is halted. If V_{BAT} drops by approximately 70 mV (the comparator hysteresis), the charging process continues again until the capacitor connected to pin VBAT is again charged to approximately 2.7 V. Note: For low power reasons, the V_{BAT} voltage is compared against the 2.7-V limit only once during each VLO clock cycle, and only then is charging disabled or re-enabled.

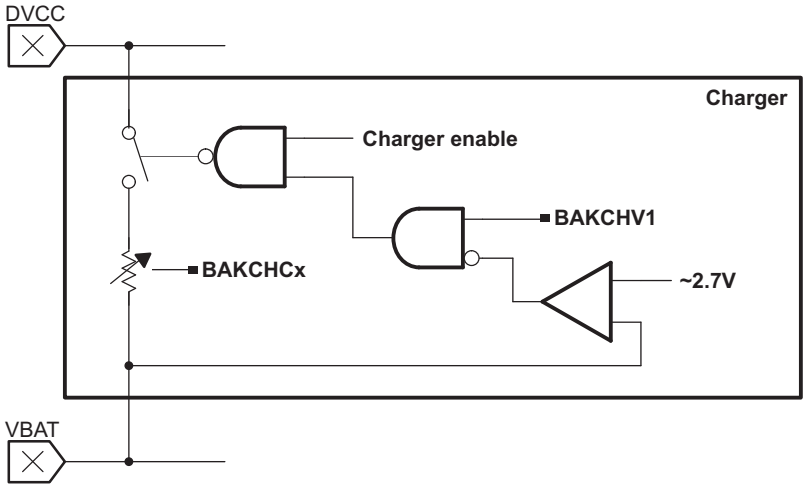

Figure 1-2. Charger Block Diagram

1.3 Battery Backup Registers

The battery backup registers are listed in Table 1-1. The base address for the backup RAM registers can be found in the device-specific data sheet. The address offsets are given in Table 1-1.

Table 1-1. Battery Backup Registers

Offset	Acronym	Register Name	Type	LPMx.5, Backup Retention	Section
00h	BAKCTL	Battery Backup Control	Read/write	not retained	Section 1.3.1
02h	BAKCHCTL	Battery Charger Control	Read/write	not retained	Section 1.3.2

1.3.1 BAKCTL Register

Battery Backup Control Register

Figure 1-3. BAKCTL Register

15	14	13	12	11	10	9	8
Reserved							
r	r	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved				BAKDIS	BAKADC	BAKSW	LOCKBAK
r0	r0	r0	r0	rw	rw-(0)	rw-(0)	r/w0-[1]

Table 1-2. BAKCTL Register Description

Bit	Field	Type	Reset	Description
15-4	Reserved	R	0h	Reserved. Always reads as 0.
3	BAKDIS	RW	0h	Disable backup supply switching. Reset to 0 after a complete power cycle. 0b = Backup supply switching enabled 1b = Backup supply switching disabled. Backup subsystem always powered from VCC (also during LPMx.5).
2	BAKADC	RW	0h	Battery backup supply to ADC 0b = Vbat measurement disabled 1b = Vbat measurement enabled
1	BAKSW	RW	0h	Manual switch to battery backup supply 0b = Switching is automatic 1b = Switch to battery backup supply
0	LOCKBAK	RW	0h	Lock backup subsystem. Can only be written as 0. The LOCKBAK bit should only be written as 0 after configuring the RTC control registers. This ensures that RTC will not be stopped after leaving backup or LPMx.5 mode. SVSH has to be active when LOCKBAK bit is cleared. LOCKBAK is always set to 1 by hardware after the core was powered down either due to a complete power cycle of the main supply DVCC or due to LPMx.5 operation. 0b = Backup subsystem not locked 1b = Backup subsystem locked

1.3.2 BAKCHCTL Register

Battery Charger Control Register

Figure 1-4. BAKCHCTL Register

15	14	13	12	11	10	9	8
BAKCHKEYx							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Reserved		BAKCHVx		Reserved	BAKCHCx		BAKCHEN
r0	r0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 1-3. BAKCHCTL Register Description

Bit	Field	Type	Reset	Description
15-8	BAKCHKEYx	RW	5Ah	Charger access key. Always read as 05Ah. Must be written as 069h together with low byte; any other write disables the charger and all control register bits are reset to 0.
7-6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	BAKCHVx	RW	0h	Charger end voltage 00b = Charger disabled 01b = VCC 10b = Approximately 2.7 V, or VCC if VCC is lower than 2.7 V 11b = Reserved
3	Reserved	R	0h	Reserved. Always reads as 0.
2-1	BAKCHCx	RW	0h	Charger charge current 00b = Charger disabled 01b = Charge current defined by a maximum 5-kΩ resistor 10b = Charge current defined by a maximum 10-kΩ resistor 11b = Charge current defined by a maximum 20-kΩ resistor
0	BAKCHEN	RW	0h	Charger enable 0b = Charger disabled 1b = Charger enabled

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265