ControlNet™ Applications With the SN65HVD61 PHY

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ABSTRACT

This application note is a guide for using the SN65HVD61 physical layer transceiver (PHY) for ControlNet industrial data communications network applications. Designers familiar with existing ControlNet PHY implementations will find guidance for converting to the SN65HVD61, which offers cost-effective improvements in board space, power consumption, and robustness. In addition to advice for drop-in replacement, we also present suggestions for taking advantage of the new features of the SN65HVD61 (hereafter also referred to as the HVD61), including low-voltage MAC interface, signal diagnostics, and enable/disable functions.

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1 Introduction to ControlNet

1.1 Overview

ControlNet is an open standard network that meets the demands of industrial applications requiring high speed (5 Megabits per second), high throughput with predictable and repeatable transfers of mission critical data.

ControlNet is one of the network technologies that comprise the family of networks built on the Common Industrial Protocol. ControlNet meets the demands of real-time, high speed applications at the automation and control layer for integration of complex control systems such as coordinated drive systems, weld control, motion control, vision systems, complex batch control systems, process control systems with large data requirements, and systems with multiple controllers and human-machine interfaces. ControlNet is effective for systems with multiple PC-based controllers and Programmable Logic Controller (PLC)-to-PLC and PLC-to-Digital Control System (DCS) communication. ControlNet allows multiple controllers – each with their own I/O and shared inputs – to talk to each other, with any possible interlocking combination.

ControlNet can be implemented on several different types of media, including copper coax cable, fiber optic cable, and fiber ring, with variations for media redundancy and intrinsically-safe applications. In this application note, the discussion is limited to copper coax cable implementations.

ControlNet supports a maximum of 99 nodes, with no minimum distance limitation between nodes. It offers high network efficiency with multicast of inputs and peer-to-peer data, using a Producer/Consumer communication model that allows the user to configure devices, control actions, and collect information over a single network

More information about ControlNet can be obtained from the ControlNet International website: http://www.odva.org

1.2 Physical Layer

ControlNet's coax media specifies RG-6 quad shield cable, which is relatively inexpensive and used widely in the cable TV industry. The standard provides support for bus, star, or tree topologies to meet various application needs. Passive taps can be installed anywhere on the trunk with no minimum spacing requirements.

In a typical ControlNet application, several nodes will be connected to a common bus, as shown in Figure 1. At any time, only one node should drive the bus; all active nodes continually receive the bus state. The node, which is actively driving the bus, will sink current through one of the HVD61 drivers, causing the voltage on the bus to be either differential high or differential low.

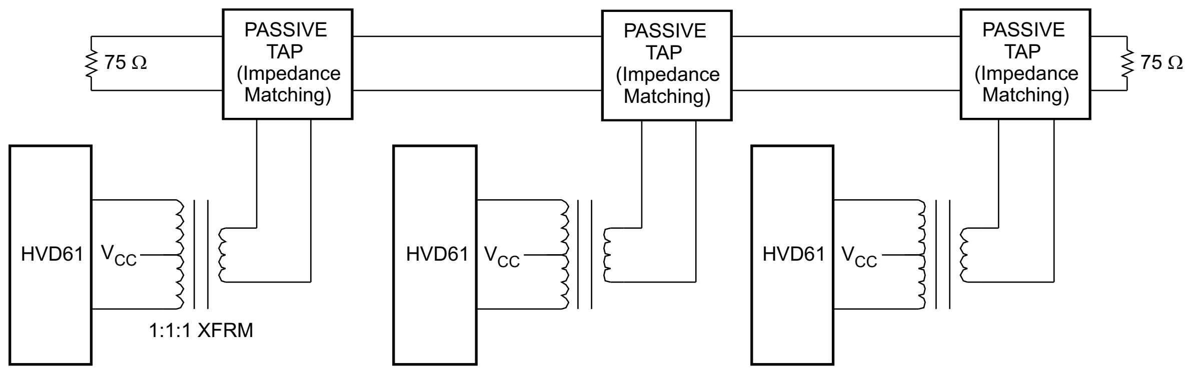

Figure 1. ControlNet Applications

2 The SN65HVD61 ControlNet PHY

2.1 Circuit Placement with MAC and Transformer

The SN65HVD61 transceiver is a mixed-signal (digital and analog) device that translates the logic signals between the Media Access Controller (MAC) and the ControlNet bus lines. The logic signals to and from the MAC are compatible with TTL, LVTTL, or CMOS logic levels. The XF1 and XF3 pins (see Figure 3) are designed to connect with a pulse transformer as specified by the ControlNet specification.

Figure 2 shows the connections between the MAC and the HVD61. For simplicity, power supply connections and external protection components are not shown.

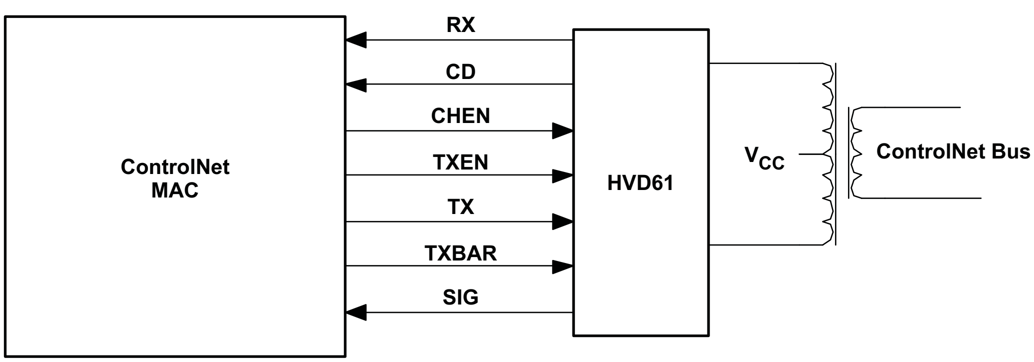

Figure 2. HVD61 PHY Connects the MAC to the ControlNet Bus

2.2 Block Diagram of the HVD61

Figure 3 shows a block diagram of the HVD61 ControlNet transceiver. Each of the functional blocks is implemented in proven Linear BiCMOS process technology. The transceiver is packaged in a standard 14-pin small-outline integrated circuit (SOIC). Full specifications for the performance and operating conditions of the HVD61 are detailed in the SN65HVD61 datasheet available at www.ti.com.

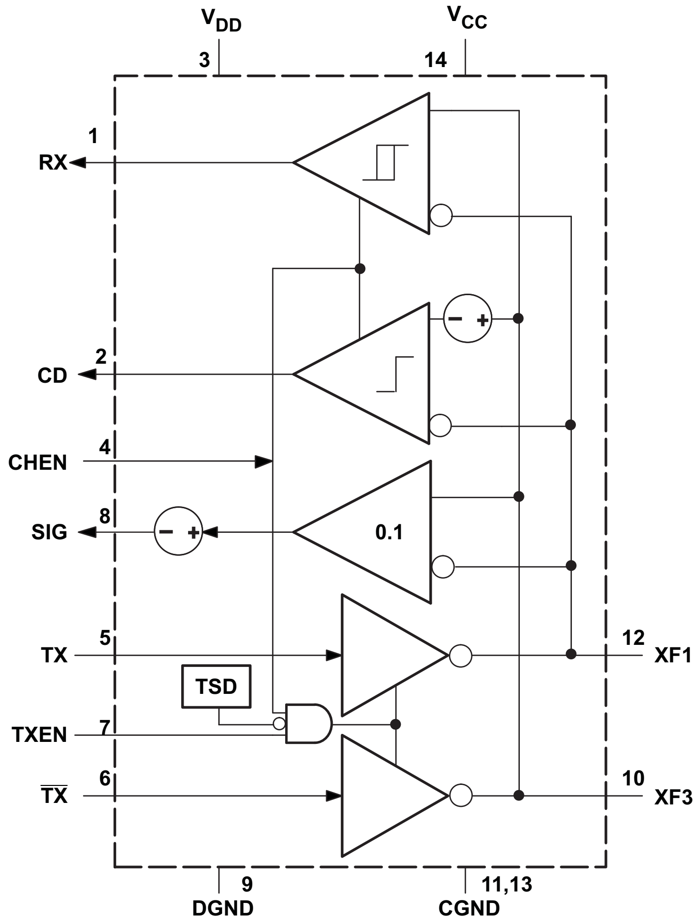

Figure 3. HVD61 Block Diagram

3 Replacing the Hybrid Module With the HVD61

Rockwell Automation® (formerly Allen Bradley®) has supplied single-channel and dual-channel ControlNet transceivers for several years. Each hybrid transceiver module implements the requirements of a coax transceiver when combined with a transformer and certain external components for electromagnetic compatibility. The hybrid transceiver functionally replaces about 50 discrete surface-mount components, in a Single-In-line Package (SIP) as shown in Figure 4.

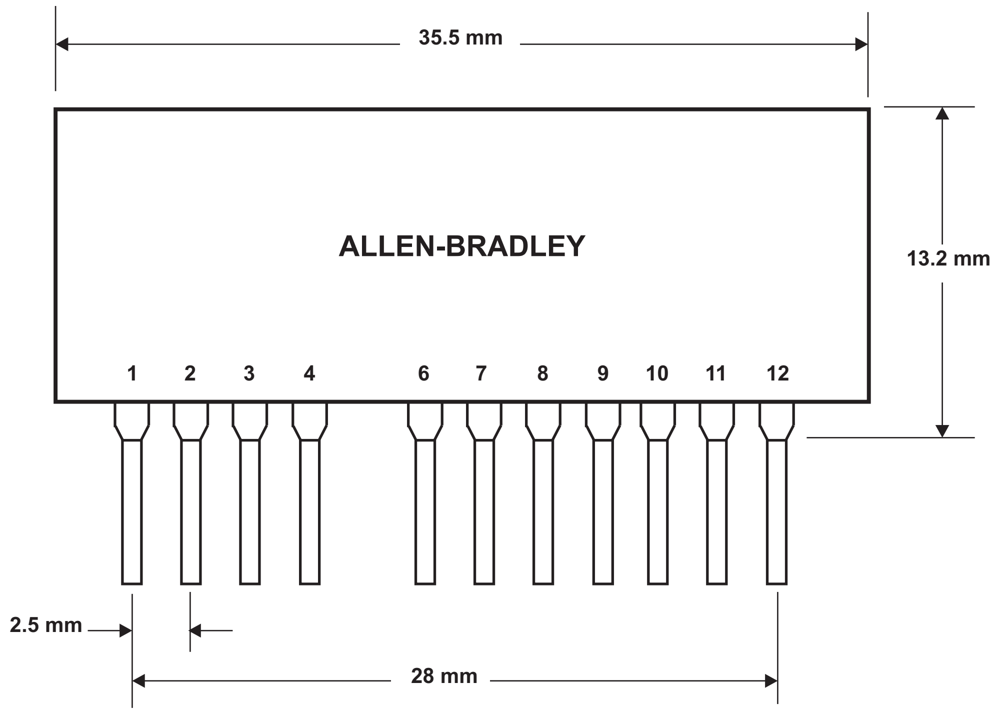

Figure 4. Hybrid Package (Single Channel)

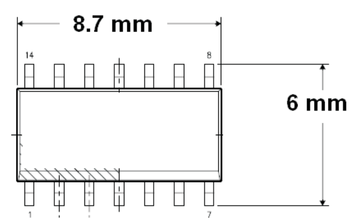

Figure 5. SN65HVD61 Package (Single Channel)

3.1 Compatibility With Existing Solutions

3.1.1 ControlNet Standard Requirements

All the requirements for ControlNet communications are specified to be measured relative to the bus lines, which are coupled to the SN65HVD61 by a transformer as shown in Figure 2. Therefore, the transceiver specifications given in the SN65HVD61 datasheet reflect the bus requirements with additional parameters needed to ensure that the overall interface performs as needed.

An example of this is the level of the transmitted signal. On the bus, the signal amplitude is required to be at least 6.9 V_{pp} when loaded with 37.5 Ω (two 75 Ω termination resistors in parallel). In the HVD61 datasheet, this is assured by specification of the low-state and high-state voltages of the driver outputs at XF1 and XF3. The outputs are symmetrical and should be driven in complementary phase, so that XF1 presents a high output when XF3 presents a low output, and vice versa. The high output is specified to be at least V_{CC}-0.05 V, and the low output is specified to be not more than 1.2 V. Even with a V_{CC} supply as low as 4.75 V, this produces a differential voltage of at least 4.70 V – 1.20 V = 3.50 V. Reflecting this signal through the 1:1 ControlNet transformer, this minimum bus voltage of ±3.5 V exceeds the requirement of 6.9 V_{pp}. Figure 6 illustrates how the HVD61 conforms to the ControlNet requirements for transmits levels

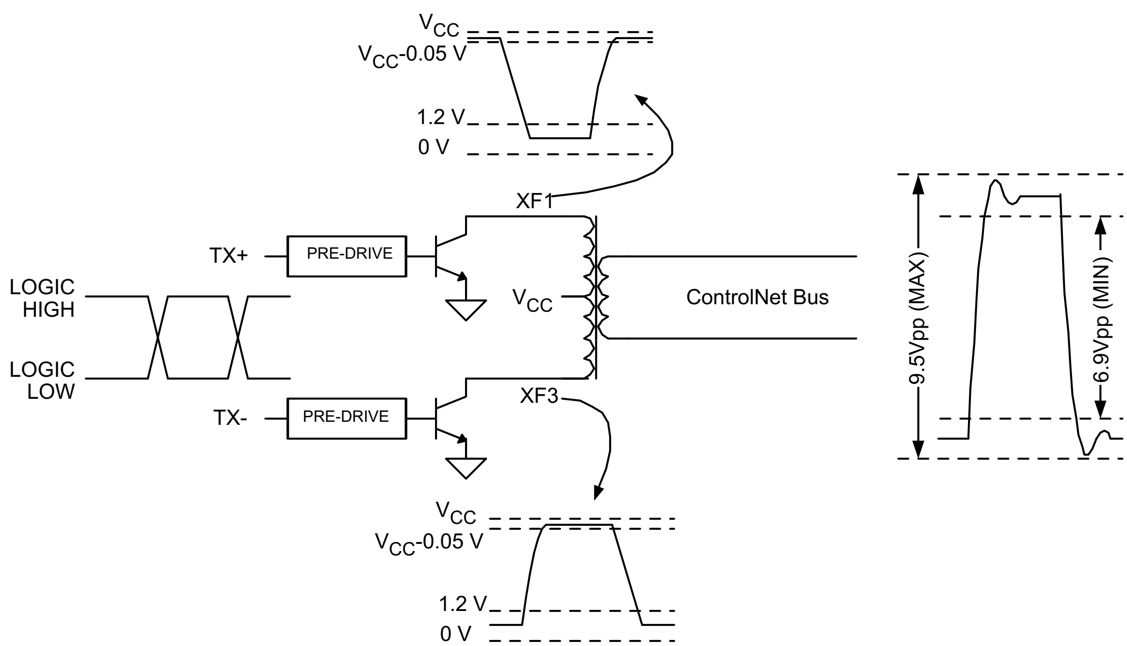

Figure 6. Transmitted Signal Levels

3.1.2 Similarity to Hybrid Characteristics

The design of the HVD61 is such that a ControlNet node using the HVD61 has performance that matches the characteristics of nodes using the existing hybrid transceiver in all critical parameters. This assures interoperability of networks with mixed old and new types of transceivers. This also assures compatibility of the HVD61 for applications replacing the existing hybrid transceiver.

To demonstrate interoperability between the HVD61 and hybrid transceivers, the test set-up shown in Figure 7 was used to observe typical bus signal data. Standard ControlNet components were used to illustrate a simple application.

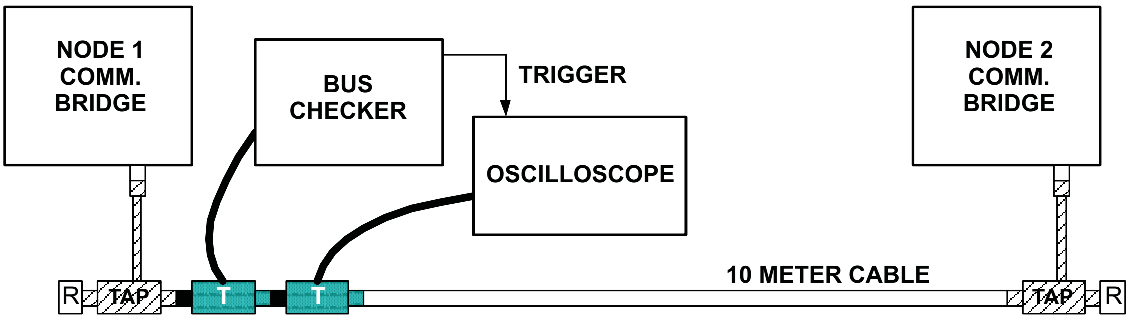

Figure 7. Test Set-up Demonstrates Interoperability of Old and New Transceivers

Table 1. Components Used in Interoperability Demonstration

MANUFACTURER	DESCRIPTION	PART NUMBER	QUANTITY
Allen-Bradley	ControlNet Communications Bridge	1756-CNBR/D	2
Allen-Bradley	ControlLogix Power Supply	1756-PA72/B	1
Allen-Bradley	ControlLogix 4-Slot Chassis	1756-A4/A	1
Allen-Bradley	Passive Tap	1786 TPR/B	2
	75 Ω Coax Terminator		2
Belden	Quad Shield ControlNet Cable	3092A	10 meters
Allen-Bradley	Net Checker	1788 CNCHR/A	1

The following figures show oscilloscope traces of bus activity with two nodes communicating. In each pair of figures, the first figure shows two hybrid (old) transceivers communicating, and the second figure shows one SN65HVD61 (new) and one hybrid (old) transceiver communicating. Note that there is no noticeable difference in the signaling between the two different combinations.

In Figure 8 and Figure 9, we see two bursts of communication signals, one from Node 1 at the near end of the cable, and one from Node 2 at the far end of the cable. No particular details are intended, but these traces give an overview for the total communications sequence. The blue (top) trace in both figures is the synchronization trigger signal from the bus checker. This trigger signal can be used to select either Node 1 or Node 2 for the more detailed traces to follow.

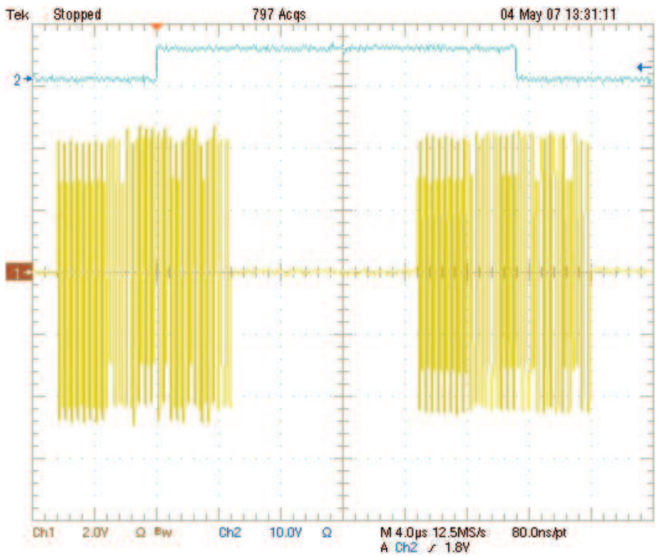

Figure 8. Hybrid and Hybrid Communication

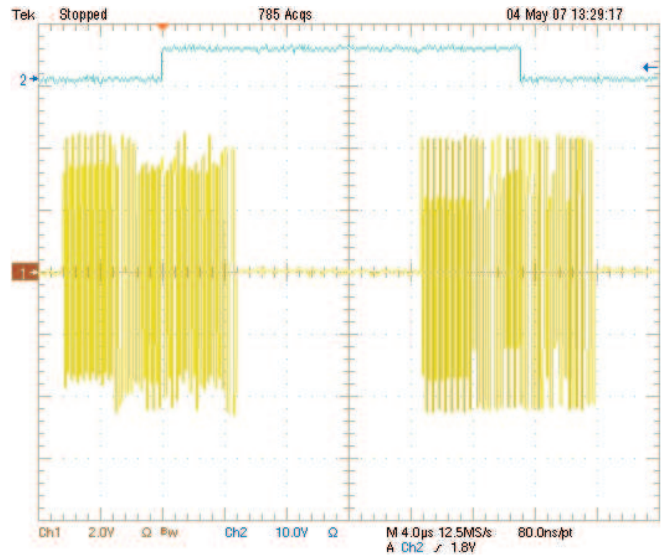

Figure 9. SN65HVD61 and Hybrid Communication

In Figure 10 and Figure 11, the synchronization trigger is set for Node 1. The bus signal trace shows the characteristics of amplitude (>6.9 V_{pp}) and bit width (either 100 ns or 200 ns depending on Manchester code symbol) that are appropriate for ControlNet signaling.

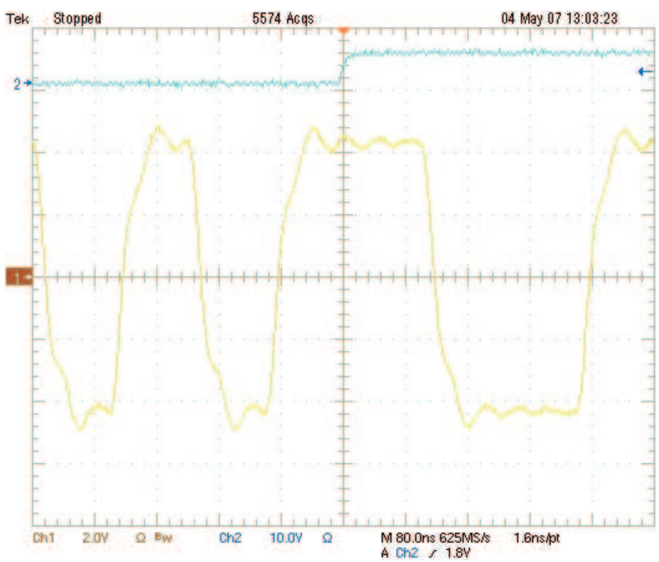

Figure 10. Hybrid and Hybrid Communication – Trigger on Node 1

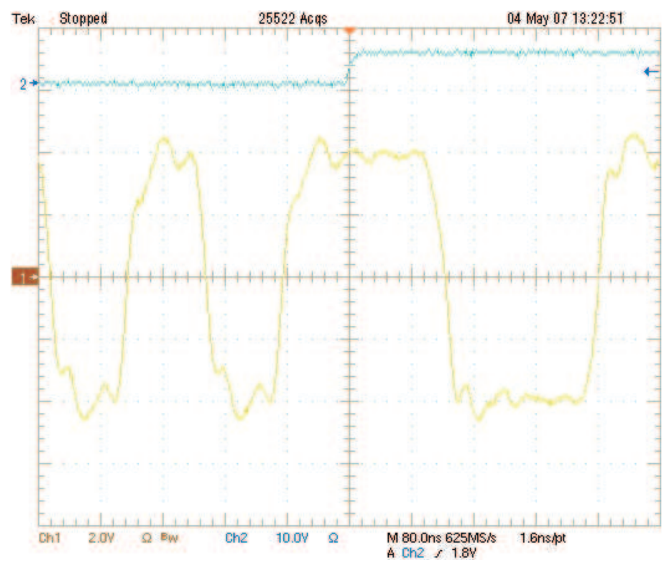

Figure 11. SN65HVD61 and Hybrid Communication – Trigger on Node 1

In Figure 12 and Figure 13, the synchronization trigger is set for Node 2. The effects of the cable losses are evident as some of the higher frequencies have been attenuated, but the signal retains the characteristics of valid ControlNet signaling.

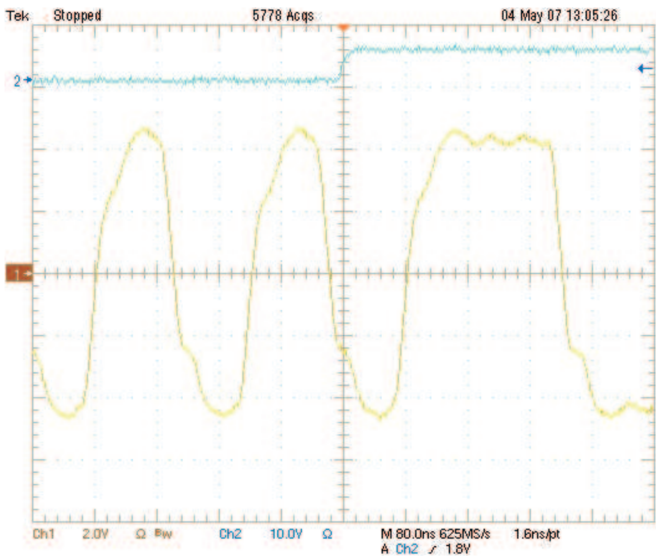

Figure 12. Hybrid and Hybrid Communication – Trigger on Node 2

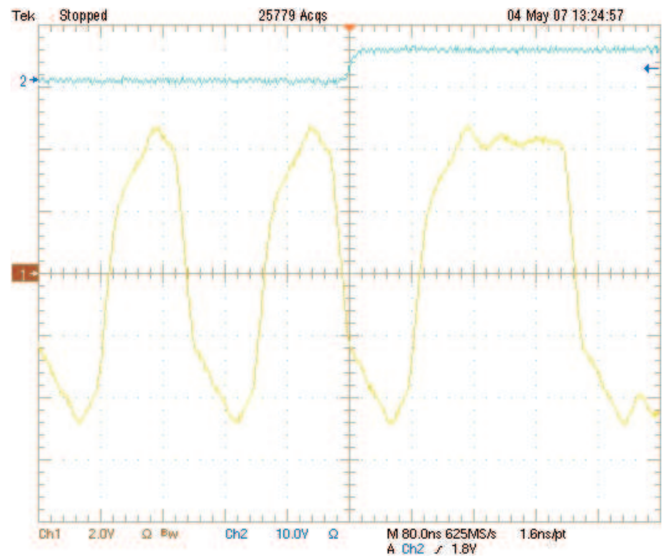

Figure 13. SN65HVD61 and Hybrid Communication – Trigger on Node 2

3.2 Single-Channel Application

In single-channel applications, one SN65HVD61 can be configured to function in place of one coax transceiver hybrid (Rockwell Automation part number 94180202). For some applications, the HVD61 may be used to directly replace the hybrid transceiver, without taking advantage of the additional features the HVD61 implements. In these applications, Table 2 shows the pin-to-pin equivalence between the SIP hybrid and the SOIC HVD61.

Table 2. SN65HVD61 Pin Assignments for Direct Replacement of a Single-Channel Hybrid

HYBRID PIN		SN65HVD61 PIN		
1	XF3_A	10	XF3	Connections to transformer
2	XF1_A	12	XF1	
3	TX_A	5	TX	Complementary transmit inputs
4	TXBAR_A	6	TXBAR	
5	No pin			
6	RX_A	1	RX	Receiver output
7	V_{CC}	3, 14	VDD, VCC	5-V supply
8	CD_A	2	CD	Carrier Detect
9	TXEN_A	7	TXEN	Transmit Enable
10	n/c			No connection
11	n/c			No connection
12	GND	9, 11, 13	DGND, GND	Signal grounds
		4	CHEN	Chip Enable – connect to Vcc
		8	SIG	Signal Strength – no connection

Note that in these direct-replacement applications, both supply lines (Vcc and VDD) should be tied to a single 5-V supply. Also, all ground pins (DGND and both CGND pins) should be tied to the common signal ground

3.2.1 External Components

In order to achieve system-level performance similar to the hybrid transceiver, applications replacing the hybrid with the HVD61 should use the same external components as in previous designs. These external components include decoupling capacitors on the power supply and protection devices on the bus signals.

During system-level testing with the HVD61, external components were used as suggested by Rockwell Automation, as shown in Figure 14.

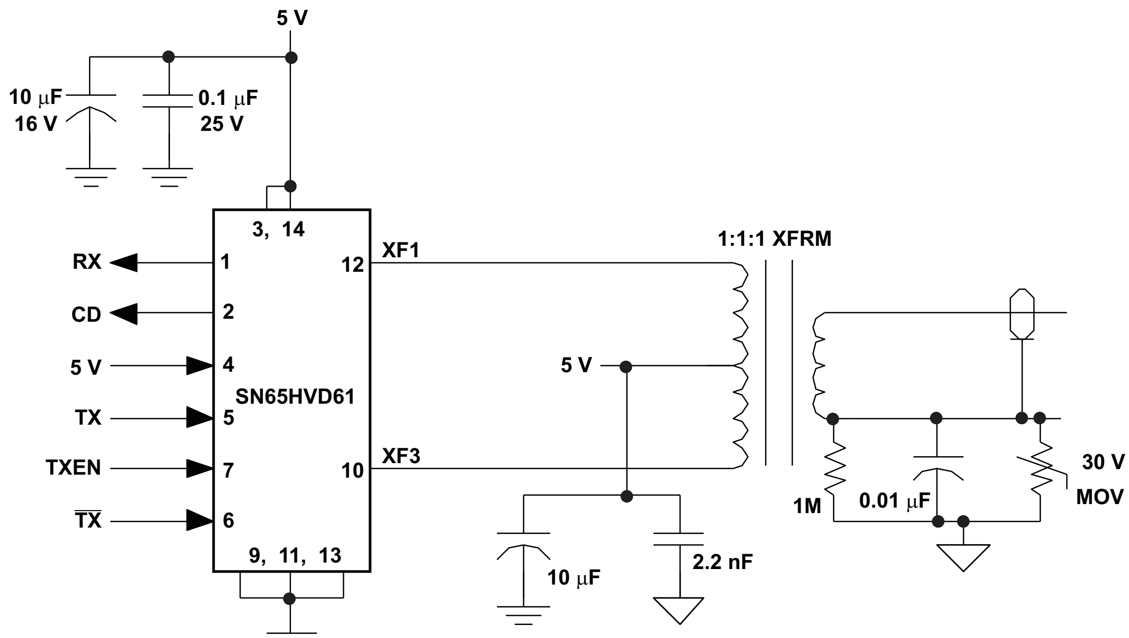

Figure 14. Schematic for Direct Replacement in Single-Channel Application

The 1:1:1 pulse transformer is described by the ControlNet specification, and may be available from Rockwell Automation. EPCOS (www.epcos.com) also provides a transformer suitable for ControlNet applications; this is series T4312 with ordering code B78417P8441A005.

The 30-V MOV acts to reduce transient surge voltages. Rockwell Automation in the past has suggested the Harris part number V30MLA1812TX1884 to help pass surge testing. Littelfuse (www.littelfuse.com) makes a family of multilayer transient voltage suppressors, which may have similar characteristics to the Harris part.

The 2.2 nF (2200 pF) capacitor shown in the circuit is optional, and is intended to improve electromagnetic compatibility performance at the systems level. This capacitor is connected across the transformer from the primary to the secondary, between V_{CC} on the chip side and chassis ground on the bus side. Since the isolation rating on the transformer is 500 Vac rms, the capacitor should have a voltage rating of at least 500 Vac.

3.3 Dual-Channel Application

3.3.1 Pin-to-Pin Assignment

In dual-channel (redundant) applications, two SN65HVD61 transceivers can be configured to function in place of one coax dual transceiver hybrid (Rockwell Automation part number 94180201). For some applications, the HVD61 devices may be used to directly replace the hybrid transceiver, without taking advantage of the additional features the HVD61 implements. In these applications, the table below shows the pin-to-pin equivalence between the SIP hybrid and the two SOIC HVD61 devices.

Table 3. SN65HVD61 Pin Assignments for Direct Replacement of a Dual-Channel Hybrid

HYBRID PIN		SN65HVD61 A PIN	SN65HVD61 B PIN		
1	XF3_A	10		XF3 (A)	Connections to transformer (A)
2	XF1_A	12		XF1 (A)	
3	TX_A	5		TX (A)	Complementary transmit inputs (A)
4	TXBAR_A	6		TXBAR (A)	
5	No pin				
6	RX_A	1		RX (A)	Receiver output (A)
7	V_{CC}	3, 14	3,14	VDD, VCC	5V supply
8	CD_A	2		CD (A)	Carrier Detect (A)
9	TXEN_A	7		TXEN (A)	Transmit Enable (A)
10	TXEN_B		7	TXEN (B)	Transmit Enable (B)
11	RX_B		1	RX (B)	Receiver output (B)
12	GND	9, 11, 13	9,11,13	DGND, CGND	Signal grounds
13	CD_B		2	CD (B)	Carrier Detect (B)
14	TXBAR_B		6	TXBAR(B)	Complementary transmit inputs (B)
15	TX_B		5	TX (B)	
16	XF1_B		12	XF1 (B)	Connections to transformer (B)
17	XF1_B		10	XF3 (B)	
		4	4	CHEN	Chip Enable – connect to Vcc
		8	8	SIG	Signal Strength – make no connection

Note that in these direct-replacement applications, all supply lines (VCC and VDD) should be tied to a single 5-V supply. Also, all ground pins (DGND and CGND pins) should be tied to the common signal ground.

3.3.2 External Components

For a dual-channel application, the same external protection and filtering components are suggested as for the single-channel application. For simplicity, replicate the circuit shown in Figure 14 for each channel. Figure 15 shows an example implementation of a dual-channel application using two HVD61 devices on a single single in-line package (SIP) board.

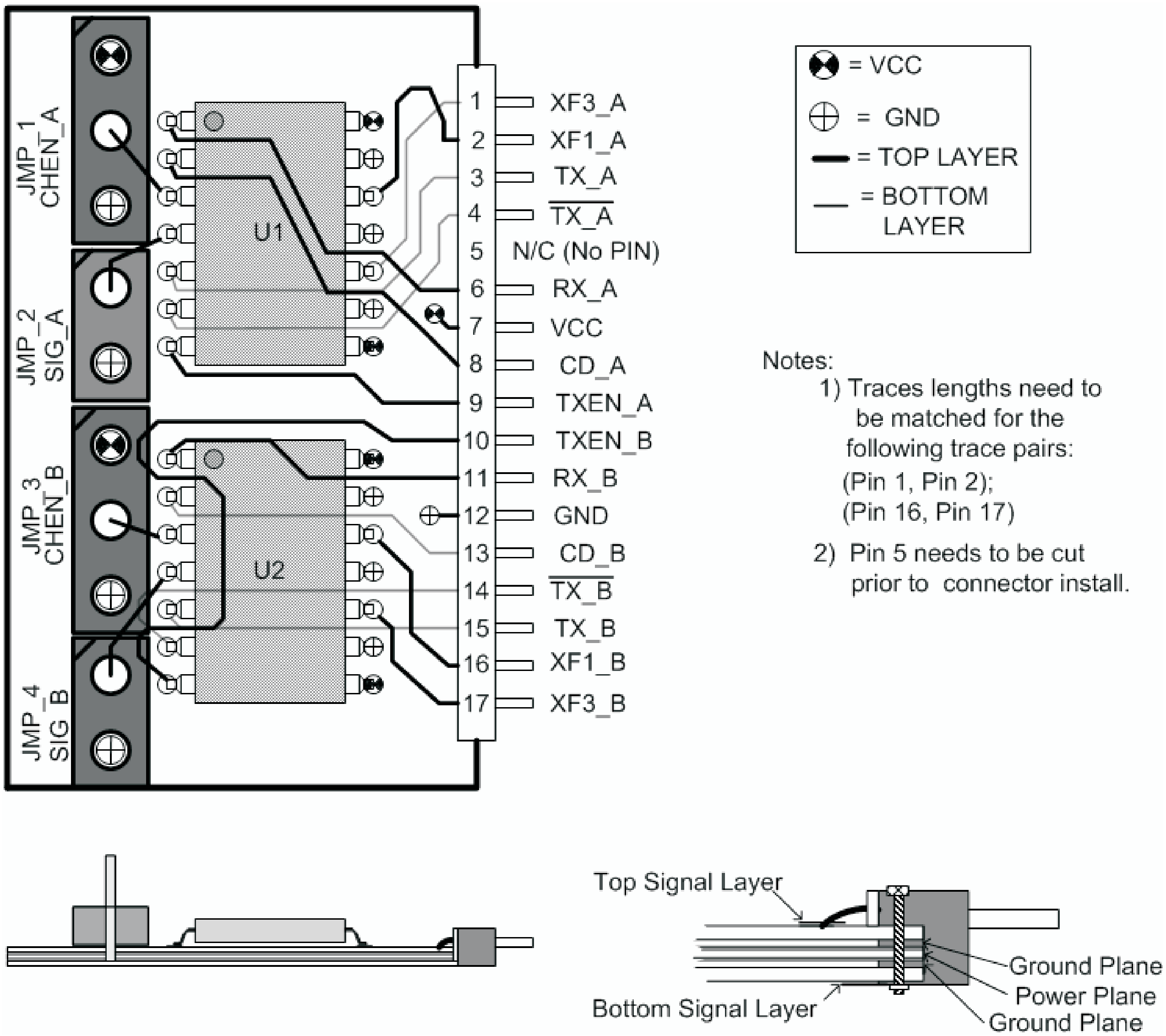

Figure 15. Dual-Channel SIP Hybrid SN65HVD61 Implementation

4 Next-Generation Design With the SN65HVD61

4.1 Improved Characteristics

4.1.1 1. Operating Temperature to 100°C

The HVD61 is characterized for operation over the temperature range of –40°C to 100°C. This gives system designers more latitude compared to previous implementations, which were typically limited to temperature ranges of 0°C to 85°C. As with all designs, proper care must be taken to ensure that the maximum temperature of any device does not exceed the rated temperature. This involves understanding not only the ambient temperature, but also the junction temperature rating and thermal design of the board.

For more information regarding thermal constraints, see the ABSOLUTE MAXIMUM RATINGS table, the ABSOLUTE MAXIMUM RATINGS table, and the THERMAL CHARACTERISTICS OF IC PACKAGES section in the SN65HVD61 data sheet. A discussion of thermal modeling and junction temperature calculations is given in the Texas Instruments Applications Note IC Package Thermal Metrics (TI literature number SPRA953).

4.1.2 Lower Power Consumption

The quiescent (transmitter off) supply current for hybrid implementations of the ControlNet transceiver is specified as typically about 50 mA, and can vary to a maximum of almost 75 mA. Under similar conditions with the chip disabled, the HVD61 supply current is specified as typically about 1.8 mA, with a maximum of 3 mA. This includes both the analog supply VCC and the digital supply VDD.

In dynamic operating conditions, the active supply current is much higher for both the hybrid-transceiver and the SN65HVD61 implementation. The load current is supplied through the center-tap of the transformer, so this is not included as part of the transceiver supply current. The rms supply current to the hybrid transceiver can typically be as high as 180 mA; the analog rms supply current to the SN65HVD61 is typically about 36 mA, and the digital supply less than 5 mA for a total of about 40 mA.

The load current on the bus is supplied by the 5 V on the bus transformer’s center-tap, independent of which type of transceiver is used. Assuming that the bus is correctly terminated with 37.5 Ω (75 Ω impedance at each end), and that the signaling levels meet the ControlNet requirements of ±4.1 V (8.2 V_{pp}), a nominal current of 109 mA occurs when the transmitter is active. The maximum level of ±4.75 V (9.5 V_{pp}) corresponds to a load current of 127 mA.

Table 4. Power Supply Requirements

Transceiver	VCC (5 V)	VDD (2.5 V, 3.3 V, or 5 V)	VCC (5 V) Transformer	Total Power Supply Current
Hybrid (single)	200 mA	Not applicable	130 mA	330 mA
SN65HVD61	65 mA	5 mA	130 mA	200 mA

4.1.3 ESD Protection

4.1.3.1 Chip-Level ESD Protection

Electrostatic discharges constitute a danger for all integrated circuits, including the SN65HVD61. Electrostatic charging can occur as a result of friction, such as when one walks on a carpet, causing the body to become charged. If a conducting object such as a piece of equipment connected to a ground line is touched, the body is discharged. The electrostatic energy stored as charge is injected into the object that is touched, and is converted primarily into heat. The power dissipation that arises in such cases can damage the electronic circuits.

Test circuits have been developed to test sensitivity to electrostatic discharges by simulating various scenarios. These test circuits are analyzed in more detail in the following paragraphs. These should provide the design engineer with insight into the protection circuits, and whether additional precautions are necessary.

Human-Body Model (HBM) – The HBM test was developed to simulate the action of a human body discharging accumulated static charge through a device to ground, and employs a series RC network consisting of a 100-pF capacitor and a 1500-Ω resistor. The SN65HVD61 has been tested and rated for HBM ESD conditions up to 16 kV on the bus pins, and up to 2 kV on all other pins.

Charged-Device Model (CDM) – The CDM test simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occur when there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube and hitting a metal surface. The CDM addresses the possibility that a charge may reside on a lead frame or package (e.g., from shipping) and discharge through a pin that subsequently is grounded, causing damage to sensitive devices in the path. The discharge current is limited only by the parasitic impedance and capacitance of the device. CDM testing consists of charging a package to a specified voltage, then discharging this voltage through the relevant package leads. At TI, the CDM testing is conducted using a field-induced CDM (FCDM) simulator. The HVD61 has been tested and rated for CDM ESD conditions up to 500 V on all pins.

Machine Model (MM) – The MM test simulates a machine discharging accumulated static charge through a device to ground. It comprises a series RC network of a 200-pF capacitor, and nominal series resistance of less than 1 Ω. The output waveform usually is described in terms of peak current and oscillating frequency for a given discharge voltage. The HVD61 has been tested and rated for MM ESD conditions up to 200 V on all pins.

4.1.3.2 Board-Level Protection

The ControlNet network is intended to operate reliably in harsh industrial environments, which often involve significant electromagnetic-transient events. Ater the HVD61 has been installed in a circuit board, the applicable levels of transient protection are very dependant on the surrounding components, board layout, etc. Test specifications such as the IEC-61000-4 series are used to provide a relative measure of system-level robustness to ESD, voltage surges, and other electromagnetic compatibility (EMC) issues.

End equipment with the SN65HVD61 has been tested to various levels of system-level IEC test standards. The requirements are summarized in Figure 16 and Table 5.

Table 5. EMC Standards

EMC STANDARD	DESCRIPTION OF TEST METHOD	LEVEL
IEC 61000-4-2	Electro Static Discharge (ESD) Immunity	6 kV Contact 8 kV Air-Gap
IEC 61000-4-3	Radiated Radio Frequency (RF) Immunity	10 V/m at 80 MHz to 2.7GHz
IEC 61000-4-4	Fast Transients / Burst Immunity	1 kV
IEC 61000-4-5	Surge Immunity	1 kV
IEC 61000-4-6	Conducted Radio Frequency (RF) Immunity	10V at 150 kHz to 80 MHz 1 kHz AM 80% modulation

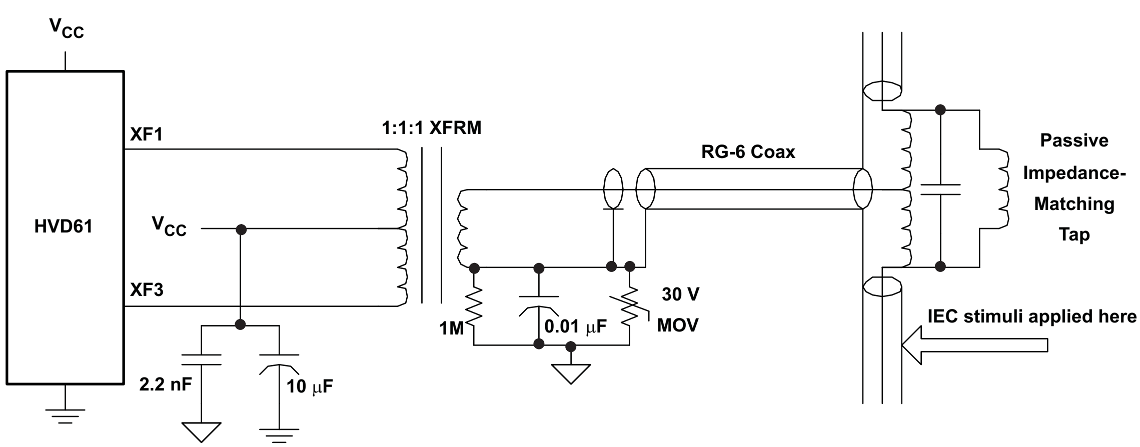

Figure 16. Simplified Test Set-up for EMC Standards

4.2 New Functions

4.2.1 Low-Voltage Interface to MAC

To maintain backward compatibility with previous transceiver implementations, the SN65HVD61 can be supplied by a single 5 V supply. However, it can also be supplied by split Logic/Bus supplies, to facilitate operation with MACs using digital supplies down to 2.5 V. The logic supply (VDD) can be any voltage between 2.375 V (5% below 2.5 V nominal) and 5.25 V (5% above 5 V nominal). The input logic thresholds for TX, TXBAR, TXEN and CHEN will automatically adjust to standard CMOS logic levels depending on the value of VDD. That is, logic low will be any voltage below 30% of VDD and logic high will be any voltage above 70% of VDD. This can eliminate the need for external level-shifters for the case of MACs with supplies below 5 V.

4.2.2 SIGNAL Function

The Signal Strength output (SIG) is a new function not available on previous implementations of the ControlNet transceiver. This output provides an analog voltage which is a single-ended version of the differential voltage across the XF1 and XF3 pins. The SIG function converts the differential voltage to single-ended, scales the value by 0.1, and offsets the results by 1.25 V. The resulting voltage is then a suitable representation of the input-bus signal strength, and may be used for network diagnostic functions, or system built-in tests (BIT). Figure 17 shows the transfer function from differential signal in (XF1,XF3) to SIG voltage out.

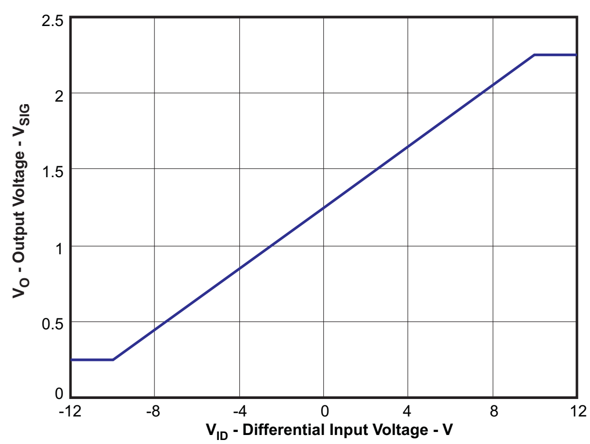

Figure 17. Nominal Transfer Function of the SN65HVD61 SIG Feature

[Figure 18](#) shows an oscilloscope trace with the differential signal (Ch.1, top trace) and the SIG voltage (Ch.2, bottom trace). Note that from the ControlNet bus through the transformer and differential inputs, there are dynamic effects that distort the higher-frequency content of the SIG output.

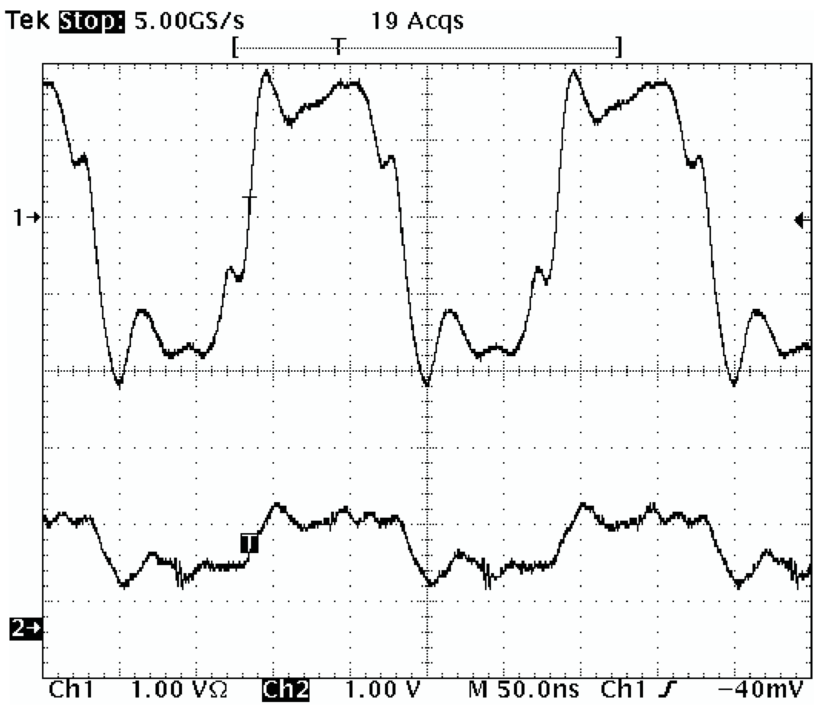

Figure 18. Differential Input (Ch.1) and SIG Output (Ch.2)

4.3 CHIP ENABLE Function

The SN65HVD61 implements a Chip Enable (CHEN) feature that was not available on previous ControlNet transceivers. When the CHEN pin is connected to logic high, the transceiver is fully enabled. When the CHEN pin is connected to a logic-low level or left disconnected, the transceiver functions are disabled. In the disabled state, the VCC and VDD power supply currents are very low, less than 3 mA total. This feature facilitates low power modes for end-equipment using the HVD61.

When the transceiver is re-enabled (rising edge on CHEN), all functions become fully operational in less than one microsecond.

Note that the CHEN function enables/disables all the functions of the HVD61, while TXEN enables/disables only the transmitter function.

5 More Information

For more information regarding the ControlNet protocol or Common Industrial Protocol (CIP) of which ControlNet is part, see the ODVA web site at www.odva.org.

5.1 Example Implementations

The two photographs below show two implementations of using the SN65HVD61 as a direct replacement for the hybrid transceiver. In the first photo, an engineering version is shown. The *surf board* can be quickly wired as shown (refer to Table 2 for pin assignments). These prototype boards are available from sources such as Capital Advanced Technologies (capitaladvanced.com). The specific board shown in this figure is Capital Advanced part number 9165.

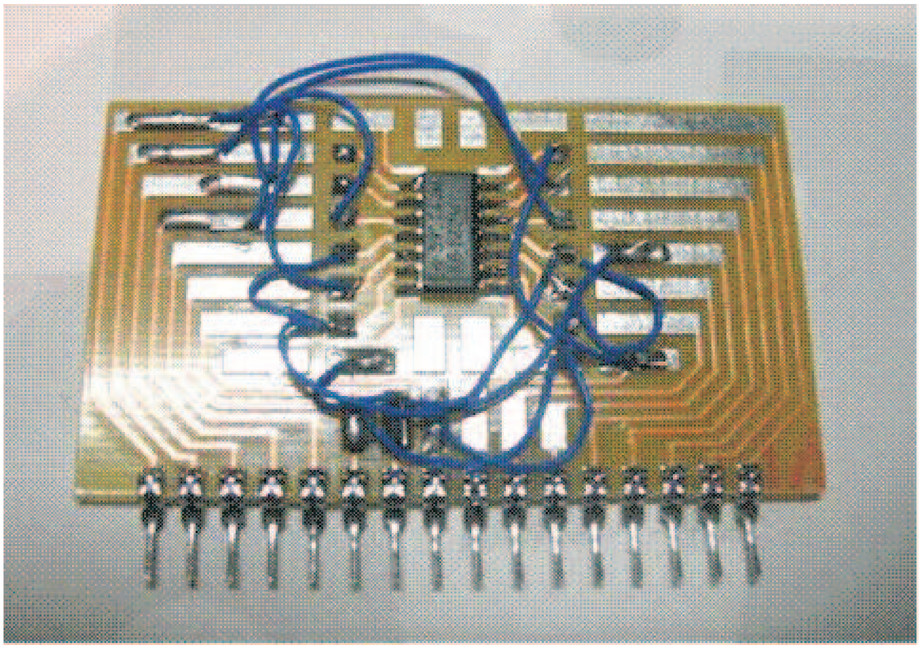

Figure 19. Engineering Prototype SN65HVD61-to-Hybrid Replacement

The second photograph shows an implementation using a small circuit board to carry the SN65HVD61 transceiver and a few other passive components to replace the hybrid SIP transceiver. Note that this instance is a single-channel application.

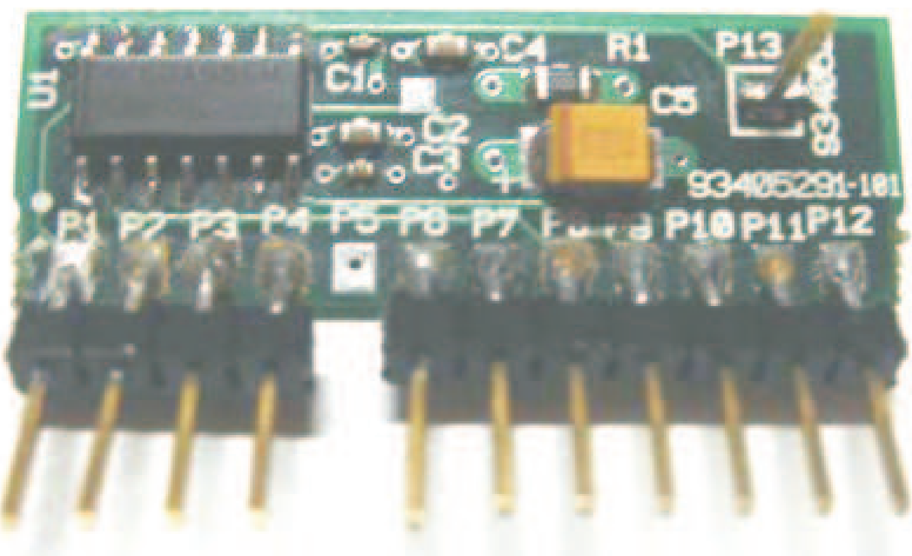

Figure 20. Example SN65HVD61-to-Hybrid Replacement Printed Circuit Board

6 Conclusion

The SN65HVD61 integrated ControlNet transceiver gives industrial network designers a new option when designing products. This transceiver works interchangeably with the older hybrid SIP implementation, but also offers many advantages in terms of new functions, lower power, and board space savings.

Texas Instruments looks forward to discussing your ControlNet or other industrial interface applications; contact your local Texas Instruments representative for samples or more information.

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