- Single-Chip and Single-Supply Interface for IBM PC/AT™ Serial Port
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.11 Standards
- Operates With 3.3-V or 5-V Supplies
- One Receiver Remains Active During Standby (Wake-up Mode)
- Designed to Operate at 128 kbit/s Over a 3-m Cable
- Low Standby Current . . . 5 μA Max
- ESD Protection on RS-232 Pins Meets or Exceeds 4 kV (HBM) and 1.5 kV (HBM) on All Pins Per MIL-STD-883, Method 3015
- External Capacitors . . . 0.1 μF
   (V<sub>CC</sub> = 3.3 V . . . Five External Capacitors)
   (V<sub>CC</sub> = 5 V . . . Four External Capacitors)
- Accepts 5-V Logic Input With 3.3-V Supply
- Applications
  - RS-232 Interface
  - Battery-Powered Systems, PDAs
  - Notebook, Laptop, and Palmtop PCs
  - External Modems and Hand-Held Terminals
- Packaged in Shrink Small-Outline Package

#### (TOP VIEW) $V_{DD}$ 28 ∏ C3+ C2+ [ GND 2 27 V<sub>CC</sub> **□** 3 26 C3-C2- $\Pi$ 25 VSS EN [ 5 24 ∏ C1– С1+ П 23 STBY 6 DIN1 22 DOUT1 21 DOUT2 DIN2 8 DIN3 [ 20 DOUT3 9 ROUT1 10 19 RIN1 ROUT2 □ RIN2 11 18 ROUT3 ∏ RIN3 12 17 16 RIN4 ROUT4 13 ROUT5 15 RIN5

DB PACKAGE<sup>†</sup>

† The DB package is only available in left-ended tape and reel (order part number SN75LV4737ADBR).

#### description

The SN75LV4737A<sup>‡</sup> consists of three line drivers, five line receivers, and a charge-pump circuit. It provides the electrical interface between an asynchronous communication controller and the serial-port connector, and meets the requirements of TIA/EIA-232-F. This combination of drivers and receivers matches those needed for the typical serial port used in an IBM PC/AT or compatibles. The charge pump and five small external capacitors allow operation from a single 3.3-V supply, and four capacitors allow operation from a 5-V supply.

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-high STBY input. The active-low  $\overline{EN}$  input is an enable for one receiver to implement a wake-up feature for the serial port. All the logic inputs can accept signals from controllers operating from a 5-V supply, even though the SN75LV4737A is operating from 3.3 V.

The SN75LV4737A is characterized for operation over the temperature range of 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

‡ Patent-pending design

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#### **Function Tables**

#### **EACH DRIVER**

INP	UTS	OUTPUT
DIN	STBY	DOUT
Х	Н	Z
L	L	Н
Н	L	L
Open	L	L

H = high level, L = low level, X = irrelevant, Z = high impedance

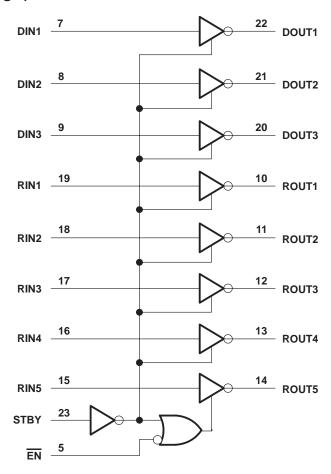
#### **EACH RECEIVER**

		INPUTS		OUTPUTS				
STBY	EN	RIN5	RIN1-RIN4	ROUT5	ROUT1-ROUT4			
Н	Н	Х	Х	Z	Z			
Н	L	Н	X	L	Z			
Н	L	L	X	н	Z			
L	Χ	L	L	Н	Н			
L	Χ	Н	Н	L	L			

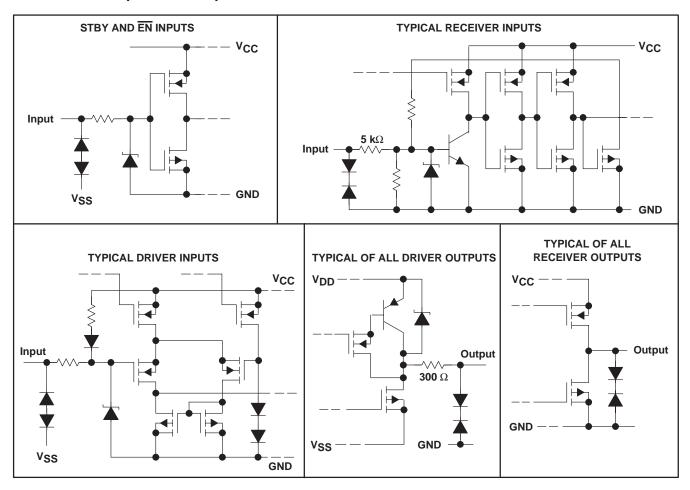
H = high level, L = low level, X = irrelevant, Z = high impedance



## logic diagram (positive logic)



#### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub>	
Positive output supply voltage, V <sub>DD</sub> (see Note 1)	
Negative output supply voltage, V <sub>SS</sub>	–15 V
Input voltage range, V <sub>I</sub> : Driver	–3 V to 7 V
Receiver	
Output voltage range, V <sub>O</sub> : Driver	$\dots$ V <sub>SS</sub> – 0.3 V to V <sub>DD</sub> + 0.3 V
Receiver	–0.3 V to 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2)	62°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to network GND.
  - 2. The package thermal impedance is calculated in accordance with JESD 51.



### SN75LV4737A 3.3-V/5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER

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### recommended operating conditions

				MIN	NOM	MAX	UNIT
Vac	Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
Vcc	Supply voltage		V <sub>CC</sub> = 5 V	4.5	5	5.5	V
		DIN, EN, STBY	V <sub>CC</sub> = 3.3 V	2			
VIH	Driver high-level input voltage	DIN	V 5 V	2			V
		EN, STBY	V <sub>CC</sub> = 5 V	2.5			
VIL	Driver low-level input voltage	DIN, EN, STBY				0.8	V
٧ <sub>I</sub>	Receiver input voltage					±30	V
	External capacitor	3.3-V operation (C1, C3) 5-V operation (C1, C3) See Note 3 and Figur	0.1			μF	
T <sub>A</sub>	Operating free-air temperature			0		70	°C

NOTE 3: C2 is needed only for 3.3-V operation.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 6 and 7) (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	V <sub>CC</sub> = 3.3 V			V <sub>CC</sub> = 5 V			UNIT
	PARAMETER	1531	MIN	TYP†	MAX	MIN	TYP <sup>†</sup>	MAX	ONIT	
$V_{DD}$	Positive supply voltage	No load			10		7	8.7		V
Vss	Negative supply voltage	No load			-9.5	-7		-8	-6	V
II	Input current (EN, STBY)	See Notes 4 a			±2			±2	μΑ	
	Supply current		STBY at GND, EN at V <sub>CC</sub> or GND	8.4	10	18	10	12	20.7	mA
ICC	Supply current (standby mode) (see Note 4)	No load, Inputs open	EN, STBY at V <sub>CC</sub>			5			5	^
	Supply current (wake-up mode) (see Note 5)		EN at GND, STBY at V <sub>CC</sub>			10			10	μΑ

† All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ . NOTES: 4. When standby mode is not used, STBY input must be taken low.



<sup>5.</sup> When wake-up mode is not used,  $\overline{\mathsf{EN}}$  input must be taken high.

#### **DRIVER SECTION**

# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITION	MIN	TYP†	MAX	UNIT	
Vон	High-level output voltage	$R_L = 3 \text{ k}\Omega$		5.5	7		V
VOL	Low-level output voltage	$R_L = 3 \text{ k}\Omega$			-6	-5	V
lн	High-level input current	VI = VCC				1	μΑ
I <sub>I</sub> L	Low-level input current	V <sub>I</sub> at GND				-10	μΑ
loo	Short-circuit output current (see Note 6)	V <sub>CC</sub> = 3.6 V,	VO = 0 V		±1 <i>E</i>	±40	mA
los	Short-circuit output current (see Note 6)	V <sub>CC</sub> = 5.5 V,	VO = 0 V		±15	±40	ША
r <sub>O</sub>	Output resistance	$V_{CC} = V_{DD} = V_{SS} = 0 V$	V <sub>O</sub> = ±2 V	300	500		Ω

 $<sup>^{\</sup>dagger}$  All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST COI	NDITIONS	MIN	TYP	MAX	UNIT
	Propagation delay time, low- to high-level output		V <sub>CC</sub> = 3.3 V	100	500	850	ns
tPLH	Propagation delay time, low- to high-level output	$C_L = 50 \text{ pF},$	V <sub>CC</sub> = 5 V		500	850	115
<b></b>	Propagation delay time, high- to low-level output	$R_L$ = 3 kΩ to 7 kΩ, See Figure 1	V <sub>CC</sub> = 3.3 V	100	500	850	20
tPHL	Propagation delay time, high- to low-level output		V <sub>CC</sub> = 5 V	100	500	850	ns
<sup>t</sup> PZH	Output enable time to high level	C <sub>L</sub> = 50 pF,	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$		1	5	ms
tPZL	Output enable time to low level	See Figure 2	_		3	7	ms
4	Output disable time from high level		V <sub>CC</sub> = 3.3 V		0.9	3	
tPHZ	Output disable time nom nign level	C <sub>L</sub> = 50 pF,	V <sub>CC</sub> = 5 V		0.6	3	μs
4	Output disable time from law lavel	$R_L$ = 3 kΩ to 7 kΩ, See Figure 2	V <sub>CC</sub> = 3.3 V		0.5	3	
tPLZ	Output disable time from low level	J	V <sub>CC</sub> = 5 V		0.3	3	μs
SR	Slew rate	C <sub>L</sub> = 50 pF, See Figure 1	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$	4		30	V/μs
SR(tr)	Slew rate, transition region	C <sub>L</sub> = 2500 pF, See Figure 3	$R_L = 3 \text{ k}\Omega \text{ to } 7 \text{ k}\Omega,$	3		30	V/μs

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .



NOTE 6: Short-circuit durations should be controlled to prevent exceeding the device absolute maximum power dissipation ratings, and not more than one output should be shorted at a time.

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#### **RECEIVER SECTION**

# electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

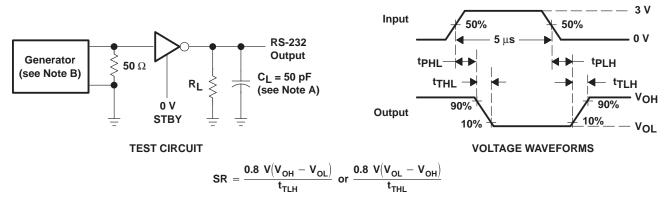
	PARAMETER	TEST COND	MIN	TYP	MAX	UNIT	
\/011	High-level output voltage	I <sub>OH</sub> = -2 mA	V <sub>CC</sub> = 3.3 V	2.4	3		V
VOH	riigh-level output voltage	10H = -2 IIIA	V <sub>CC</sub> = 5 V	3.5	5		V
VOL	Low-level output voltage	$I_{OL} = 2 \text{ mA}$		0.2	0.4	V	
V <sub>IT+</sub>	Positive-going input threshold voltage				2.2	2.6	V
V <sub>IT</sub> _	Negative-going input threshold voltage			0.6	1		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5	1.2	1.8	V
rį	Input resistance	$V_{ } = \pm 3 \text{ V to } \pm 25 \text{ V}$		3	5	7	kΩ

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$  or  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, CL = 50 pF, RL = 3 k $\Omega$ to GND

	PARAMETER	TEST	٧c	V <sub>CC</sub> = 3.3 V			CC = 5 V	'	UNIT
	PARAINETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output		10	70	200	10	70	200	ns
tPHL	Propagation delay time, high- to low-level output		10	60	200	10	55	200	ns
<sup>t</sup> PLH	Propagation delay time, low- to high-level output (wake-up mode)	See Figure 4		40	200		40	200	μs
tPHL	Propagation delay time, high- to low-level output (wake-up mode)			90	500		70	500	ns
<sup>t</sup> PZH	Output enable time to high level			3	10		1.2	10	μs
tPZL	Output enable time to low level	See Figure 5		100	250		60	250	ns
t <sub>PHZ</sub>	Output disable time from high level	See Figure 5	100	200	600	100	150	600	ns
tPLZ	Output disable time from low level			130	250		60	250	ns

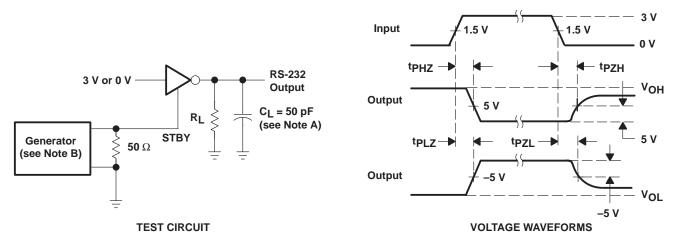
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \le 10$  ns,  $t_f \le 10$  ns.

Figure 1. Driver Propagation Delay Times and Slew Rate (5-μs Input)

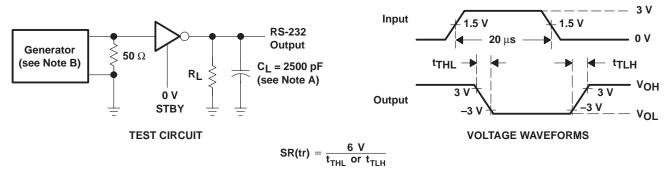


NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_O = 50~\Omega$ , 50% duty cycle,  $t_\Gamma \le 10~\text{ns}$ .

Figure 2. Driver Enable and Disable Test Times

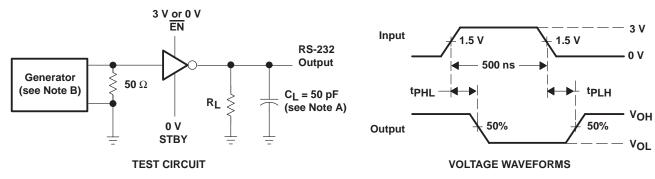
#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. The pulse generator has the following characteristics:  $Z_{O} = 50 \Omega$ , 50% duty cycle,  $t_{r} \le 10$  ns,  $t_{f} \le 10$  ns.

Figure 3. Driver Transition Times and Slew Rate (20-µs Input)

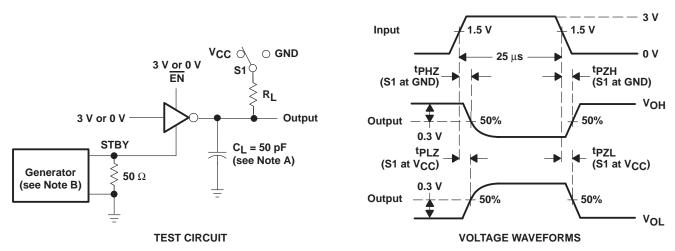


NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_O$  = 50  $\Omega$ , 50% duty cycle,  $t_\Gamma \le$  10 ns,  $t_f \le$  10 ns.

Figure 4. Receiver Propagation Delay Times

#### PARAMETER MEASUREMENT INFORMATION



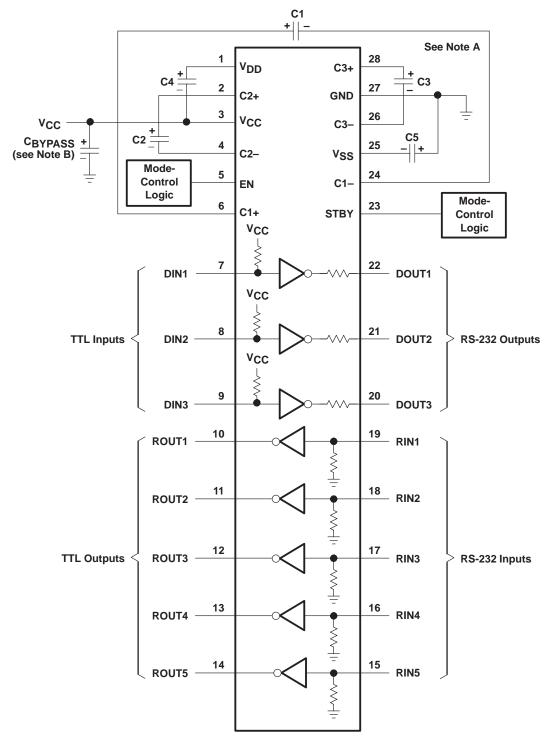
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_O = 50~\Omega$ , 50% duty cycle,  $t_\Gamma \le 10~ns$ ,  $t_f \le 10~ns$ .

Figure 5. Receiver Enable and Disable Times



#### **APPLICATION INFORMATION**

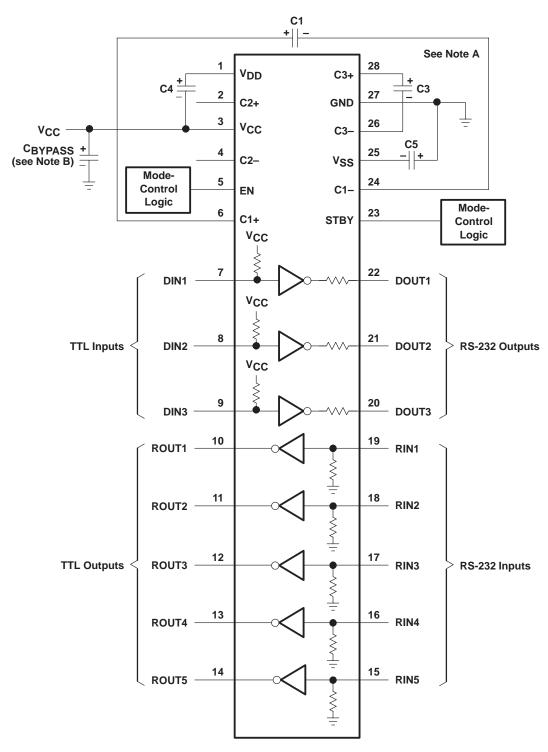


NOTES: A.  $C1 = C2 = C3 = C4 = C5 = C_{BYPASS} = 0.1 \,\mu F$  B.  $C_{BYPASS}$  is used as a decoupling capacitor.

Figure 6. Typical 3.3-V Operating Circuit



#### **APPLICATION INFORMATION**



NOTES: A. C2 is not used. C1 = C3 = C4 = C5 = CBYPASS = 0.1  $\mu F$ 

B.  $C_{\mbox{\footnotesize{BYPASS}}}$  is used as a decoupling capacitor.

Figure 7. Typical 5-V Operating Circuit



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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/		
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN75LV4737ADB	Active	Production	SSOP (DB)   28	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADB.A	Active	Production	SSOP (DB)   28	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADBR	Active	Production	SSOP (DB)   28	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A
SN75LV4737ADBR.A	Active	Production	SSOP (DB)   28	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LV4737A

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

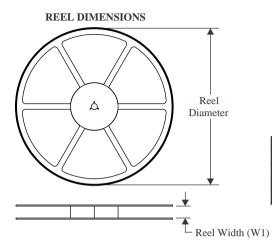
<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

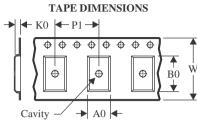
<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

## **PACKAGE MATERIALS INFORMATION**

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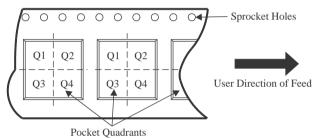
#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

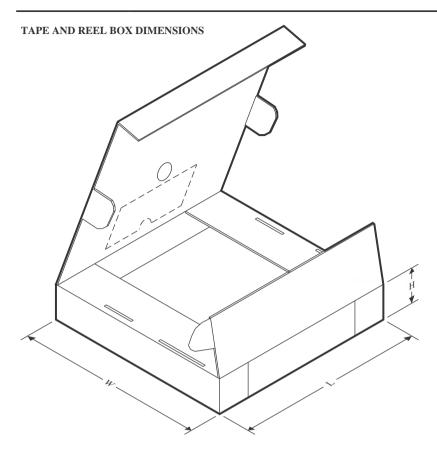


#### \*All dimensions are nominal

	Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ĺ	SN75LV4737ADBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

## **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LV4737ADBR	SSOP	DB	28	2000	353.0	353.0	32.0

## **PACKAGE MATERIALS INFORMATION**

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#### **TUBE**

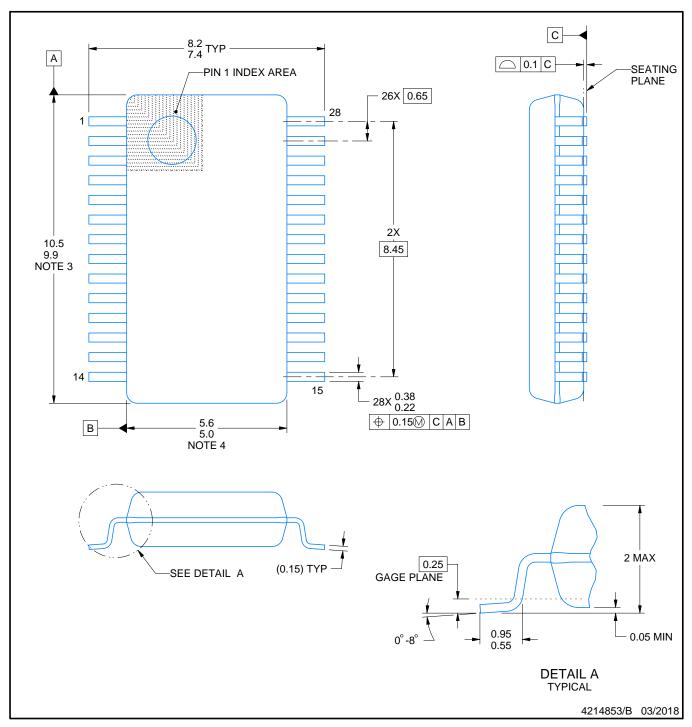


#### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LV4737ADB	DB	SSOP	28	50	530	10.5	4000	4.1
SN75LV4737ADB.A	DB	SSOP	28	50	530	10.5	4000	4.1



SMALL OUTLINE PACKAGE



#### NOTES:

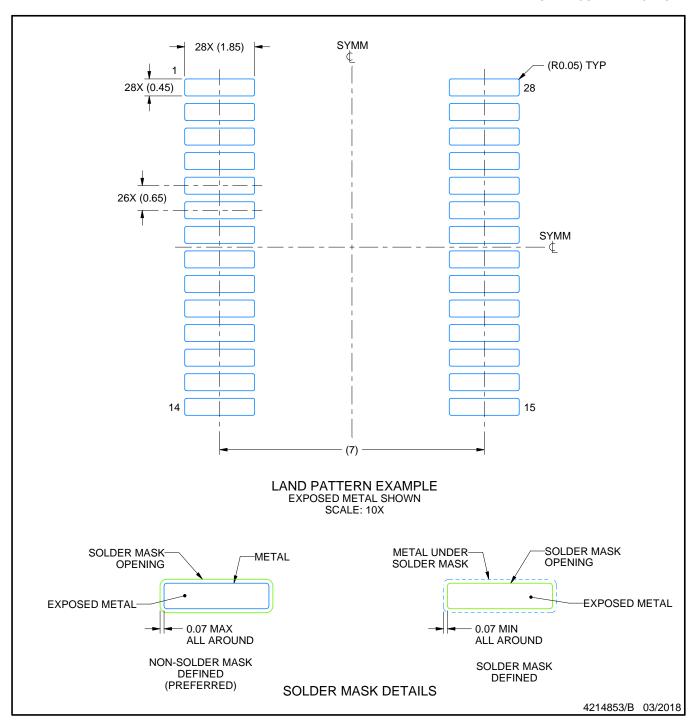
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.



SMALL OUTLINE PACKAGE



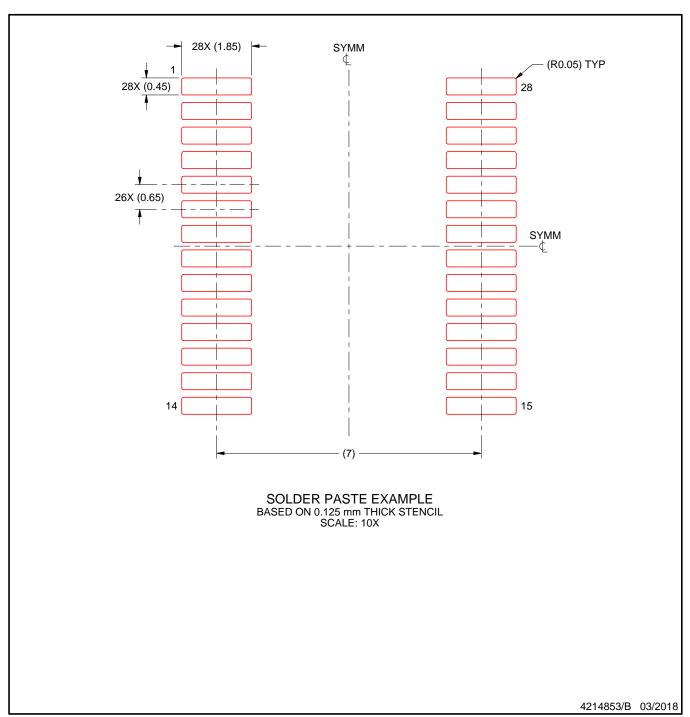
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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