2004/05
POWER SUPPLY DESIGN SEMINAR

TEXAS INSTRUMENTS

TABLE of CONTENTS

TEXAS INSTRUMENTS

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Topic 1

Safety Considerations in Power Supply Design

Texas Instruments

Safety Considerations in Power Supply Design

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ABSTRACT

Increasingly, the responsibilities of a power supply designer extend beyond merely meeting a functional specification, with designing to meet safety standards an important collateral task. Since all commercial and home-use supplies must eventually be certified as to safety, knowledge of the requirements should be a part of every designer's repertoire. This simplified overview has been prepared with the collaboration of Underwriters Laboratories, Inc. to provide a basic introduction to the issues and design solutions implicit in assuring the safety for both the user and service personnel of your power supply products, as well as easing the certification process.

I. INTRODUCTION

It should come as no surprise that safety is an important issue in the design of any electrical equipment which is liable to come into contact with a human operator or servicing individual. And this issue should be even more obvious when the equipment is designed to operate from a source of power which could experience or deliver voltage levels that could be hazardous to the human body. Recognizing this, a large collection of design standards and certification processes have been developed to define the requirements for insuring the safety of power supplies. A thorough treatment of this information takes much more space and time than available within the context of this seminar program – it is a subject more commonly taught with the dedication of one to two full days of presentation – however it is hoped that the brief overview provided herein will be useful in describing the basics both for designers who may have in-house resources with more detailed expertise, or who plan to follow up with attendance at a more in-depth program as those presented by Underwriters Laboratories, Inc.

Note that UL60950-1 (including Annexes P and Q) was used as the source for all numbers quoted here but many of the conditions and contingencies have been excluded in the interests of simplicity. Reference to the complete and latest revision of the appropriate standard should be made for any and all design decisions.

II. PRINCIPLES OF SAFETY

While one would expect that a safety standard for power supplies would be dominated by consideration of electrical hazards, this is not the only aspect of power supply design affected. A more complete listing of safety issues could include the following:

- **Electric Shock:** This is the shock hazard resulting from the passage of electric current through the human body. The physiological effects can range from perception or a startle involuntary movement, all the way to ventricular fibrillation or, ultimately, death.
- **Energy Hazards:** Even at voltages too low to produce a shock, burns can be caused when metallic objects such as tools, jewelry, etc. get very hot or melt and splash when they bridge sources with high VA potential (typically 240 VA or more).
- **Fire:** Fire is normally considered as a secondary effect from overload, abnormal operating conditions, or fault in some system component. However induced, it should not spread to adjacent components or equipment.
- **Heat Related Hazards:** High temperatures on accessible surfaces or components under normal operating conditions.
- **Mechanical:** Injury or damage resulting from contact with sharp edges or corners, moving parts, or physical instability.

While not usually associated with power supplies, other hazards that might need consideration could include the effects of radiation, chemicals, or hazardous vapors.

There are at least two types of persons whose safety needs must be considered: users (or operators) of the equipment, and service personnel. Users are not expected to identify hazards, and must not be allowed contact with hazardous parts. This is normally accomplished through the use of such means as enclosures or other protective shielding. Service personnel, on the other hand, are assumed to have access to all parts of the system and for their safety, the requirement is to identify the hazardous components or areas and to ensure against inadvertent contact with a hazardous surface, or bridging a tool between parts with high energy levels while working in another part of the equipment.

In addition to the types of personnel coming into contact with the equipment, there is an additional consideration as to the end use for a power supply. Power supplies can typically be divided into two categories:

- whether the supply is to be sold as a stand-alone item, or
- as a component to be installed into a specific system or equipment.

In either case, however, it is the end use conditions that apply and it is the end use standards that must be considered with respect to safety.

In additional principle of safety is that designers must consider not only normal operating conditions, but also likely faults, foreseeable misuse, external influences and environments, and overvoltages that might occur on input or output lines.

III. Safety Standards for Power Supplies

Safety standards, like most standards affecting electrical equipment, were originally very specialized and unique to a given country. The driving force for a unified standard was primarily the information technology industry whose efforts led to the first international standard for safety, IEC950, prepared by the International Electrotechnical Commission (IEC). With the release in the late 1980s of UL1950, UL expanded the scope of IEC950 to include electrical business equipment along with ITE, but this standard excluded telecommunication equipment. In the meantime, however, a working group of the IEC (TC-74) had generated a harmonized standard, IEC60950 (third edition), to cover products from all three industries and, upon its release in 1999, it was quickly adopted by most countries and is today the primary standard for safety for most, but certainly not all, users of power supplies. In addition to IEC, designations of this standard can be found as EN (European Union), UL (United States), and CSA (Canada). In the USA, the plan is to withdraw approvals to all earlier standards by July, 2006. The US National Standard, as of this writing, is UL60950-1, first edition, published in November, 2003.

While UL60950-1 is the most widely applied standard for power supplies today, it is intended for use with information technology, business, and telecom equipment. Other standards exist for other industries, such as IEC 60065 for audio and video, IEC 60601 for medical, IEC 61010 for laboratory supplies, and others. Further efforts at harmonization are under way with a sub-committee of the IEC (SC22E) proposing a new standard, IEC 61204-7, which is intended for use with power supplies sold into multiple industries. This standard is currently under development.

The point to remember here is that safety standards, like most things high-tech, represent an evolving field. While UL 60950-1 has been used to prepare this subject, one of the first tasks in any new design activity should be to identify the standards, including recent revisions, which applies to the intended end use.

IV. Elements of a Power Supply

A block diagram for a typical power supply is shown in Fig. 1 where the blocks have been defined in a way to ease the consideration of safety implications. While this figure illustrates an AC-line powered unit which, of course, is clearly an application where hazardous voltage levels could be present or internally generated, a similar blocking of functions could be derived for other designs, i.e., battery chargers or dc-to-dc converters.

The task of certifying a design for safety is made easier by the identification and use of as many components which, in themselves, are already qualified to an appropriate IEC safety standard. Many such power supply components are available, including:

- Power cords and/or input terminal assemblies
- Protective devices (fuses, clamps, etc.)
- EMI filters
- Power switches
- Wiring, PWBs, chassis
- Isolators (optocouplers)
- Transformers
- Rectifier assemblies
- Output connectors or terminals
- Cooling devices
- And many others…

Components which are already certified as conforming to the applicable standards need be evaluated only individually as to their application within their ratings, and then indirectly as a part of the complete power supply or end use application. Non-qualified components may need additional testing to the appropriate standard at the component level. Since this can add a significant amount of time and cost in the qualification process, it is highly advantageous to pick components which have already achieved prior approval.

V. Considerations for Electrical Safety

The prevention of electric shock is clearly a major safety goal. The impact on a human body is defined by the flow of current which, in turn, is affected by the body's resistance. The accepted value for the body's resistance is approximately 2000 Ω at a voltage of 110 Vdc; however this value decreases with increasing voltage. Another factor that affects resistance is the amount of surface area of contact. This has been quantized by defining two classifications of skin contact as:

- Full contact, meaning full contact by hand which has a typical area of about 8000 mm^2, but is simulated by a metal contact surface of 20 cm by 10 cm.

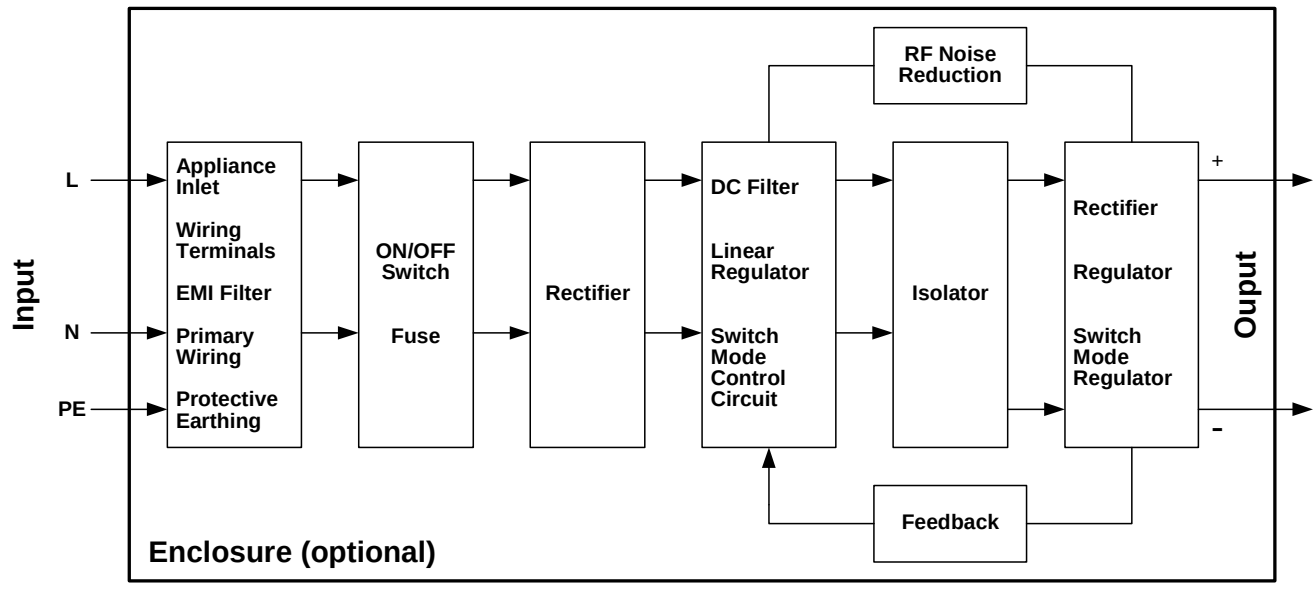

Fig. 1. The elements of a typical power supply.

- Limited contact is described as contact by finger tip and simulated by a metal contact surface of 10 mm^2. A standardized "finger probe" is defined to test for contact in tight regions or through enclosure openings.

In any case, it is current that affects the body and the effects have been categorized according to the table of threshold values in Table 1.

TABLE 1. THRESHOLD VALUES

Current (mA)	Effect
0.0 to 0.5	Perception, minimal reaction
0.5 to 3.5	Startle reaction, but ability to tolerate
3.5 to 10	Muscles contract, inability to let go
10 to 50	Fibrillation, cell damage

The acceptable limit for current is 2.0 mA dc, 0.7 mA pk ac and 0.5 mArms at frequencies up to 60 Hz. High-frequency current is less harmful to the human body and the permitted current is calculated by multiplying the 50/60 Hz threshold by the frequency in kHz, but with a maximum of 70 mA at all frequencies above 100 kHz. However, these limits can still cause burns if one touches a sharp edge or corner, as current density may be high.

Since it is the circuit voltage that drives this current, UL60950-1 categorizes circuits within a power supply as either hazardous or safe according to the maximum voltage or the maximum current possible at all points within the circuit, during both normal operating conditions and under any single fault. Within this criterion, there are three classifications of safe circuits

- **Limited Current Circuits (LCC)** where the maximum available current cannot exceed 2.0 mA dc, 0.7 mA peak ac, or 0.5 mA rms under both normal and single-fault conditions. There are also limits on allowable capacitance.
- **Safety Extra Low Voltage (SELV)** circuits where voltage levels cannot exceed 42.4 V pk ac or 60 Vdc, under both normal and single-fault conditions.
- **Telecommunication Network Voltage (TNV)** voltages may exceed SELV limits but are constrained by either accessibility or duration. The normal operating voltage can be up to 71 V peak ac or 120 V dc where the accessible contact area is limited to that of a connector pin. The voltages under a single fault can be higher for a short duration but must return to normal limits within 200 ms. Higher transient levels (up to 1500 V, but of short duration) are possible from the public switching telecom network.

Note that although all three of the above designations are considered as safe, only SELV and LCC circuits allow the operator unrestricted access to bare circuit components.

Classifications for circuits which are considered as unsafe and which must be protected against operator contact include:

- **Hazardous Voltage** circuits, where voltages above SELV limits can appear on bare components, or which contain components without adequate insulation from a potential high voltage source.
- **Extra Low Voltage (ELV)** circuits, which defines a circuit that meets SELV voltage limits under normal operating conditions but is not safe with a single fault.

Two other circuit classifications are defined by their location within a power supply's architecture:

- **Primary circuits**, where there is a direct connection to the ac mains voltage and clearly have the potential to reach hazardous voltage levels, and
- **Secondary circuits**, which have no direct connection to the primary circuits but may experience hazardous voltage levels.

VI. PROTECTION WITH INSULATION

UL60950-1 defines five categories of insulation.

A. Types of Insulation

- **Functional insulation** is that which is only necessary for circuit operation. It is assumed to provide no safety protection.
- **Basic insulation** provides basic protection against electric shock with a single level; however this category does not have a minimum thickness specification for solid insulation and is assumed to be subject to pinholes. Safety is provided by a second level of protection such as Supplementary insulation or protective earthing.
- **Supplementary insulation** is normally used in conjunction with Basic insulation to provide a second level of protection in the event that the Basic level fails. A single layer of insulating material must have a minimum thickness of 0.4 mm to be considered Supplementary insulation.
- **Double insulation** is a two-level system, usually consisting of Basic insulation plus Supplementary insulation.
- **Reinforced insulation** is a single-insulation system equivalent to Double insulation. It also requires a minimum thickness of 0.4 mm for use in a single layer.

Electric circuits rely upon insulation for operator protection, but designing for safety requires the premise that anything can fail. Therefore safety standards demand a redundant system with at least two levels of protection under the assumption that any single level may experience a failure but the chance of two simultaneous failures in the same spot is so improbable as to represent an acceptable risk. It should be noted that while two random failures need not be considered, the possibility of a second failure as a consequence of a first failure is something that the designer must evaluate if the two together would result in a total breakdown.

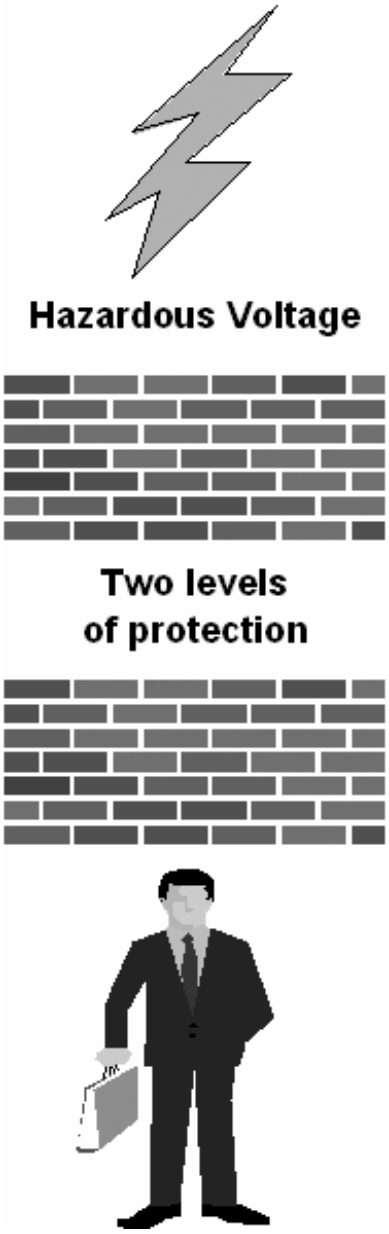

Fig. 2. Safety requires a Double barrier for redundant protection.

The general requirements are that a single level of insulation is acceptable if the circuit is not accessible, but wherever there are accessible components, they must be insulated from hazardous voltages by a Double-level system, and each level must meet the insulation specifications appropriate to the application. One qualification to this statement is that one level of protection could be protective earth provided by a conductive grounded enclosure.

B. Class Categories

Categories are used to define different classes of circuits and the type of insulation needed for each, as:

- **Class I Equipment**: Systems which use protective earthing (e.g., a grounded metal enclosure) as one level of protection and thus require only Basic insulation between the enclosure and any part at hazardous voltage
- **Class II Equipment**: The use of Double or Reinforced insulation to eliminate the need for a grounded metal enclosure as well as a grounded power plug.
- **Class III Equipment**: Powered from a SELV source and with no potential for generation of hazardous voltages internally, and therefore requiring only Functional insulation.

The process for defining insulation requirements starts with identifying each circuit block within the system according to the categories described above: LCC, SELV, TNV, ELV, or Hazardous. Then, with this knowledge, the appropriate insulation type and number of levels can be defined for use between blocks and between internal components and the user. A guide to insulation planning for a simple power supply example is shown in Fig. 3, which illustrates that there must always be two levels of protection between a hazardous voltage (on the left) and components accessible to the user (on the right).

For example, the path through a floating ELV circuit must have two levels, and at least one of those must be between the ELV and the user as an ELV could become unsafe with a single fault. However, if the ELV has grounded protection (providing one level), then only one additional level is needed. Similarly, external metal, (typically heatsinks or the power supply's enclosure), must isolate the user from the hazardous voltage with two levels of protection, unless one level is provided by grounding the metal.

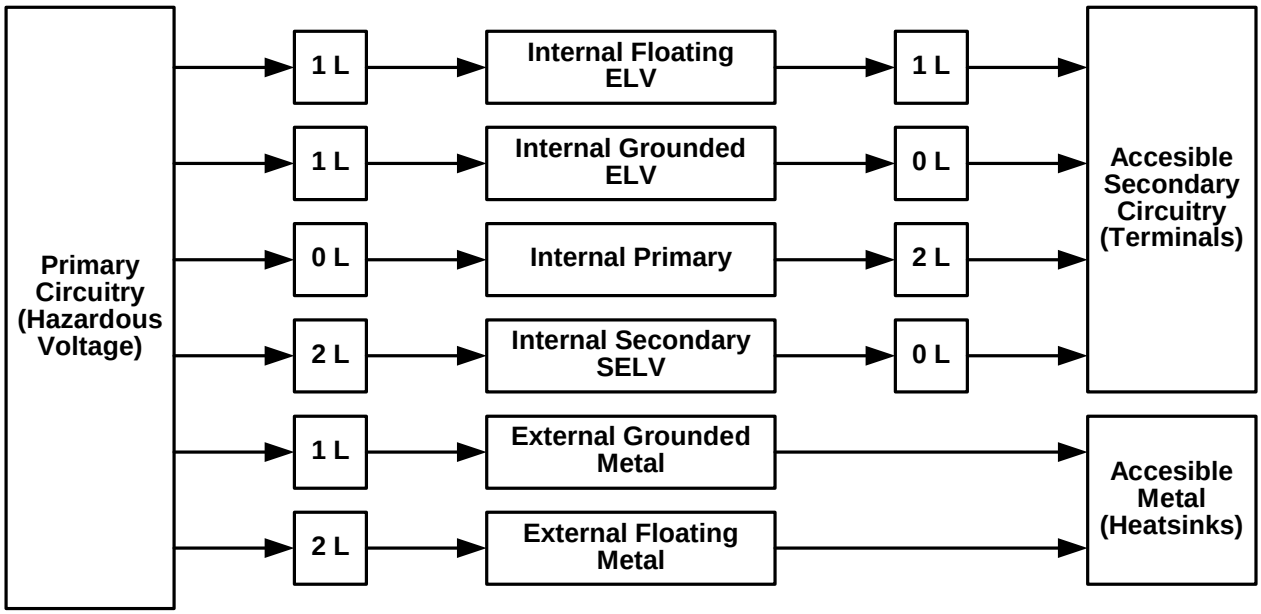

Fig. 3. Insulation coordination for a typical line-powered supply.

VII. WORKING VOLTAGE

With the insulation levels defined, specific requirements for the insulating medium must be considered. This medium can be either a solid material (such as plastic molding); or air (as in the space between components), and the requirements for both are affected by the voltage stress across the medium. Typically, a power supply is evaluated to determine the highest voltage levels possible at all points in the circuitry and under all operating conditions. The highest measured voltage between any two points then defines the **working voltage** for those two points. The working voltage between a primary circuit and a secondary circuit, or between the primary and ground, is taken as the upper limit of the rated voltage range for the supply.

An example is illustrated in Fig. 4 showing the schematic for a simple off-line power supply in which protective isolation is provided in both the transformer and the optocoupler. With all points on the primary referenced to either the line or the neutral power connections, hazardous voltage levels with respect to earth are assumed to be possible at any point on the primary side. The individual working voltages within the primary circuitry are evaluated as the maximum rated or measured voltage (whichever is higher) between any circuit element and either earth or any point on the secondary side of the transformer.

As shown in Fig. 4, the highest working voltages would normally be found on points labeled 0, 1, and 2 on the primary side of the transformer, and these points would then each be measured with respect to both earth and all secondary points labeled 3, 4, 5, and 6 with the condition that when one end of a secondary winding is used as a reference point, then the other end is to be connected to earth. These measurements - dc, rms, or peak - are evaluated to determine the highest value, which then establishes the minimum working voltage requirement for the protective insulation.

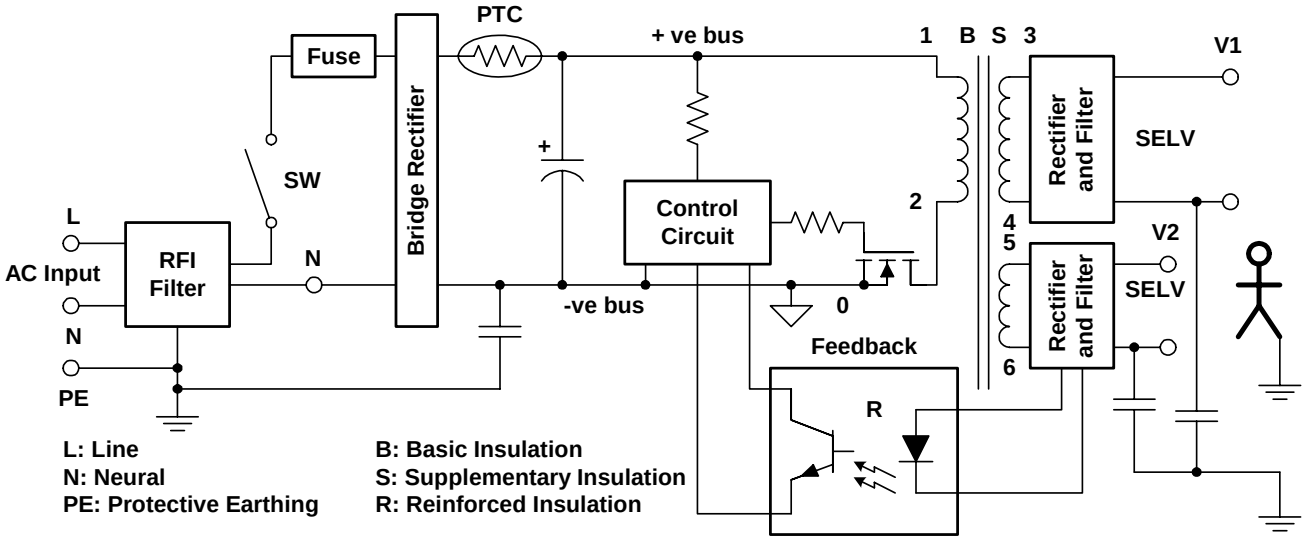

Fig. 4. Measurement points to determine the working voltage in the primary circuitry.

VIII. Insulating Materials

A. *Solid Insulation*

The choice and application of solid insulating material must consider, in addition to working voltage, the needs for electrical, thermal, and mechanical strength, as well as the operating environment. Only non-hygroscopic and flame resistant materials may be used. With particular respect to wiring insulation, it should be noted that some material compounds may contain plasticizers, intended to make them more flexible but with a side effect of increased flammability.

Semiconductor devices and other components that are molded in solid insulating material typically are independently qualified and inspected in the manufacturing process.

Solid insulation material in sheet form must also conform to the following thickness requirements:

- If a single sheet of insulation is provided, the minimum thickness is 0.4 mm.
- With two sheets together, there is no thickness requirement but each sheet must meet the required electric strength value.
- With three or more sheets, there is also no minimum thickness but every combination of two sheets must have adequate electric strength.
- There is no thickness requirement for Functional or Basic insulation.

B. *Air Insulation*

The use of air as an insulation medium introduces concerns both about the "quality" of the air and the spacing between electrically conducting components. The potential for conduction through air is affected by temperature, pressure, humidity, and pollution, with "pollution" being defined according to the operating environment by the following categories:

- Pollution Degree 1 – Components and assemblies which are sealed to exclude dust and moisture.
- Pollution Degree 2 – General office or home environment.
- Pollution Degree 3 – Equipment where the internal environment is subject to conductive pollution or possible moisture condensation.

The spacing distance between components that are required to withstand a given working voltage is specified in terms of Clearance and Creepage. A visual representation of the distinction between these terms, and their applicability to board-mounted components, is shown in Fig. 5

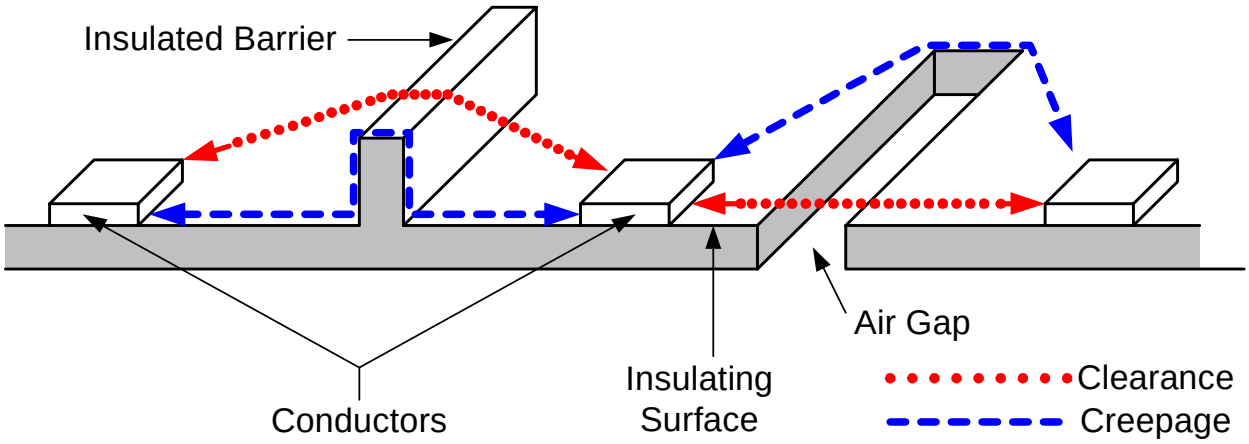

Fig. 5. Definitions of Creepage and Clearance.

IX. Clearance and Creepage

In the discussion that follows, the tables presented show quantitative values for spacing requirements, in millimeters, which are listed as a function of the voltage, material, and environment. An additional distinction is the category of insulation system of which these spacings are a part, i.e., Functional, Basic/Supplementary, or Reinforced. In other words, if the spacing between components is not needed for safety, the "F" column may be used; if only one level of safety insulation is needed because a second level is provided elsewhere, the "B/S" column is applicable; and for the equivalent of a complete 2-level safety insulation, the "R" column should be used.

A. Clearance

Clearance is defined as the shortest distance through air between two conductive parts. Breakdown along a Clearance path is a fast phenomenon where damage can be caused by a very short duration impulse. Therefore, it is the maximum peak voltage, including transients, that is used to determine the required Clearance spacing according to charts given in the standard. A sample of one of these is shown in Table 2 where the spacing in millimeters required for different levels of insulation is given as a function of working voltage. Additional variables of ac mains voltage and the quality of the air within the space are indicated in this illustration but are applied more quantitatively in additional charts given in the complete standard.

B. Creepage.

Creepage is defined as the shortest distance between two conductive parts along the surface of any insulating material common to both parts. While the path is in the air, it is heavily influenced by the surface condition of the insulating material. Breakdown of the Creepage distance is a slow phenomenon, determined by dc or rms voltage levels rather than peak events. Inadequate Creepage spacing may last for days, weeks, or months before it fails. A sample of a table of Creepage requirements is given as Table 3 where the spacings are given as a function of the steady-state working voltage with additional variables of insulation type, material composition, and content of the air.

Table 2. Partial Clearance Dimensions (mm) from UL60950-1, Section 2.10.3, Table 2H

Working Voltage		AC Mains < 150 V (Transient to 1500 V) Pollution levels 1 and 2			AC Mains < 300 V (Transient to 2500 V) (Pollution levels 1 and 2)		
Peak dc V	rms V	F	B/S	R	F	B/S	R
71	50	0.4	1.0	2.0	1.0	2.0	4.0
210	150	0.5	1.0	2.0	1.4	2.0	4.0
420	300	1.5	2.0	4.0	1.5	2.0	4.0
840	600	3.0	3.2	6.4	3.0	3.2	6.4

Table 3. Sample Creepage Dimensions (mm) from UL60950-1, Section 2.10.4, Table 2L

Working Voltage	Pollution Level 1 Material Group III			Pollution Level 2 Material Group III			Pollution Level 3 Material Group III		
dc or rms	F	B/S	R	F	B/S	R	F	B/S	R
< 50 V	0.4	0.7	1.4	1.2	1.2	2.4	1.9	1.9	3.8
< 150 V	0.6	0.9	1.8	1.6	1.6	3.2	2.5	2.5	5.0
< 300 V	1.6	1.9	3.8	3.2	3.2	6.4	5.0	5.0	10
< 600 V	3.2	3.2	5.0	6.3	6.3	12.6	10	10	20

Semiconductor components, particularly optocouplers, do not typically have Clearance or Creepage requirements. Clearance and Creepage distances do not exist if the component is completely filled with an insulating compound or molded in solid insulating material, and the component is independently qualified and inspected in the manufacturing process. Creepage, however, can become important with respect to the boards upon which these devices are mounted. This often dictates a requirement for spreading the package pins to maintain the required board spacing.

Fig. 6 illustrates some alternative pin configurations available with the popular 4N25 series of optocouplers. Note that with a surface mount configuration, the shape of the leads allows a board spacing close to 8 mm while with through-hole mounting, meeting an equivalent Creepage spacing would require either a wider lead bend or a slot cut in the PC board between the input and output rows of pins.

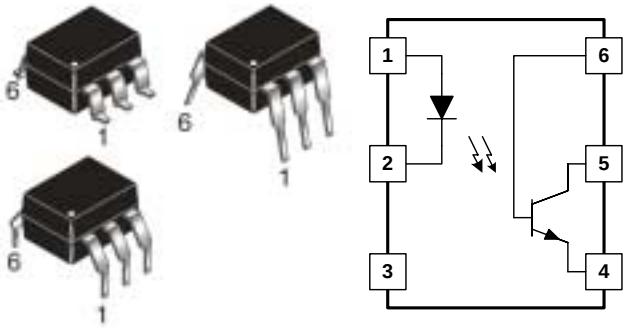

Fig. 6. Three pin configurations are offered with the popular 4N25 optocoupler to accommodate varying Creepage requirements for PCB mounting pads.

C. Transformer Construction

Fig. 7 shows a cross-section view of a typical isolating transformer where primary and secondary windings are wound on a common bobbin. Where hazardous voltages are involved, the insulation between primary and secondary must be at least Double or Reinforced with a minimum of two layers to allow for a single-element failure. Any enamel coating on the wire is not counted as an insulation level, although what is called "triple-insulated winding" wire meets Supplementary or Reinforced status depending upon the number of layers and their method of construction.

Unless the transformer is tested and qualified as a solid structure, completely filled with a solid insulating material, it is always assumed that there is a small amount of air present between the layers, even though there may be adhesive on one side of the insulating tape. In most transformer structures, Clearance and Creepage are the same and are shown in the figure as the sum of distances A and B. (The thickness of the tape is generally not taken into account.)

Transformer leads, as well as all other wires or cables must meet their own specifications and standards. Wire insulation must be PVC, neoprene, TFE, PTFE, or polyimide, or tested for flammability. Usually, insulating materials are required to meet one of the following classifications:

- V-1. Material is self-extinguishing upon removal of an external flame. Any flaming particles which drop do not ignite a cheese cloth fabric placed underneath.
- V-2. Material is self-extinguishing but cheese cloth may be charred or ignited from dropped flaming particles. V-2 material may only be used within an enclosure having no bottom openings.

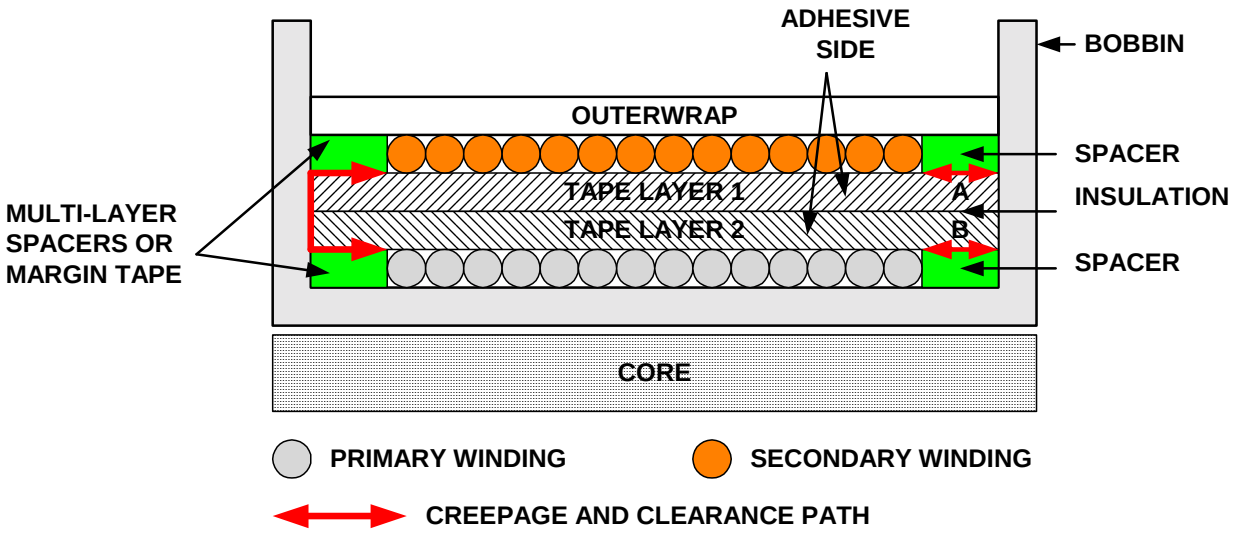

Fig. 7. Definitions insulation requirements for isolating transformers.

XI. Designing for Safety

Clearly, there are many decisions in the design process where a knowledge of safety requirements and the application of their principles can go a long way toward easing the time and cost of the safety certification process. Particularly if a failure in safety testing requires a redesign effort late in the program. Anticipating the testing which may be required and designing accordingly certainly pays off at the end of the day. While definitely not all-inclusive, a summary of some of the design considerations is given below:

A. Materials

Pick components and materials which have prior safety certification. With certified components, the safety engineer looks only to see that they have been applied correctly and physical testing is done only as a complete system. Without certified components, additional component-level testing or excessively conservative design techniques could be required. As an example, the Y capacitor in an input EMI noise filter would be accepted as a certified device, but otherwise might require two capacitors in series to allow a safety test to short one of them, plus the additional testing of the capacitors themselves.

B. Mechanical

The safety engineer looks for rigid construction with all components securely attached and no sharp edges or corners. All areas containing hazardous voltages have been protected from access by the user, including through any openings in the enclosure. Openings in the enclosure are examined to ensure that there is no user access to hazardous voltage, sharp edges, hot components, fan blades, or any other item that might cause injury. A specified “finger probe” is used to probe all openings. Positive earthing connections and bonding straps must be provided where necessary.

C. Layout

An appropriate isolation strategy must be defined and rigidly applied throughout the design. Creepage and Clearance spacings must separate all hazardous voltages from user accessible points. There should be a very clear channel between primary and secondary circuits, similar to that illustrated in Fig. 8. It should be noted that hazardous voltage levels may be present on some secondary circuits where a low voltage output might be generated from a low duty-cycle, high peak voltage, PWM power pulse.

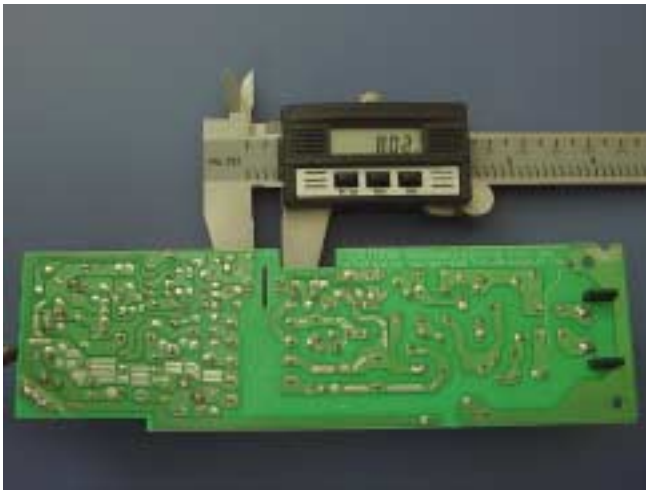

Fig. 8. PCB layout view clearly showing the Clearance spacing and Creepage slot under the optocoupler. between primary and secondary circuitry.

D. Design

Remember that hazardous conditions may also exist on low-voltage outputs where high power is possible (>240 VA). As a minimum, effective current limiting may be required. The power supply should also be able to withstand an overload test consisting of blocking the air vents, stopping the fan, and overloading or shorting the output until the condition becomes stabilized or the ultimate result is achieved. Failure would certainly include flame and smoke, excessive heating of components, flying shrapnel from an exploding component, or failure to pass an appropriate HiPot test.

The design must also ensure that no single failure causes any of the above hazardous conditions. The safety engineer randomly and selectively opens or shorts any component with flame-detecting cheese cloth draped around the unit under test. Anticipating these tests and designing for them is a necessary task. As an example, Fig. 9 shows a typical application of a low-voltage controller for an off-line supply, but modified in two simple ways. First, the start-up resistor to initially power the IC controller has been divided into two resistors, R1 and R2, allowing either to be shorted while still limiting current from the high-voltage bus. And secondly, anticipating a short applied between drain and gate of the power FET, the designer has used a fusible resistor for Rg, and added D1 to shunt excessive current around the IC and to ground through Z1.

In anticipation of these safety tests to simulate failures by shorting components, consideration should be given to insuring that either the input fuse blows (which is acceptable) or that, at least, dramatic failures (such as exploding capacitors) are prevented. Placing MOV protection devices across large electrolytic capacitors is a common way to limit over-voltage. Where voltage is not an issue, two capacitors in series may allow one to be safely shorted – a technique useful when adding a noise-reducing bypass capacitor between primary and secondary grounds.

XII. POWER SUPPLY CERTIFICATION

While testing procedures may vary according to test agency, type of power supply, and application or end use, they typically include the following steps:

- A construction analysis on open or unsealed test samples, checking:
  - Insulation coordination
  - Clearances, Creepage, and solid insulation dimensions
  - Accessibility
  - Protective earthing
  - Strain relief
  - Mechanical evaluation
- Determination, using both analysis and physical measurement, of internal working voltage limits
- Worst-case operational testing, exercising both input voltage and load variations.
- Single fault and overload testing including short circuits
- Heating tests under normal operating conditions
- Humidity
- Hi Pot leakage current measurements
- Flame tests
- And whatever additional specialized testing is deemed necessary

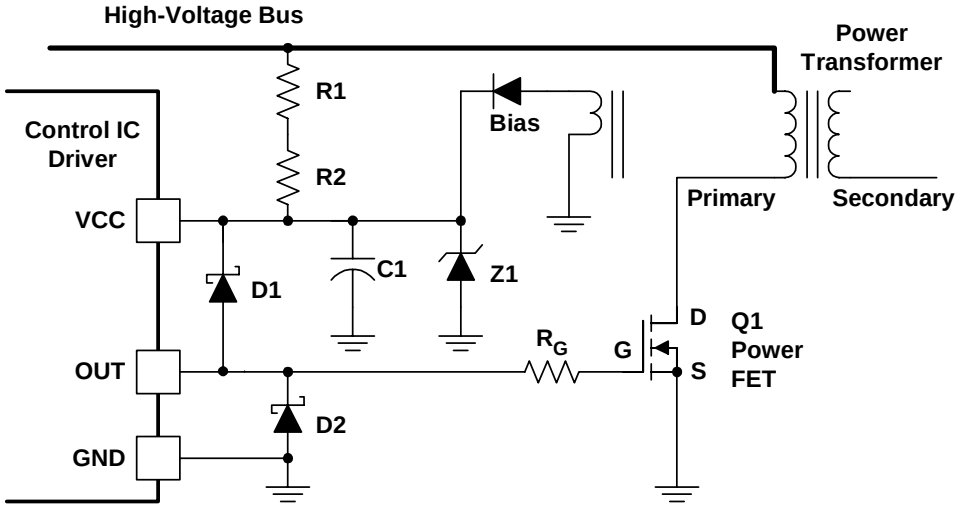

Fig. 9. An example of start-up circuitry with components R2 and D1 added in the interests of safety.

The certification process starts with the submittal of an application and documentation package to completely describe the power supply and all its component parts and materials. A number of units for testing are also provided, often five without an enclosure and five in completed form, together with a purchase order for the cost which typically ranges between $6000 and $8000 for the average small power supply. The certification process can take as little as 6 to 8 weeks, but with a product containing design deficiencies, can go much longer.

XIII. Acknowledgement

Texas Instruments recognizes and appreciates the technical material and support provided by Underwriters Laboratories in the preparation of this seminar topic. For additional information on this subject or about the specialized seminars presented by UL, use the following contact information.
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Topic 2

Sequencing Power Supplies in Multiple Voltage Rail Environments

Texas Instruments

Sequencing Power Supplies in Multiple Voltage Rail Environments

David Daniels
Dirk Gehrke
Mike Segal

ABSTRACT

Designers must consider timing and voltage differences during power up and power down in systems where multiple power rails are involved. A simple example would be a single DSP with its core and I/O voltages, requiring power supply sequencing. The possibility for a latch-up failure or excessive current draw exists when power supply sequencing is not designed properly. The trigger for latch-up may occur if power supplies are applied at different potentials of the core and I/O interfaces. This paper addresses some of the more common sequencing requirements of digital signal processing (DSPs), field programmable gate arrays (FPGAs), application-specific integrated circuits (ASICs) and microprocessors, and proposes a variety of practical solutions implemented with power management devices. These techniques take advantage of the reset, power good, enable and soft-start features available on many types of power management devices ranging from low drop out (LDO) regulators to plug-in power modules.

I. INTRODUCTION

High-performance signal processing devices, such as FPGAs, ASICs, PLDs and DSPs require multiple power supplies that generate different voltages for the core and I/O voltages. The order in which these voltages power up and power down can prove critical to device operation and long term reliability. This paper addresses some of the reasons devices require the different types of power supply sequencing and offers examples of practical supply sequencing solutions.

II. WHY SEQUENCE POWER SUPPLIES?

Designing a system without proper power supply sequencing may introduce potential risks, including compromised reliability and immediate faults. Long term reliability is sacrificed when an out-of-bounds condition persists on a multi-supply device for extended periods of time. The risk comes when there is an active power supply rail and an inactive supply on a device for long time periods. This condition can stress electrostatic discharge (ESD) protection and other internal circuits that interface between the different voltages. The amount of time the device can be stressed before potential damage occurs under these conditions may be measured in months, but it is the cumulative exposure to these conditions that determines the usable life of the product. While a few poorly controlled power-up and power-down cycles are unlikely to damage a device, a system that is power cycled time after time without proper power supply sequencing can eventually fall victim to this failure mode.

Another risk of improper power supply sequencing in a system can cause immediate damage to a device. This failure is often a result of excessive current flow into a pin or excessive voltage differential across pins that stress internal components. The causes of these immediate failures are similar to those of the reliability failures. The difference is how the device is affected by the stresses.

A. Latch-Up

Since most multi-supply devices are fabricated in CMOS technology, the devices are susceptible to an electrical failure mode called latch-up. Latch-up can occur when voltage and current levels beyond the normal operating level stress pins of a powered device. When latch-up occurs, the device draws unusually high supply current which may render the device inoperable and/or cause permanent damage to the device.

Fig. 1 depicts a cross section of a CMOS inverter with the parasitic bipolar transistors overlaying the illustration.[1][2] The source of the N-channel MOS device serves as emitter, the N-well as collector, and substrate as base of the parasitic bipolar NPN transistor. Similarly, the source of the P-channel MOS device serves as emitter, the N-well as base, and the substrate as collector of the parasitic bipolar PNP. These parasitic bipolar transistors comprise a PNPN structure commonly known as a silicon-controlled rectifier (SCR). The PN junctions of the parasitic transistors are normally reverse-biased. However, a PN junction of the parasitic SCR may become forward-biased due to electrical disturbances resulting in SCR conduction which may result in device failure. Among electrical disturbances which may cause latch-up are voltages on pins beyond the supply voltage rails, large DC currents in the substrate or N-well, and displacement currents in the substrate or N-well resulting from fast-transitioning internal nodes.

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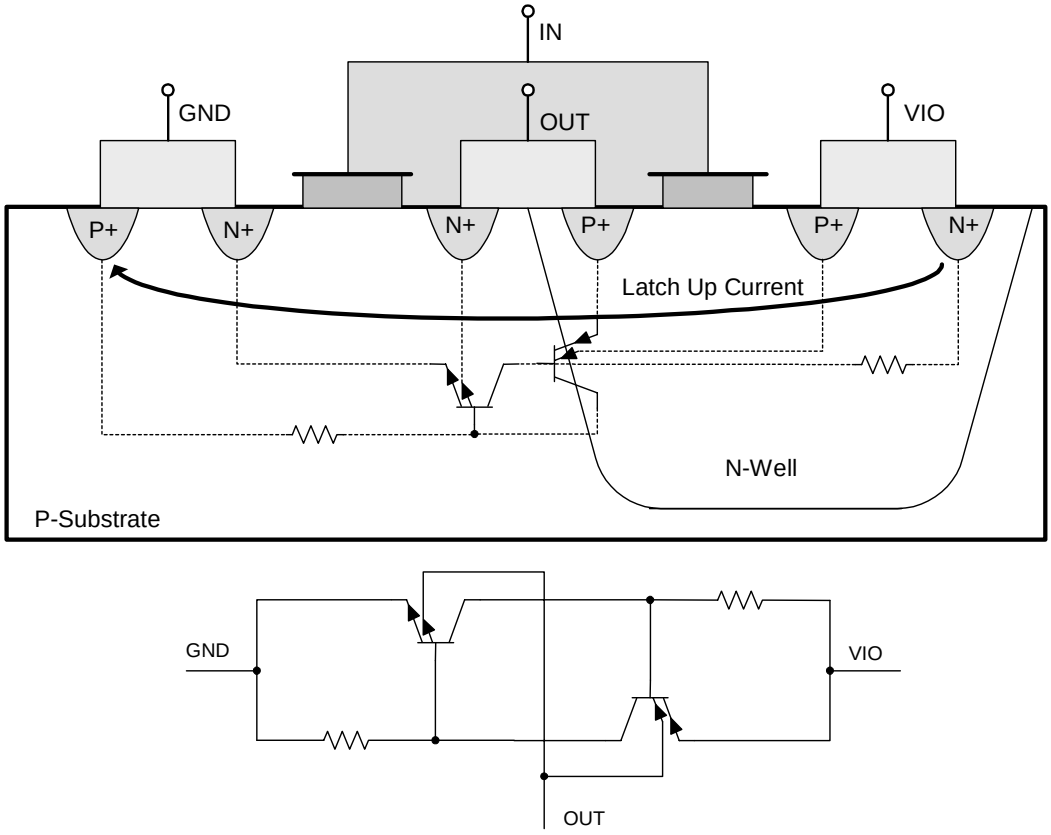


Fig. 1. Cross-section of CMOS inverter.

Fig. 2 represents the architecture of a multi-voltage device, such as a programmable logic device (PLD), interfacing to an external driver.[3] To illustrate some of the problems with sequencing power supplies, the system consists of three power supplies: V_{CORE}, V_{IO}, and V_{EXT} at 5 V, 3.3 V and 3.3 V, respectively.

Consider the following scenario: V_{IO} supply is active, V_{CORE} is inactive, and the driver input is not initialized. Since the driver is not in a known state, Q1 could be biased on, sourcing current through ESD diode D1. The magnitude of the current depends on the impedance of Q1, D1 and the inactive supply. Latch-up may occur as current flows through the ESD diode when the core supply ramps up. Whether this current causes a catastrophic latch-up failure, latent reliability issue, or neither, depends on robustness of the device design. In other words, damage may not occur if magnitude of the current is sufficiently low that the silicon can conduct the current without compromising reliability.

A potential latch-up issue arises when peripheral devices, such as data converters and memory, are coupled to the I/O pins of a multi-supply device and powered from a different supply that is ramping. Fig. 2 shows an external driver coupled to the I/O pin that has a "sneak path" through the anti-parallel body diode of Q3 when the V_{EXT} pin voltage is lower than V_{IO}. This issue can easily be resolved by connecting the V_{EXT} and V_{IO} pins to the same power supply. When V_{EXT} is active and the external driver sources current into the pin when V_{CORE} or V_{IO} is ramping, the potential for latch-up in the multi-supply device exists.

Trends in the semiconductor industry include increasing device speed, including more features, reducing power consumption, and reducing device size, all the while shortening product development cycle times. To meet these goals, design teams pack more components into a smaller area by using smaller device geometries, thinner well structures, and lighter substrate and well concentrations. Unfortunately, these design techniques increase the ohmic resistance and gain (or "beta") of the parasitic PNP and NPN transistors which, in turn, increases the likelihood of latch-up. Design techniques to prevent latch-up include using protection circuits and "guard rings". Protection circuits are used on input and output pads to safely shunt current and guard rings are used around wells to provide low-resistance. Both these prevention techniques come at the penalty of device size and cost.

The device's core voltage, susceptibility to latch-up, and supply sequencing order are, all too often, determined after pre-production silicon is available and device characterization and qualification are performed. With the emphasis on meeting cost and customer timetables for the latest product, if only minor issues are found with a device (such as a preference for supply sequencing), the issues are documented and the device released to market.

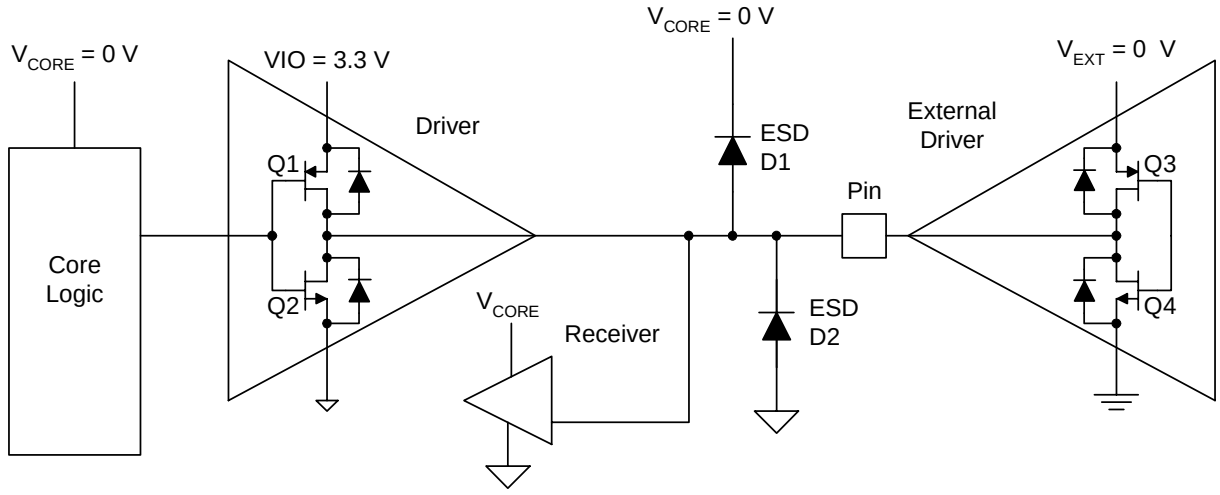


Fig. 2. Close-up of a multi-voltage device.

B. System-Level Bus Contention

Power supply sequencing may be required to prevent system-level bus contention, in which the bidirectional I/O pins of a DSP and external peripheral device oppose each other. Since the bus control logic originates in the core section of the DSP, powering I/O prior to the core may result in both the DSP and peripheral simultaneously configured as outputs. If the data values on each side are opposing, then the output drivers contend for control, as shown in Fig. 3.

Excessive current flows in one of the paths shown, depending on the opposing data-out patterns. The outputs contend for control and excessive current flows when the data values are opposing. This excessive current may damage the bidirectional I/O ports. Following the recommendation to power the core at the same time or before the I/O prevents undefined logic states on the bus control signals. [4]

III. SEQUENCING SCHEMES

There are three distinct schemes to power-up and power-down multi-rail power supplies: sequential, ratio-metric, and simultaneous [5]. The appropriate sequencing scheme is dependent on device requirements. The manufacturer's data sheet does not explicitly name which power sequencing scheme to implement, but rather outlines voltage and timing conditions that cannot be exceeded on power supply pins. Note that some devices allow out-of-bounds conditions for a short period of time. Using the pin conditions and the waveforms in the following section, a sequencing methodology can be chosen to meet the processor requirements.

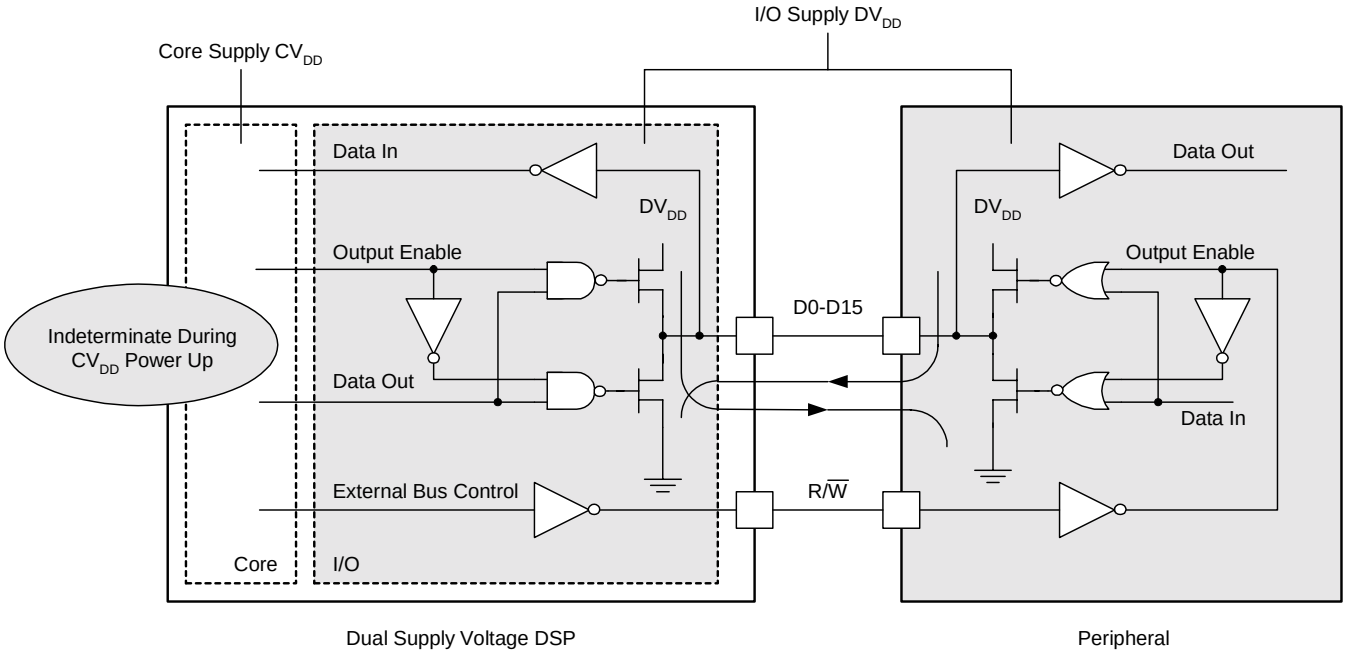


Fig. 3. System-level bus contention.

A. Sequential Sequencing

The sequential scheme of power supply sequencing is best described as one power supply ramping and settling to its final regulation voltage and then the second power supply ramping after a time delay. This method is used to initialize certain circuitry to a known state before activating another supply rail. An example applying the core supply rail prior to the I/O supply starting is shown in Fig. 4a.

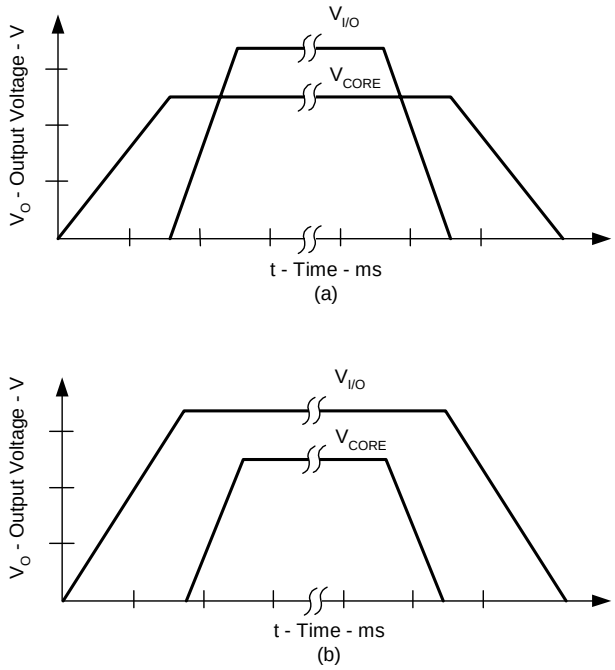


Fig. 4. Sequential sequencing schemes.

The following is an excerpt from a footnote in a device specification with recommendations best suited to using sequential power supply sequencing:

"System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as or prior to the I/O buffers and then powered down after the I/O buffers." [6]

An alternative power supply sequence order would call for the I/O supply to power up first and the core supply to start after the I/O power supply reaches regulation, see Fig. 4b. In the particular example [7], this method meets the recommended power sequencing for the device as long as the delay time for the start up of the core supply is less than 100 ms. As presented later in this topic, a typical hardware implementation employs an output voltage monitor to develop a power good (PG) signal for the first power supply, which then connects to the enable (EN) function of the second power supply.

B. Ratio-Metric Sequencing

For a dual power supply implementing ratio-metric sequencing, both power supply outputs ramp at the same time *and in proportion* until regulation is reached. Fig. 5a illustrates ratio-metric power sequencing where the core and I/O supply reach regulation at approximately the same instant. During power-up the core supply is a percentage of the I/O supply until regulation is reached. Similarly, during power-down the core is a specific percentage of the I/O supply voltage. Another example of ratio-metric sequencing may find the core supply voltage slightly greater than the I/O supply during the power-up and down, see Fig. 5b. In this particular case, to ensure the I/O buffers have valid inputs, the core rail is powered slightly before the I/O rail to eliminate problems with bus contention. [8]

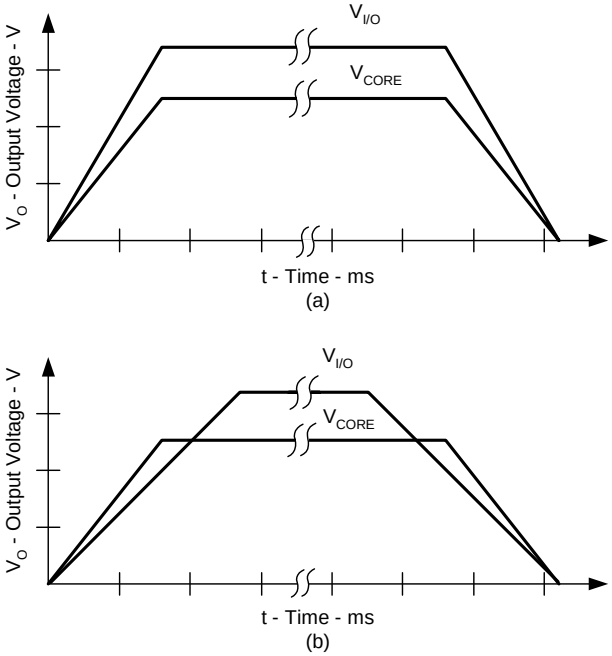


Fig. 5. Ratio-metric sequencing.

C. Simultaneous Sequencing

The simultaneous power sequencing method is similar to ratio-metric sequencing in that both power supply outputs ramp at the same time. However, in simultaneous sequencing, the objective is to minimize the voltage difference between the two supply rails during power up and down, as shown in Fig. 6, until regulation is reached for the core supply. This sequencing method is useful for devices that have "sneak paths" between supply pins or draw excessive current during startup if internal logic has not transitioned to a stable state. Reference [9] recommends simultaneous sequencing to minimize transient start-up currents.

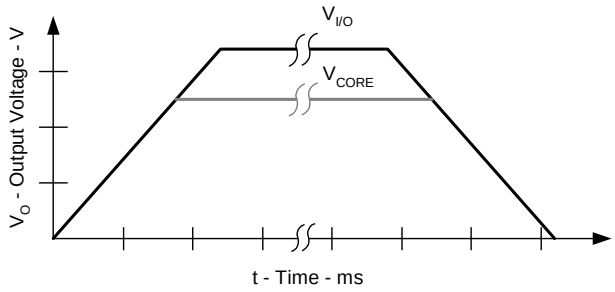


Fig. 6. Simultaneous sequencing.

The following sections show many examples of power sequencing implemented with:

- Diodes
- Low-dropout (LDO) linear regulators
- Supply voltage supervisors (SVS)
- Power distribution switches
- Hot-swap controllers
- Microcontrollers
- Switch-mode controllers (power FETs external)
- Switch-mode converters (power FETs internal)
- Plug-in power modules

IV. Sequencing Implementations Illustrated with LDOs

A. Diodes

Diodes are often used to facilitate sequencing requirements. Though diodes alone cannot achieve true sequential, ratio-metric or simultaneous sequencing, they can help maintain proper relation between various supply voltages.

Fig. 7 illustrates use of a Schottky diode to limit voltage differential between the core and I/O rail. The Schottky diode further reduces potential stress on devices by bootstrapping the I/O supply and shortening the delay between supply ramps. [5]

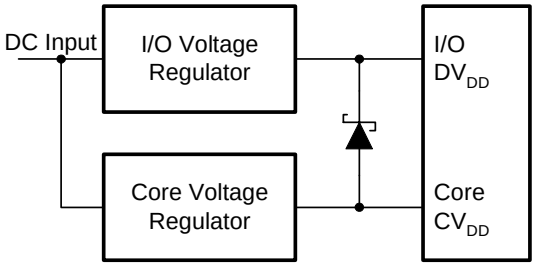


Fig. 7. Schottky diode limits voltage differential.

Fig. 8 shows rectifiers in combination to help meet these microprocessor requirements:

- *"V_{IN} must not exceed V_{DDH} by more than 2.5 V at any time, including during power-on reset.*
- *V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 1.6 V at any time, including during power-on reset.*
- *V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4 V at any time, including during power-on reset."* [17]

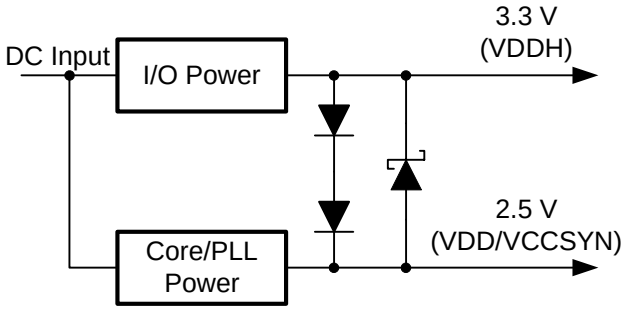


Fig. 8. Combination of diodes limits voltage differential.

"Note: There are internal diodes connected serially between VDDH and VDD, and vice-versa for ESD protection. If one of the voltages (VDD or VDDH) is applied and the other power pins are not driven, then the internal diodes pull up these pins. However, a problem could occur if one of the voltages (VDD or VDDH) is applied and the other voltage is forced to GND. In this case, the ESD diodes might be destroyed." [17]

To achieve *true* sequential, ratio-metric or simultaneous sequencing, enlist the capabilities of a wide range of active devices, as discussed in the following sections.

B. LDO Enable Via Supply Voltage Supervisor (SVS)

Sequential Sequencing

Fig. 9 shows an implementation of a supply voltage supervisor (SVS) to realize a sequential sequencing scenario. The load of this power supply is an FPGA which requires sequential sequencing. The power solution shown employs a 5-V input supply voltage rail. The core voltage is powered up first and, once the core voltage has ramped, the I/O voltage rail is enabled. Advantages of a linear regulator over a switch-mode approach typically include lower noise, reduced board space and cost. A key disadvantage is lower efficiency and, as a result, increased power dissipation.

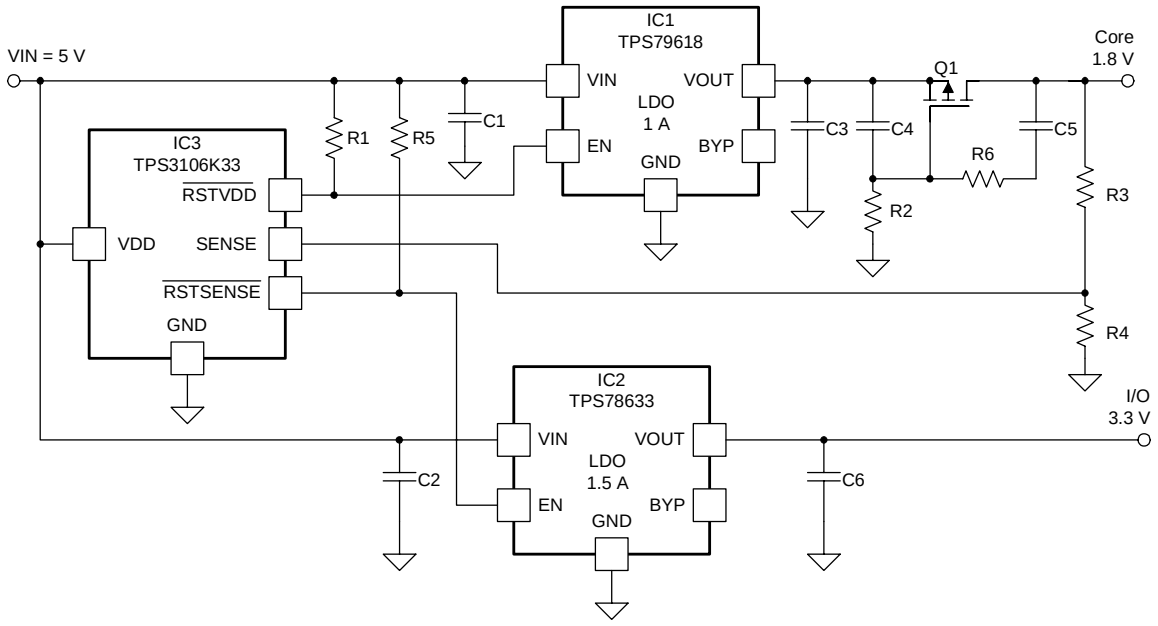


Fig. 9. Sequential sequencing using SVS.

This solution is based on two LDOs, IC1 to supply core voltage and IC2 for the I/O voltage rail, along with an SVS, IC3. The dual SVS, with trip point threshold voltage of 2.941 V (typical), monitors the input voltage rail. Once the input voltage rail has reached the threshold of 2.941 V, the SVS reset output transitions from low to high impedance state after a delay of 130 ms, enabling LDO IC1. Once LDO IC1 is enabled, the core voltage ramps up towards its final value of 1.8 V. To ensure that the input voltage rail does not drop due to the high inrush current demand of the capacitor bank and the FPGA, a current-limiting circuit has been implemented. Without this current-limit circuit, the input voltage could potentially droop during the switch-on cycle. This current-limit circuitry, consisting of Q1, C4, R2, R6 and C5, provides smooth charging of the load during power-up.

Core voltage is monitored via a comparator incorporated in SVS IC3. Voltage divider R3 and R4 adjusts the threshold voltage to the particular needs of the application. In this case, it has been adjusted to a threshold voltage of 1.7 V. Once the core voltage reaches the threshold voltage, IC3 enables LDO IC2, which provides the I/O voltage to the system, and the I/O voltage ramps to its final value of 3.3 V.

The power-up and power-down waveforms of this implementation appear in Fig. 10.

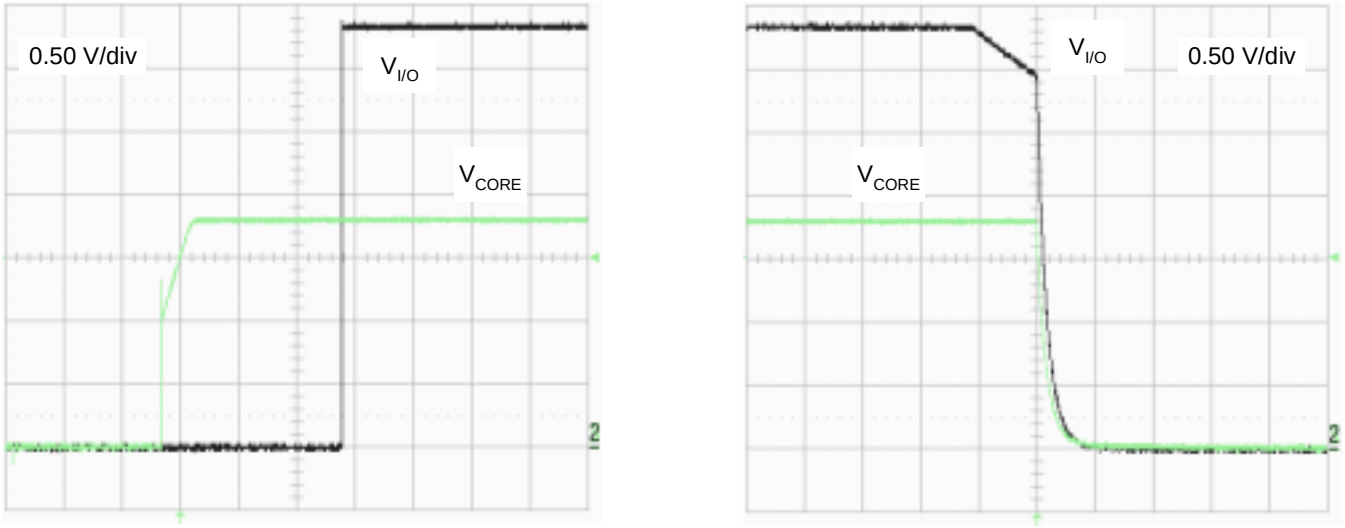


Fig. 10. Ramp-up (a) and ramp-down (b) waveforms for circuit of Fig. 9.

Simultaneous Sequencing

Some applications require either a specific slew rate or a maximum inrush current during power-up and power-down, which can be realized with the circuit in Fig. 11.

The power-up and power-down sequencing circuit employs network R3 and C2 to generate a ramp-up slope. This network is the slew rate reference for the output of the LDO during power-up and power-down. The operational amplifier compares the output voltage at its non-inverting input with the voltage applied to its inverting input. It then adjusts the output voltage to match the slew rate determined by the RC network. When $\overline{\text{ENABLE}}$ transitions low, Q1 is switched off, and R3 starts to charge C2 to the input voltage rail level. When V_{OUT} reaches 2.5 V, set by R1 and R2, the voltage at the operational amplifier inverting input continues to rise, causing the operational amplifier output to decrease. This reverse-biases D1, thereby removing the power-up and power-down sequencing circuit from the feedback loop. R4 and C1 ensure a smooth voltage rise during power-up.

In this example, the output voltage set point can be calculated as follows:

$$R1 = R2 \times \left[\left(\frac{V_{OUT}}{V_{REF}} \right) - 1 \right]$$

where V_{REF} = 1.224 V for the LDO shown.

Fig. 12 features simultaneous sequencing circuitry that programs a required slew rate during power-up and power-down using IC2 as a tracking LDO.

The power-up and power-down sequencing circuit is using the same basic circuit as described above with programmable slope. In this example, the core voltage must track the I/O voltage during power-up and power-down. Additionally, the I/O voltage must be within 600 mV of the core voltage during power-up and power-down. If these conditions are violated, the processor could be damage due to forward-biasing of the substrate diode.

During power-up and power-down, IC4 provides active tracking to ensure that the voltage difference between I/O and core voltage is far less than the required 600 mV. Schottky diode D3 provides an additional level of protection.

During power-up, IC1's output voltage increases with the applied slope ramp at the inverting node of IC3. Operational amplifier IC4 derives the ramp-up and ramp-down slope from the 2.5-V I/O output voltage rail. During power-up, the I/O voltage slowly increases, and this voltage is applied to the inverting node of IC4. The non-inverting node detects the core voltage, which is the output of linear regulator IC2. When the core voltage reaches 1.5 V, set by R5 and R6, the inverting input of operational amplifier IC4 continues to rise, causing the operational amplifier output to decrease. This reverse biases D2, removing the tracking circuit from the feedback loop. Fig. 13 displays power-up and power-down waveforms, respectively.

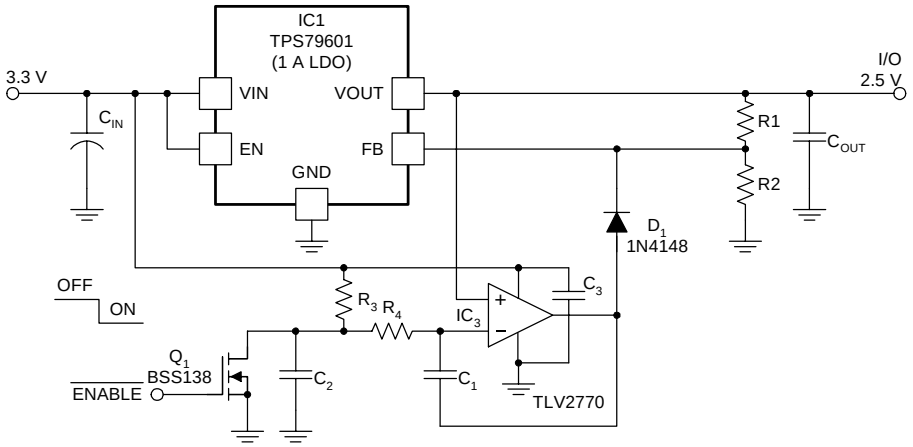


Fig. 11. Capacitor-programmable slew rate circuit.

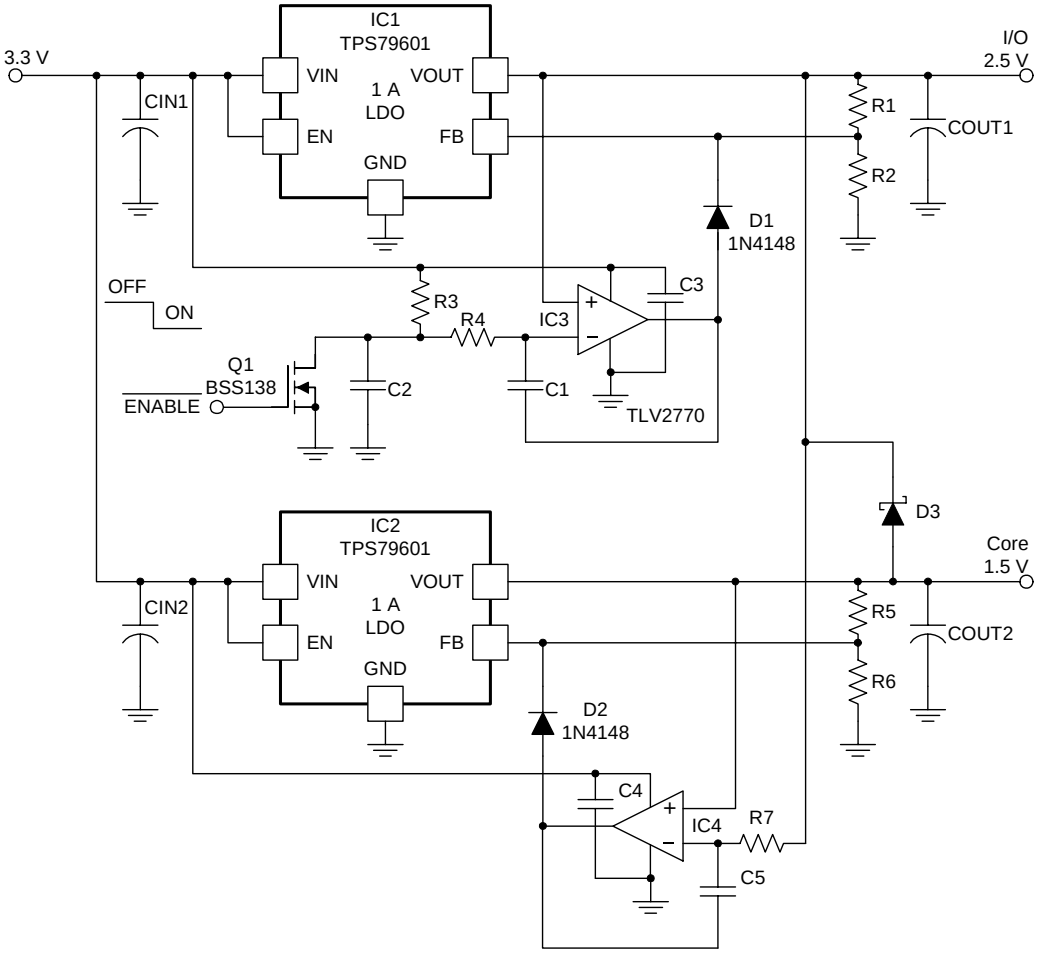


Fig. 12. Simultaneous sequencing with capacitor-programmable slew rate circuit.

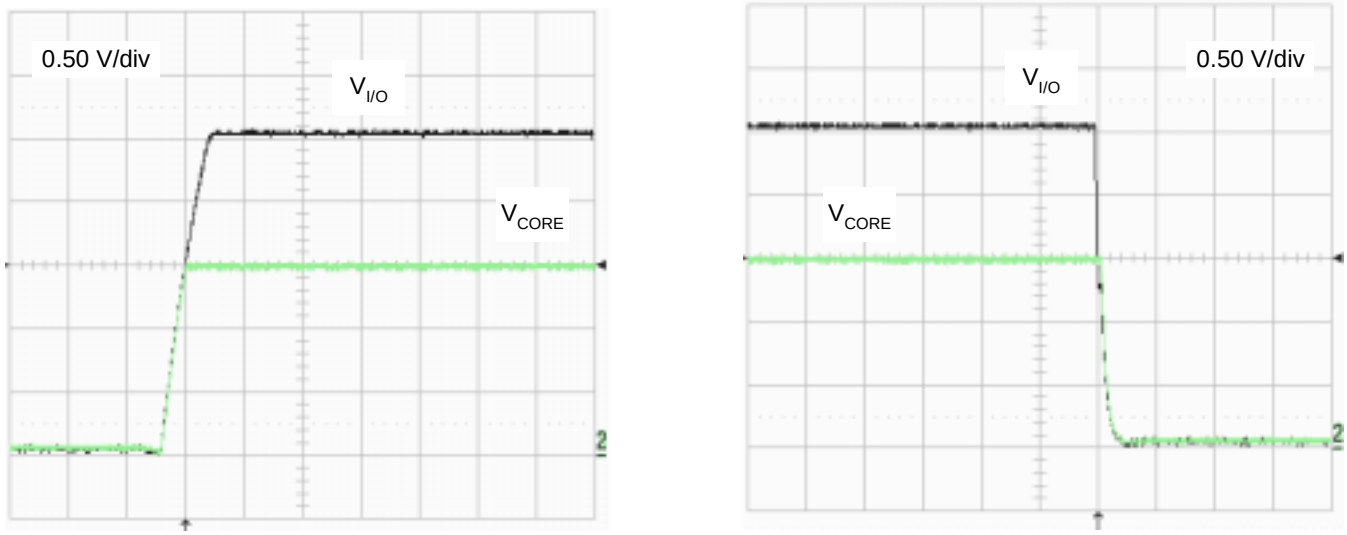


Fig. 13. Power-up (a) and power-down (b) waveforms for circuit of Fig. 12.

C. LDO and Power Distribution Switch

Sequential Sequencing

Some applications challenge the designer to apply core voltage prior to I/O voltage, even though the input source voltage is already at the I/O voltage level. A high-side power distribution switch can be used to disable the I/O supply until the core voltage is powered up and stable. Fig. 14 shows a sequential power supply sequencing implementation using the TPS2150, which integrates a high-side power switch with an LDO.

The TPS2150 uses the power good function of the LDO to enable the power switch, resulting in the power-up waveforms of Fig. 15a. The power switch and LDO feature pull down MOSFETs to discharge the bulk capacitance when the devices are disabled (Fig. 15b).

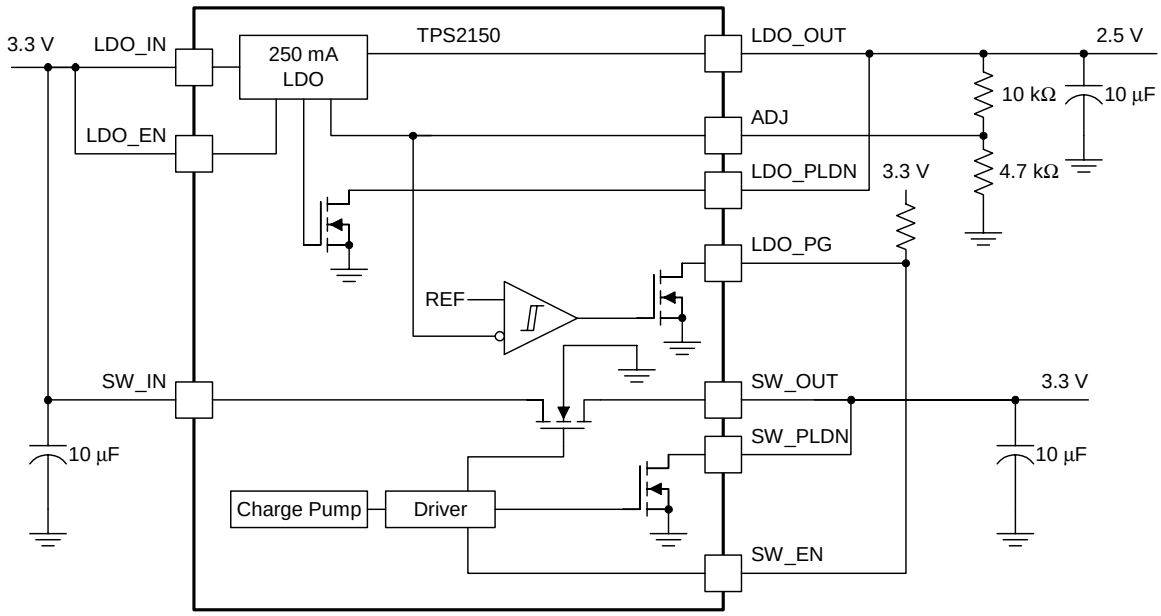


Fig. 14. Sequencing with combination LDO/high-side switch (core then I/O).

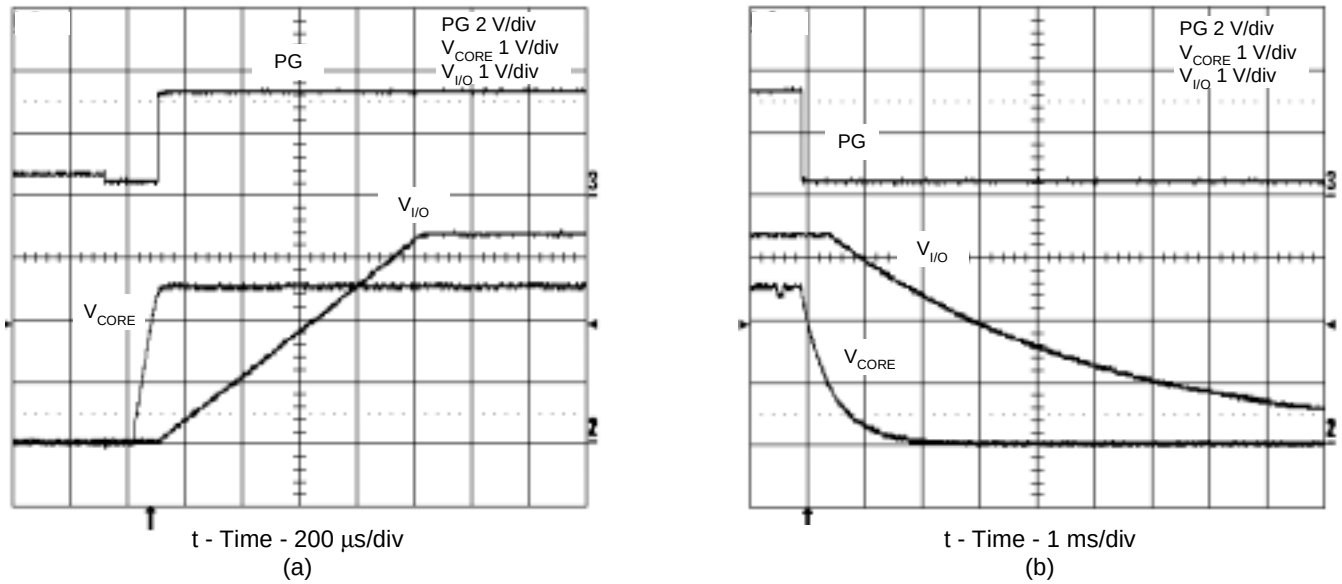


Fig. 15. Power-up (a) and power-down (b) of circuit in Fig. 14.

Fig. 16 implements the opposite configuration, in which the I/O voltage is applied before the core at turn-on. Corresponding waveforms are shown in Fig. 17.

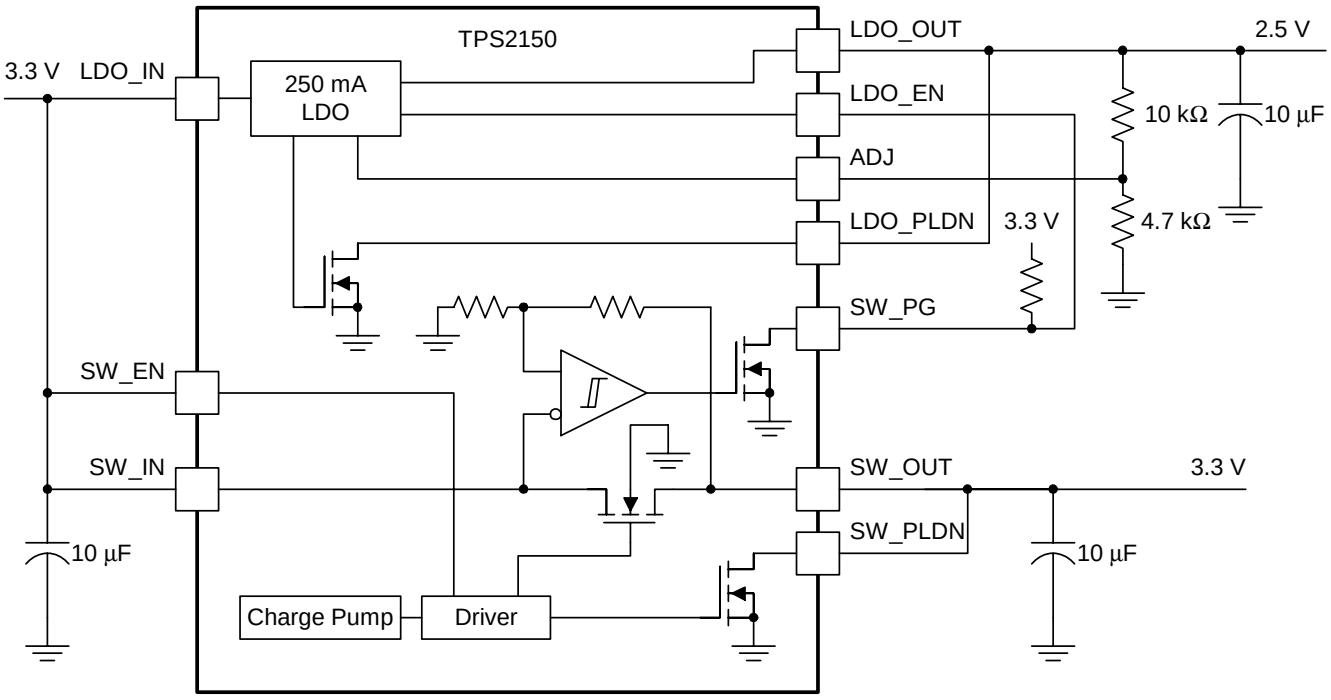


Fig. 16. Sequential sequencing (I/O then core).

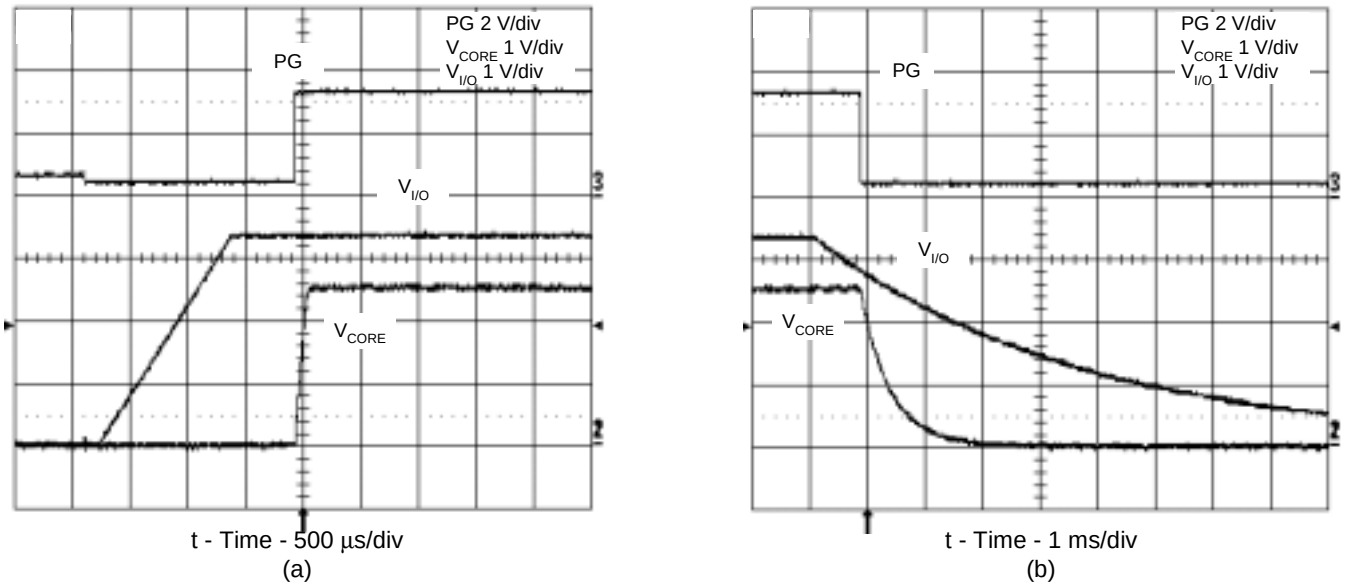


Fig. 17. Power-up (a) and power-down (b) waveforms for circuit of Fig. 16.

D. Hot-Swap Control

Simultaneous Sequencing

Another method to power-up and power-down with minimum voltage difference between the power supply rails is to use MOSFETs between the supply and load. Fig. 18 shows a simplified schematic using two MOSFETs and a TPS2331 hot swap controller to provide simultaneous start-up sequencing. By driving the gates of the MOSFETs with the same gate driver, the power supply rails effectively ramp together (Fig. 19a). The TPS2331 features an integrated pull-down transistor to discharge the bulk output capacitors, see Fig. 19b. The Schottky diode clamps the core supply during power-down.

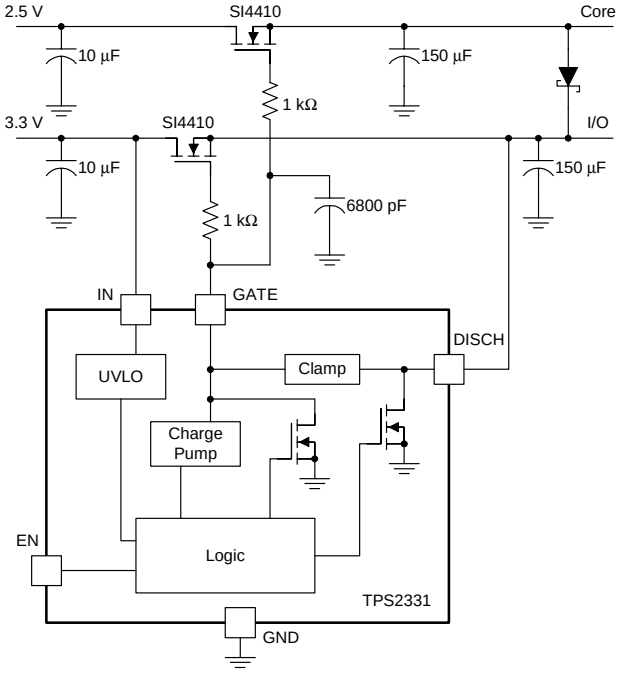
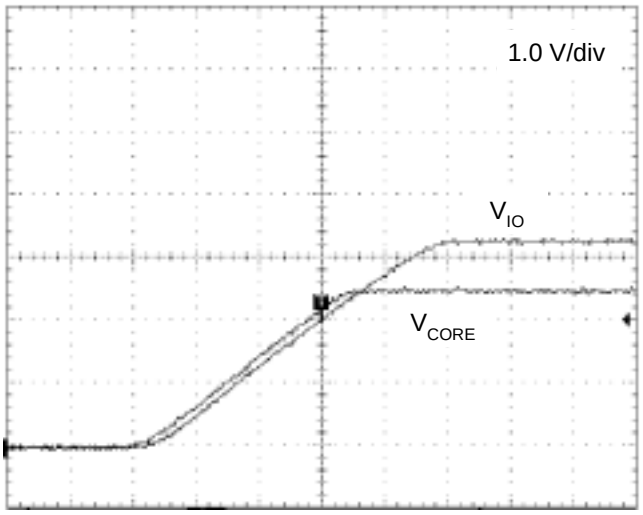
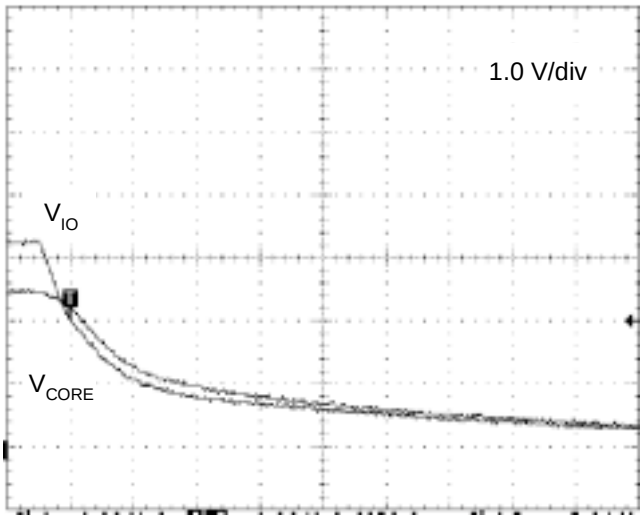


Fig. 18. Simultaneous sequencing with hot-swap controller.



t - Time - 500 µs/div
(a)



t - Time - 20 ms/div
(b)

Fig. 19. Power-up (a) and power-down (b) waveforms for circuit of Fig. 18.

E. Microcontroller

Microcontrollers are among the most versatile devices available for sequencing. If the power supplies to be controlled feature enable pins, then controlling them is a simple matter of using general purpose input and output (GPIO) lines. If the enable function is not available, an in-line MOSFET or power distribution switch can be used to control the power supply, either with a GPIO or PWM signal.

Use of a microcontroller is illustrated with the MSP430, a 16-bit RISC processor featuring several analog peripherals and a JTAG interface. The circuit of Fig. 20 uses the TPS725xx family of LDOs to provide 3.3 V, 2.5 V and 1.8 V from an input DC source. These LDOs have an enable pin and reset function. This circuit can easily be expanded to any number of voltage rails. The MSP430 monitors a control variable to determine when each rail should be activated. For power sequencing applications, the two most commonly controlled variables are time and voltage.

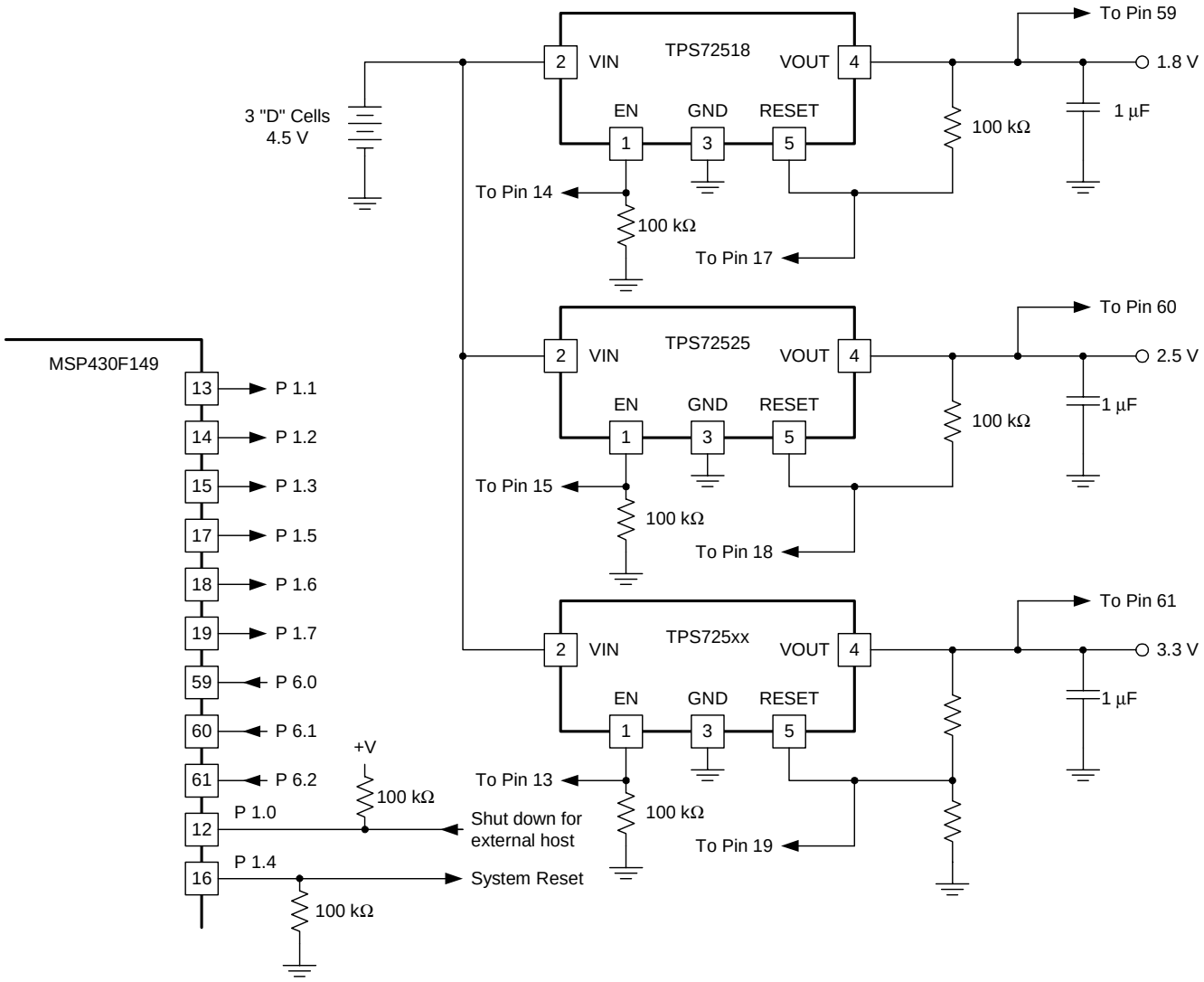


Fig. 20. Sequencing implemented with the MSP430 microcontroller.

Sequential Sequencing

When time is the control variable the first rail is enabled then, at a specific time thereafter, the next rail is enabled. Some time after that the next rail is enabled and so on, until all rails have been enabled. The MSP430 provides the timing sequence and the control signals to turn on the power supplies (Fig. 21).

If voltage is the control variable, then the first voltage rail is activated and its rise is monitored via an analog-to-digital converter (ADC). When the first voltage rail has reached a specific voltage level, the next voltage rail is enabled and its rise is monitored until it has reached a specified voltage level, at which point the next voltage rail is enabled and monitored. This continues until all voltage rails have been enabled (Fig. 22). When using voltage as the control variable, either a GPIO or PWM signal can be used as the enable signal, depending on whether rail tracking is required. Of course, a combination of voltage and timing control can also be used.

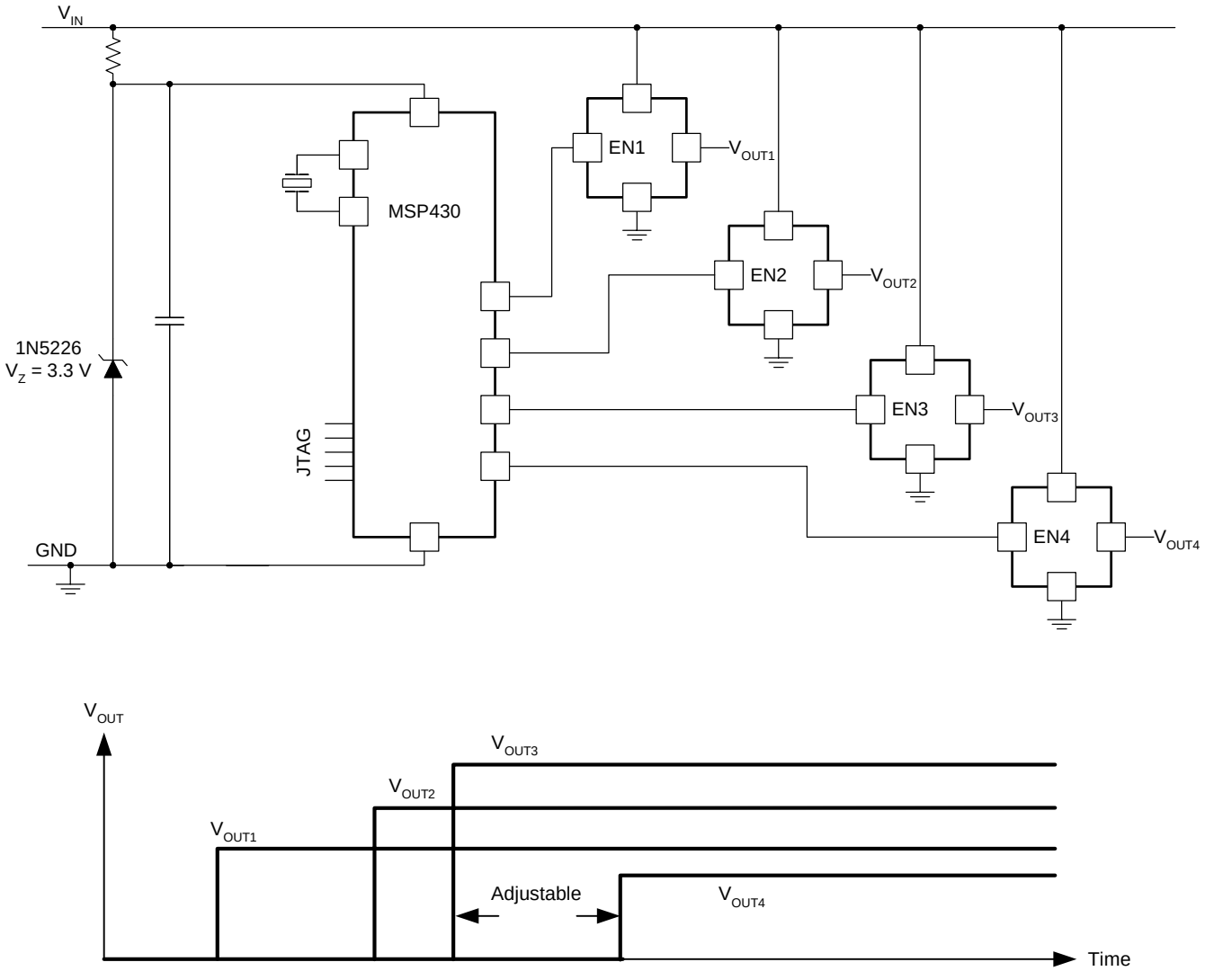


Fig. 21. Sequential sequencing with microcontroller (time as the control variable).

Once the MSP430 has turned on all the voltage rails and applied the system reset, it enters the monitor mode. It continually checks the output voltages, via the reset or output pins, depending on whether time or voltage is the control variable. If a fault occurs, the MSP430 enters an error routine. The most obvious fault would be the loss of a voltage rail, but other faults such as over- or under-voltage could also be monitored. The actions taken in the error routine are completely application-dependent. The simplest action is to power down all rails, but programmability offers the user complete control.

Power-down sequencing can be just the opposite of the power up sequence, or any sequence required to meet system demands. One addition to the power-down sequence could be turning on dummy loads to discharge the output filter capacitors. [16]

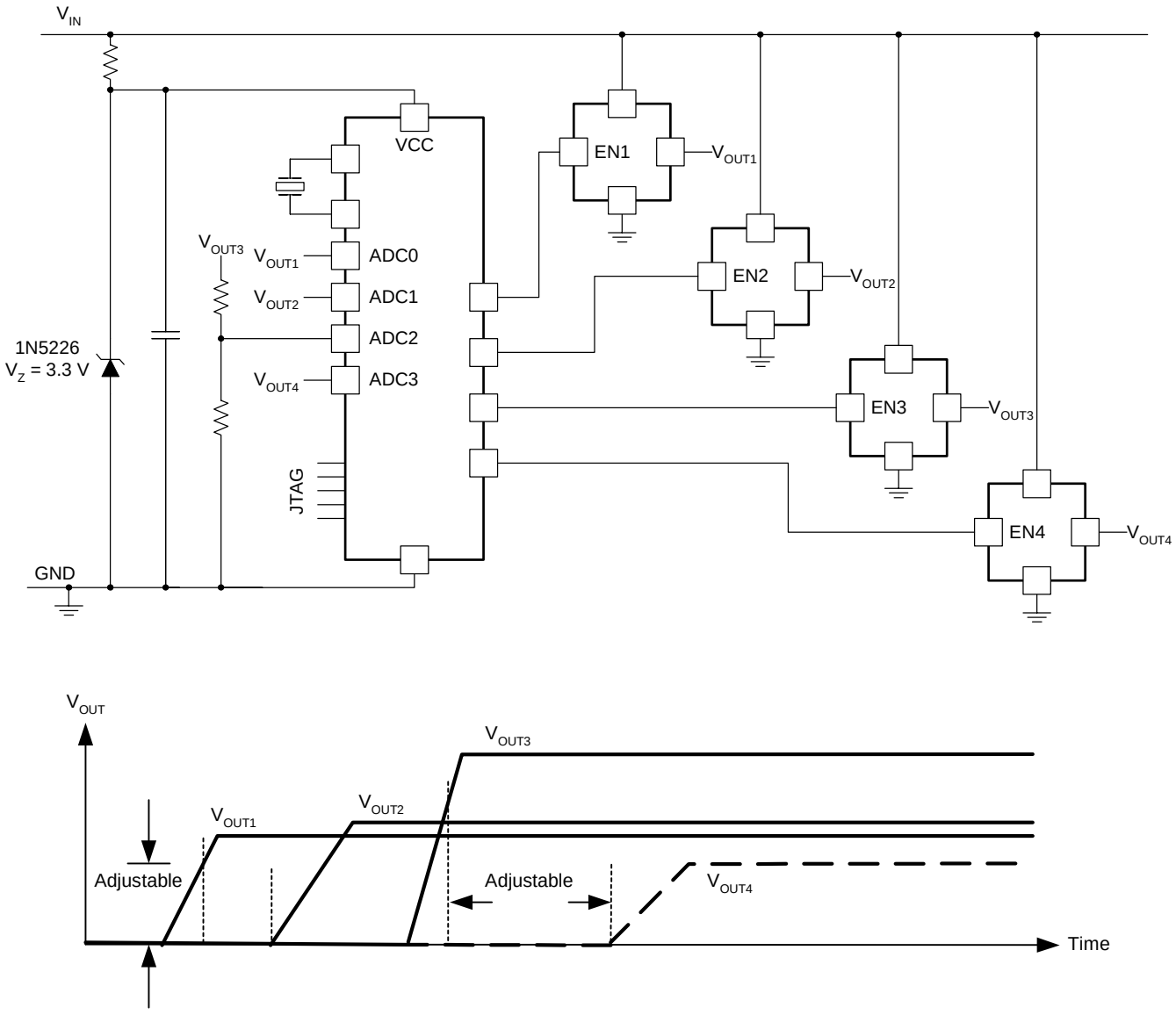


Fig. 22. Sequential sequencing with microcontroller with voltage as the control variable.

V. SEQUENCING WITH SWITCH-MODE CONTROLLERS, CONVERTERS AND MODULES

A. Pre-Bias Start-Up and Synchronous Rectifier

Many switch-mode power stages employ synchronous rectification to improve efficiency, as illustrated by the simplified synchronous buck converter shown in Fig. 23. In this example, VIO comes up first, and applies core voltage through the series diodes before the core's converter is enabled. Defining this as a pre-bias condition, in which voltage is applied at the converter output before the converter is enabled. When the converter's PWM controller is enabled, it soft-starts the high-side FET, and its duty cycle (D) ramps gradually from zero to that required for regulation. However, if during soft-start the synchronous rectifier (SR) FET is on when the high-side FET is off (SR FET duty cycle = 1-D), the SR sinks current from the output (through the inductor), tending to cause both the core and I/O voltages to drop. It is for this reason that PWM controllers with pre-bias start-up have been introduced, which disable SR drive during start-up. Until drive to the SR is enabled, inductor current flows through the parasitic body diode of the SR FET rather than through the channel. Once the soft-start time is complete, drive to the SR is enabled.

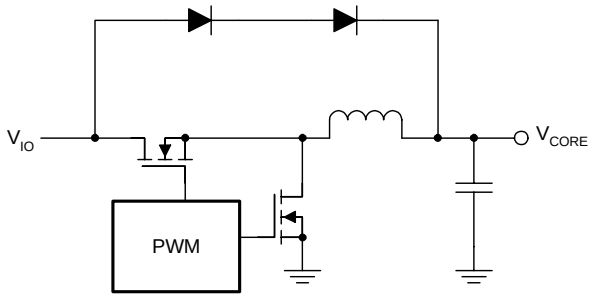


Fig. 23. Example of pre-bias condition.

The need for synchronous converters with pre-bias start-up also arises when using a sequential power-up technique with some ASICs, in which a leakage path within the device causes some I/O voltage to appear on the core voltage before the core converter is enabled. Fig. 24 uses a PTH series power module for illustration. The PTH power modules incorporate synchronous rectification, so can sink current under normal operating conditions, but the 3.3-V and 5-V input versions do not do so during power-up, or whenever the module is turned off via the Inhibit pin. In Fig. 24, module U1 (PTH05020W) produces 2.5 V for the core.

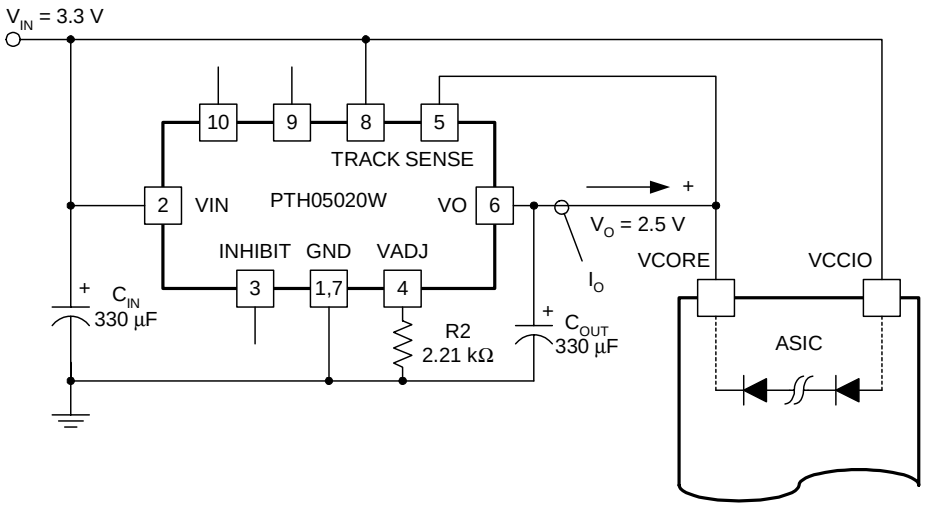


Fig. 24. Pre-bias example with PTH power module.

Fig. 25 shows the waveforms of the circuit after input power is applied. It shows V_O rising along with VIN once VIN forward-biases the leakage path within the ASIC. Note that output current (I_O) is negligible until V_O rises above the pre-bias voltage (point A). From hereon, the waveform of I_O exhibits a positive output current. [19]

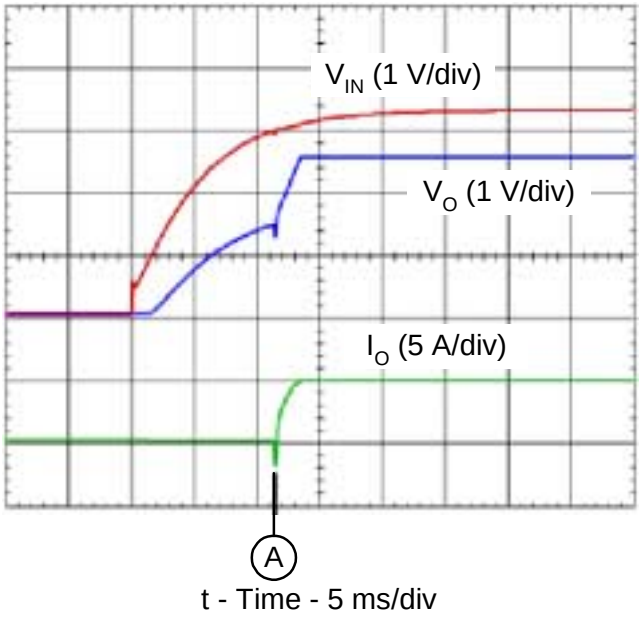


Fig. 25. Power-up waveforms with pre-bias.

B. DC-DC Controllers

Ratio-Metric Sequencing

In ratio-metric sequencing, multiple output power rails start ramping at the same time and in proportion. This function can be accomplished with multiple controllers sharing a common soft-start capacitor. The solution in Fig. 26 (waveforms in Fig. 27) is based on two TPS40051 synchronous buck controllers with a wide input voltage range of 8 V to 40 V. These controllers drive synchronous rectifiers and feature feed-forward voltage-mode control. In this example, I/O voltage is 3.3 V and core voltage is 1.8 V.

Soft-start is programmed by charging external capacitor C2 via an incorporated current source of 2.3 µA. The voltage rise on C2 is then fed into a separate non-inverting input to the error amplifier (in addition to the feedback voltage and the 700-mV reference voltage). Once voltage on C2 exceeds 700 mV, the internal reference voltage is used to establish regulation. To ensure a controlled ramp of the output voltage, the soft-start time should be greater than the output inductor and output capacitor time constant.

So, in this example,

$$t_{START} \geq 2\pi\sqrt{L1 \times C13} \quad \text{(seconds)}$$

and the soft-start capacitance calculates as:

$$C2 = 2 \times \left(\frac{2.3\ \mu A}{0.7\ V} \right) \times t_{START} \text{ (Farads),}$$

since the current feeding the soft-start capacitor is 2.3 µA per controller. [20]

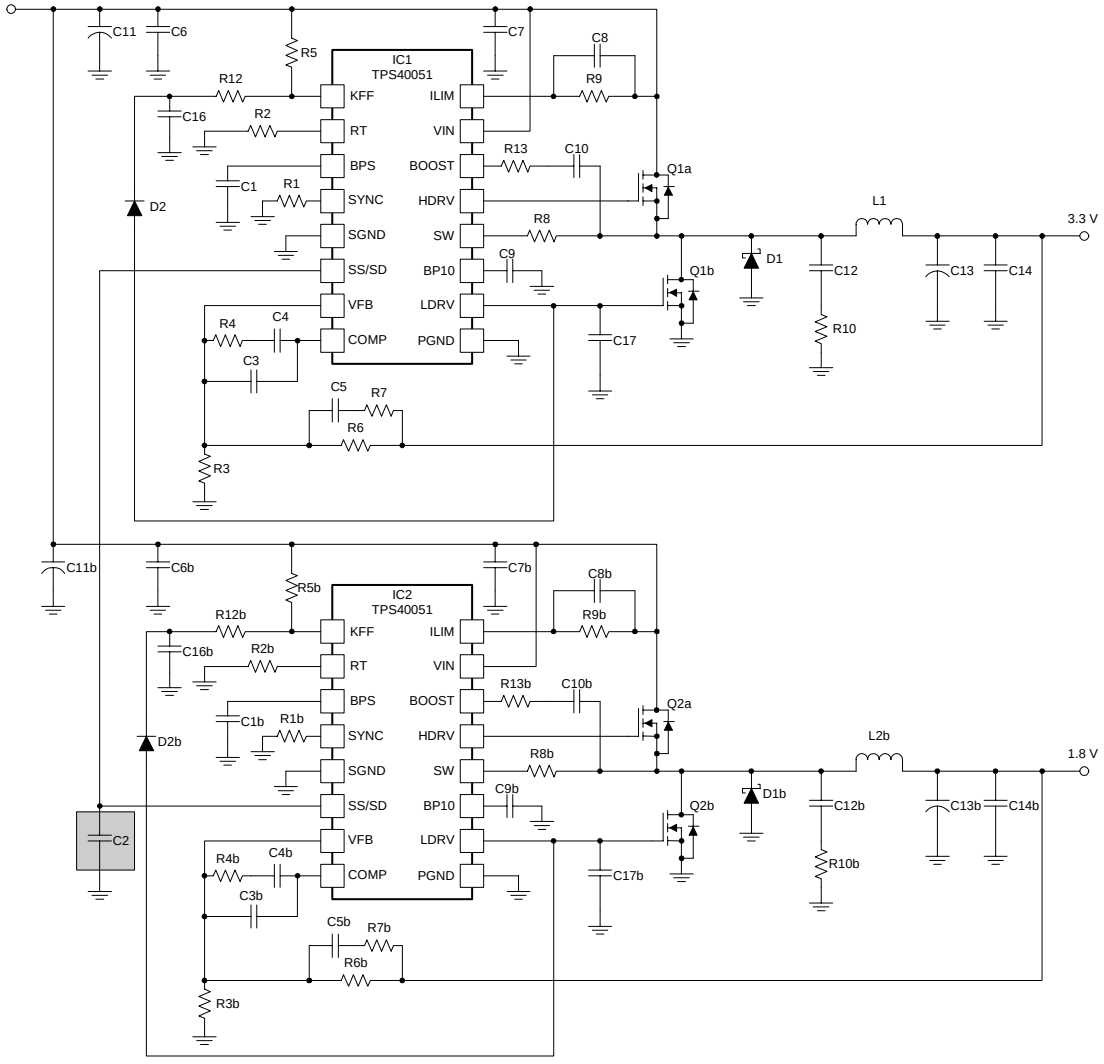


Fig. 26. Ratio-metric sequencing with common soft-start capacitor.

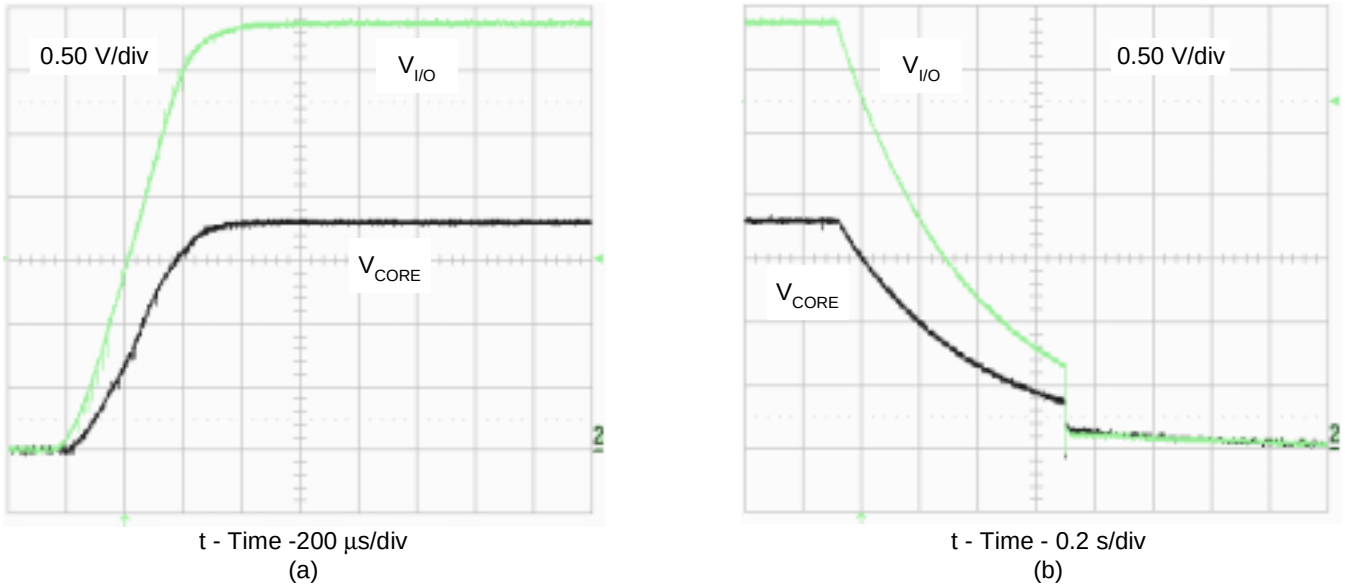


Fig. 27. Power-up (a) and power-down (b) waveforms for Fig. 26.

C. DC-DC Converters

Simultaneous Sequencing

As previously mentioned, the objective of simultaneous sequencing is to minimize the potential difference between voltage rails as they ramp. Fig. 28 illustrates such an implementation using switcher with integrated FET (SWIFT) converters that integrate both high-side and synchronous rectifier FETs. IC1 provides I/O voltage of 3.3 V, while IC2 provides core voltage of 1.5 V. The converters share one soft-start capacitor (C14) to ensure the outputs ramp at the same slope. Note that these are voltage-mode controlled converters. IC2 acts as master controller. Its output voltage is programmed at 1.5 V via voltage divider R14 and R12. Additionally, its power-good (PGOOD) comparator is used as a master flag to release the voltage divider of IC1.

During power up (Fig. 29a), both converter output voltages rise with the ramp of the soft-start capacitor to an output voltage of 1.5 V. This is due to voltage dividers R14 and R12 at IC2, and R8 and R3 at IC1. During power-up, the power good (PGOOD) pin of IC2 is active low, holding Q1 off so that the output voltages track during power up until IC2 reaches 90% of its final value. Once IC2 detects an output voltage level of 90% or greater, PGOOD goes high impedance, and pull-up resistor R4 drives the gate of Q1 on via RC network R5 and C11. Once the gate threshold voltage of Q1 reaches 1.6V (typical), it starts to conduct and switches R6 in parallel to R3. This parallel combination changes the output voltage set point of IC1 to program 3.3-V output.

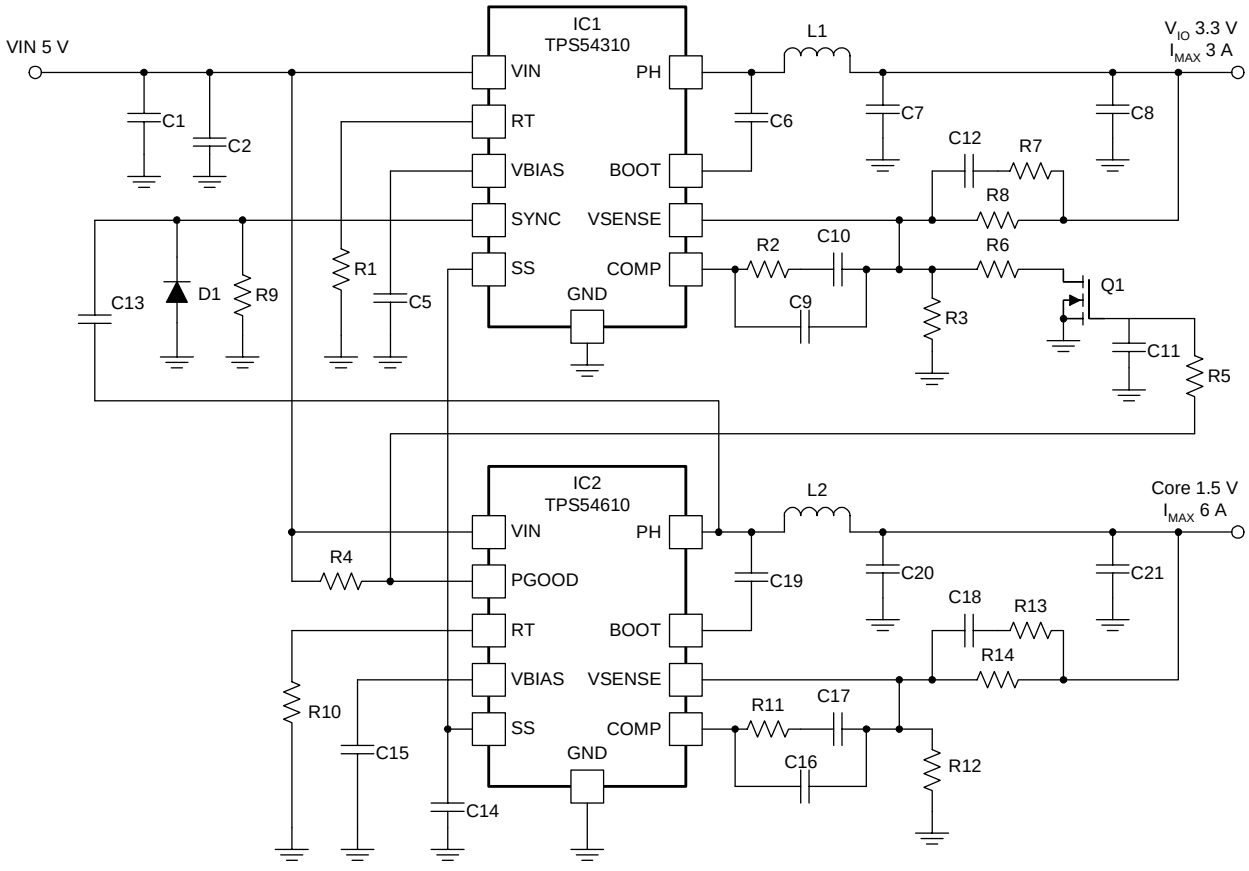


Fig. 28. SWIFT converters configured for simultaneous sequencing.

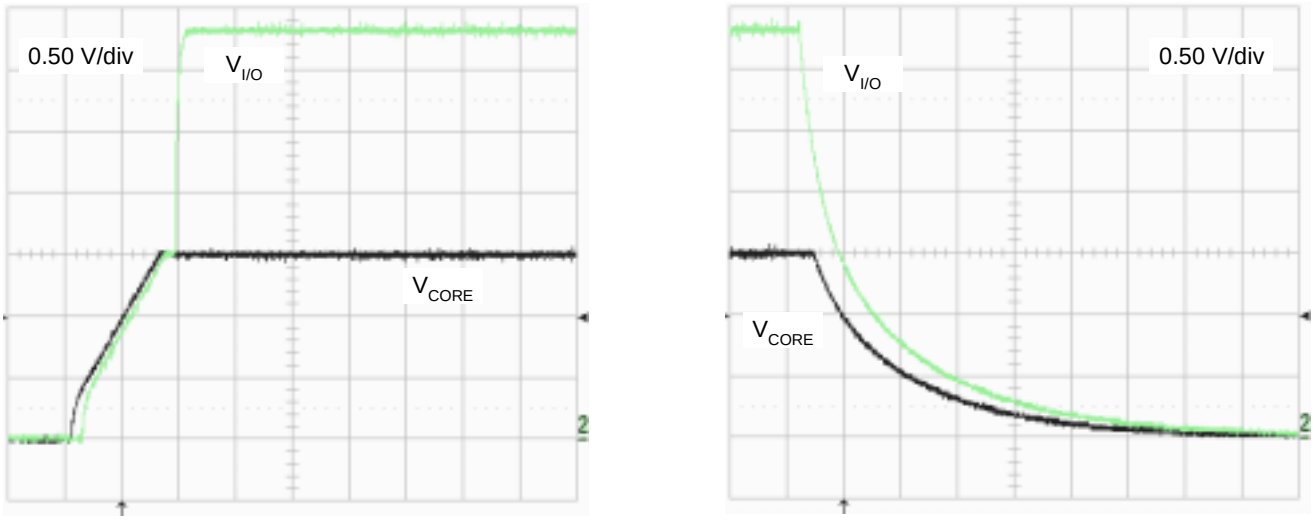


Fig. 29. Power-up (a) and power-down (b) waveforms for Fig. 28.

In this implementation, a general purpose BSS138 FET is used with a typical threshold voltage of V_{GSth} = 1.6 V. This FET features $R_{DS(on)} < 10\ \Omega$ (negligible compared to the values of R3 and R6), so does not affect the calculated output voltage set point value.

The set point resistor values can be calculated as follows:

A. Equation for V_{CORE}

$$R3 = \frac{V_{REF} \times R8}{V_{CORE} - V_{REF}}$$

V_{CORE} = 1.5 V, V_{REF} = 0.891 V

Choose R8 = 27.4 kΩ

then R3 = 40.2 kΩ

B. Equation for $V_{I/O}$

$$R_X = \frac{V_{REF} \times R_8}{V_{I/O} - V_{REF}}$$

where R_X is $R_3 \parallel R_6$

$V_{I/O}$ = 3.3 V

so R_X = 10.22 kΩ

C. Equation for R6

$$1/R_X = 1/R3 + 1/R6$$

$$\text{so, } R6 = \frac{1}{1/R_X - 1/R3}$$

R6 = 13.7 kΩ

PGOOD of IC2 transitions low when V_{CORE} falls under 90% of its initial value during power-down (Fig. 29b). This discharges C11 and the gate of Q1 via R5. Once the gate of Q1 falls below its threshold voltage level (1.6 V typical), R6 is removed from the feedback divider. Thus IC1's output voltage set point drops to 1.5 V and the I/O voltage ramps down along with the core voltage. Note during power-down the voltages do not track each other due to differing output capacitor energy storage and load levels. The tracking version of the SWIFT converters can be used to address this issue.

A noteworthy feature of this implementation is that the converters are running at the same switching frequency. IC2 is the master device programmed to a switching frequency of 700 kHz. IC1 starts at a lower initial switching frequency of roughly 630 kHz, 10% below the switching frequency of IC2. Once IC2 begins to operate, it synchronizes IC1 via the SYNC pin. Diode D1 limits negative voltage spike amplitude at the SYNC input.

Sequential Sequencing

Fig. 30 shows a dual power supply design with sequential power-up using the TPS54350 dc/dc converter. The circuit uses the power good function of the I/O supply to activate the enable of the core supply. Once the I/O supply is up and stable, the power good pin (PWRGD) transitions from active low to high impedance (see Fig. 31). The TPS54350 has an internal pull-up current source on the enable (ENA) pin, so an external pull-up resistor is not required to enable the core supply. As discussed in the last section, the challenge with using this power good and enable technique is the power-down sequence. It is preferred to power down the supply rails in the reverse order of power up. Because of supply loading and the disabling of the I/O supply and core supply at the same time, this order is not guaranteed.

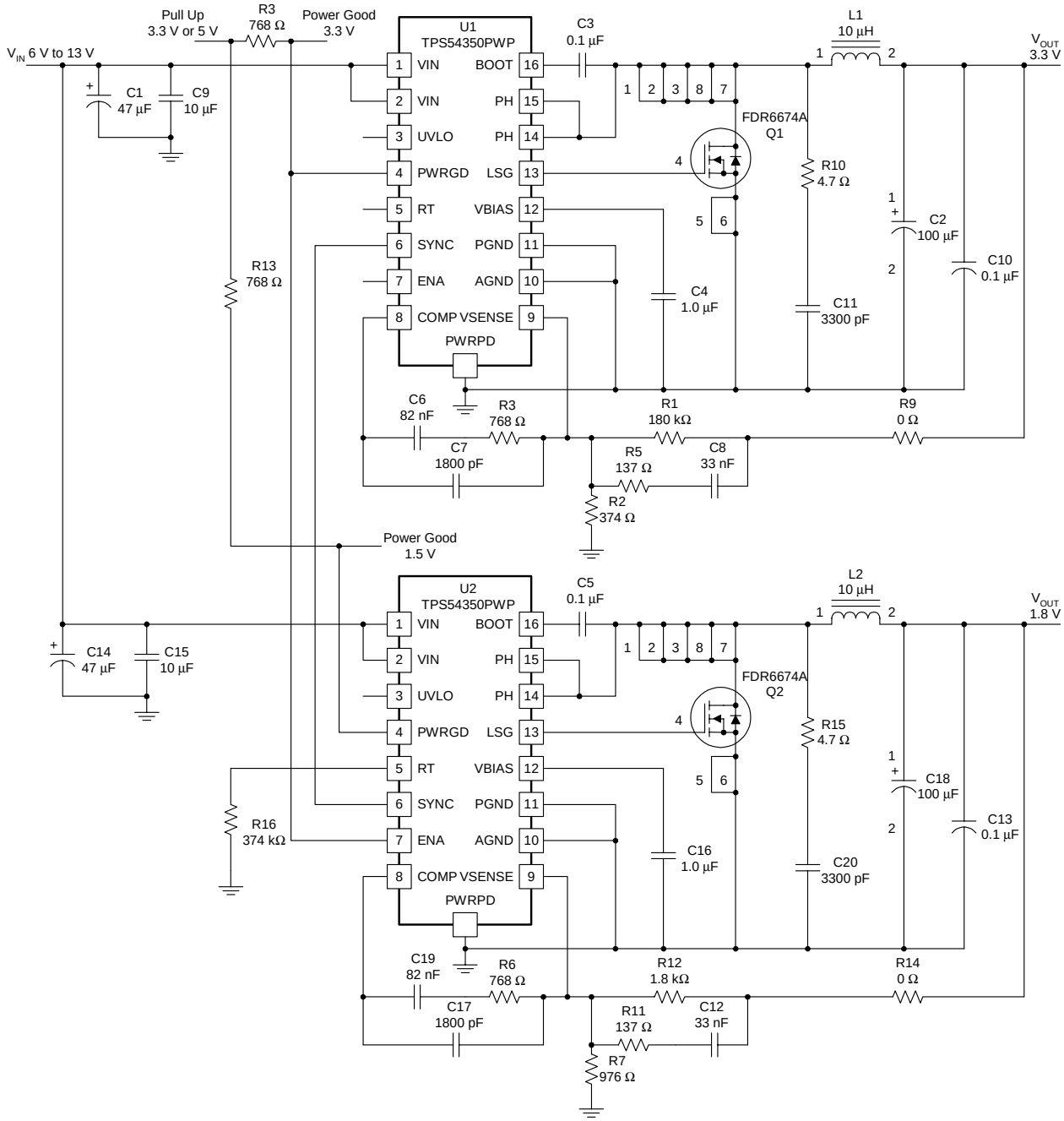


Fig. 30. Sequential sequencing with TPS54350 converters.

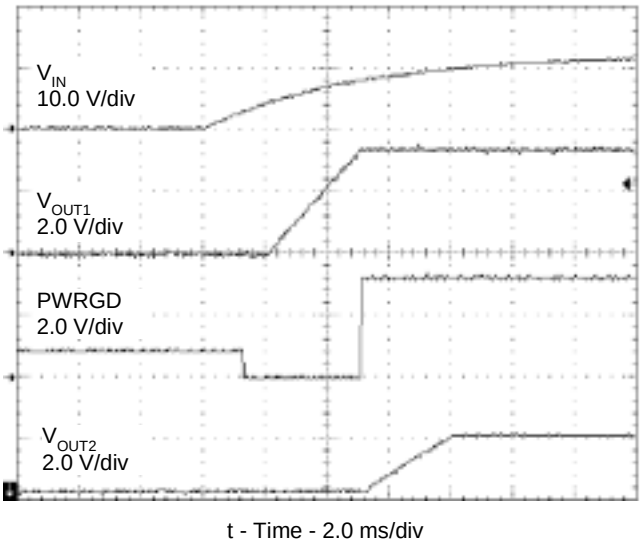


Fig. 31. Power-up waveforms of Fig. 30.

Another technique to implement sequential sequencing is implemented by connecting the power good function to the TRACKIN pin of a TPS54680 Sequencing SWIFT converter using resistors and a capacitor (Fig. 32) [10]. The TPS54680 was designed for applications that have critical power supply sequencing requirements. The device has a TRACKIN pin to facilitate the various sequencing methods. The TRACKIN pin is the input to an analog multiplexer that compares a 0.891-V internal voltage reference to the voltage on the TRACKIN pin, and connects the lower of the voltages to the non-inverting node of the error amplifier. When the TRACKIN pin voltage is lower than the internal voltage reference, the TRACKIN pin voltage is effectively the reference for the power supply. The power-up and power-down waveforms are shown Fig. 33.

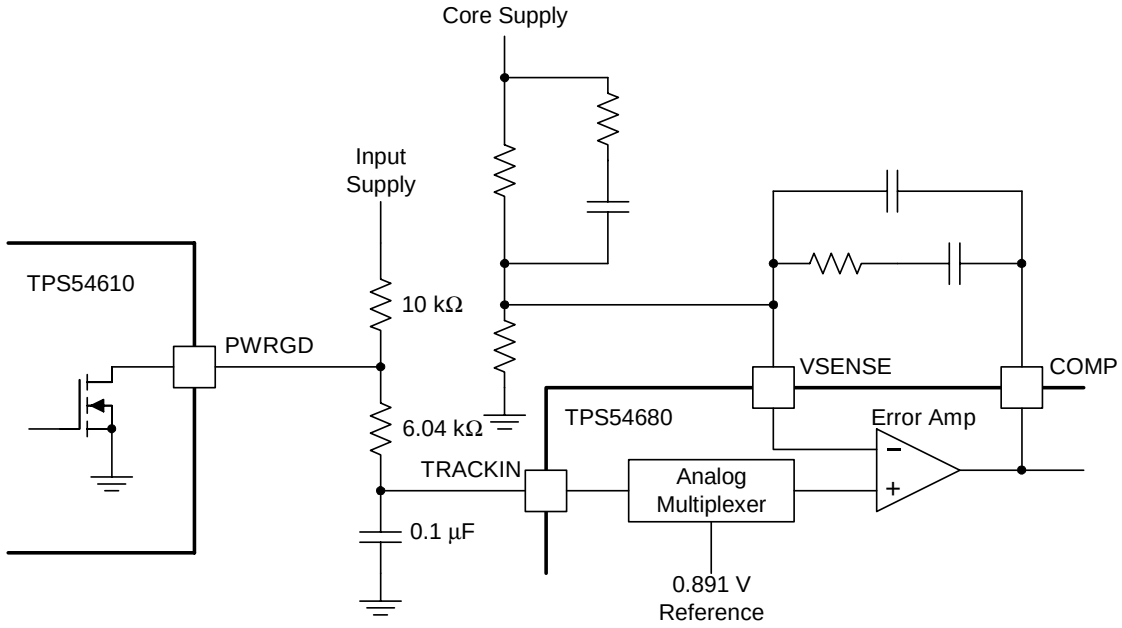
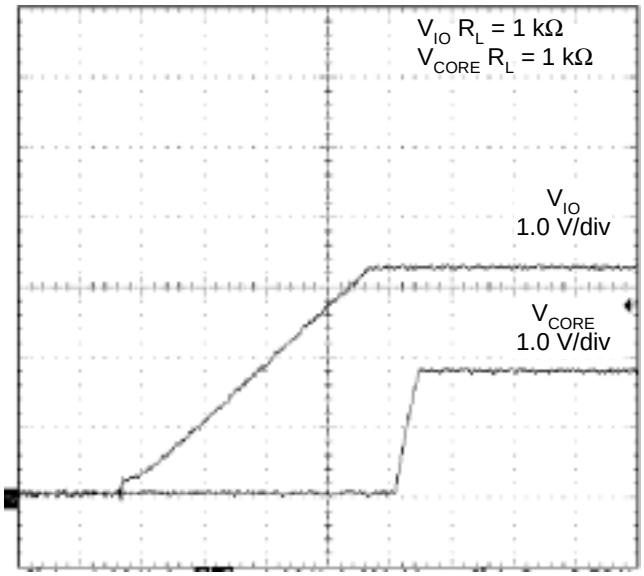


Fig. 32. Sequential sequencing with TPS54680 track input.



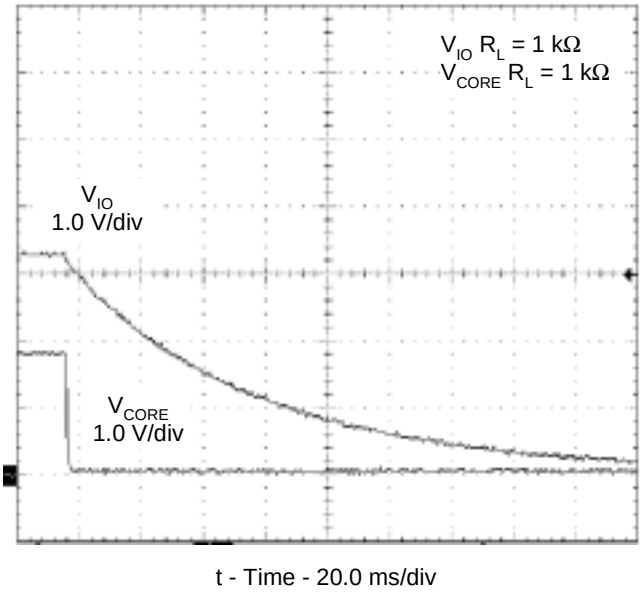


Fig. 33. Power-up (a) and power-down (b) waveforms of Fig. 32.

As shown in Fig. 33a, the 3.3-V I/O supply ramps first. When the I/O supply reaches its final 3.3-V steady state value, the open drain output of the PWRGD pin releases the TRACKIN pin, and the core supply rises at the rate of the RC time constant. The 0.1-µF capacitor is used to minimize the inrush current during startup of the core supply. The PWRGD pin asserts, pulling the TRACKIN pin low, when the SSENA pin is pulled low on the TPS54610 or when the I/O voltage is below 90% of the desired regulated voltage. Ideally, the I/O and core supplies power down in opposite order of power-up. If there is no load or a light load on the core when the I/O rail powers down, the TPS54680 device has the ability to sink current and transfers the energy stored in the output capacitor to the input capacitor. Fig. 33b shows power-down with 1-kΩ loads on both outputs.

Ratio-Metric Sequencing

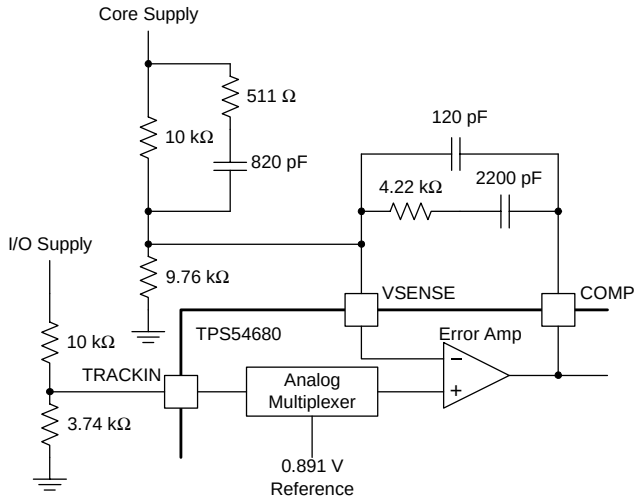
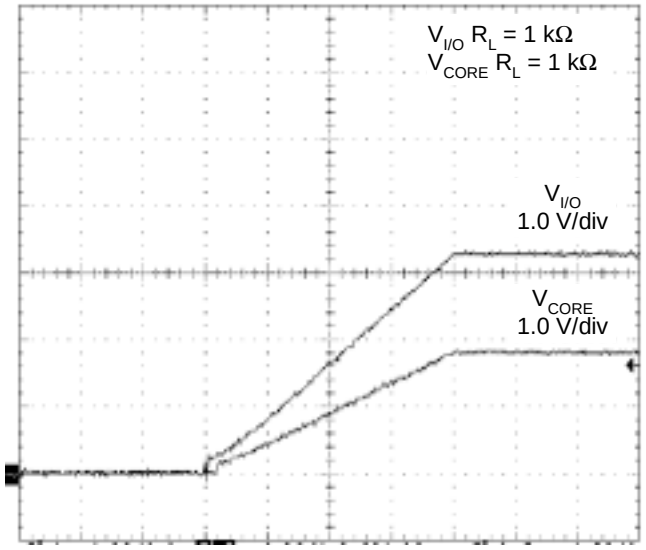
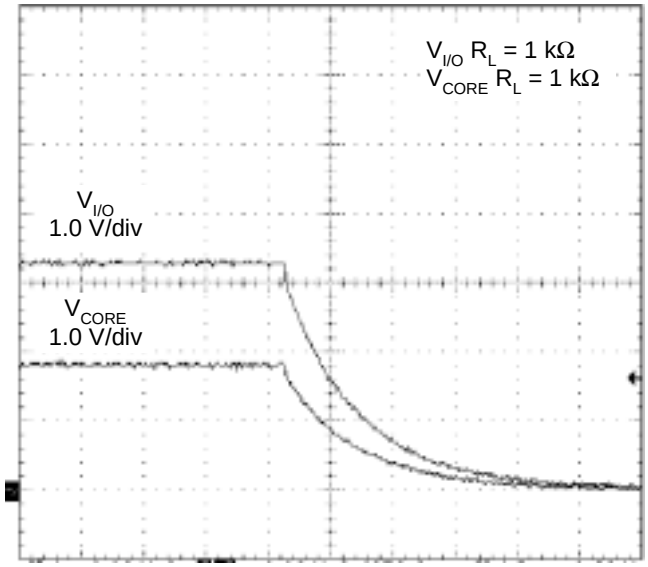


Fig. 34 Ratio-metric sequencing with TPS54680 track input.

The analog multiplexer on the TPS54680 can also provide ratio-metric power sequencing by setting the divider ratio on the TRACKIN pin to a different value than that of the feedback compensation. Fig. 34 shows a simplified schematic with the TRACKIN voltage divider set to program lower voltage than the feedback divider, resulting in the core powering-up and down in proportion to the I/O voltage. The waveforms for the core and I/O supplies are shown in Fig. 35a and 35b.



t - Time - 1.0 ms/div
(a)



t - Time - 50.0 ms/div
(b)

Fig. 35. Power-up (a) and power-down (b) waveforms of Fig. 34.

If the core supply must power up slightly before the I/O supply, the TRACKIN voltage divider ratio should be set to program higher voltage than that of the feedback divider (sample schematic and waveforms in Fig. 36 and 37). For an equation on the selection of the TRACKIN resistors see reference [10].

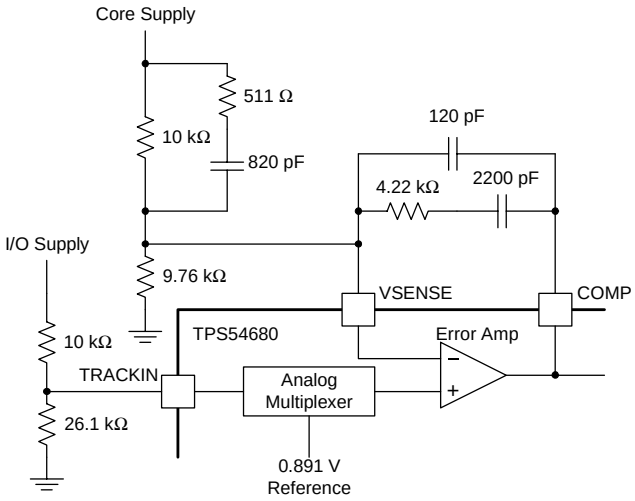


Fig. 36. Ratio-metric sequencing (core up first).

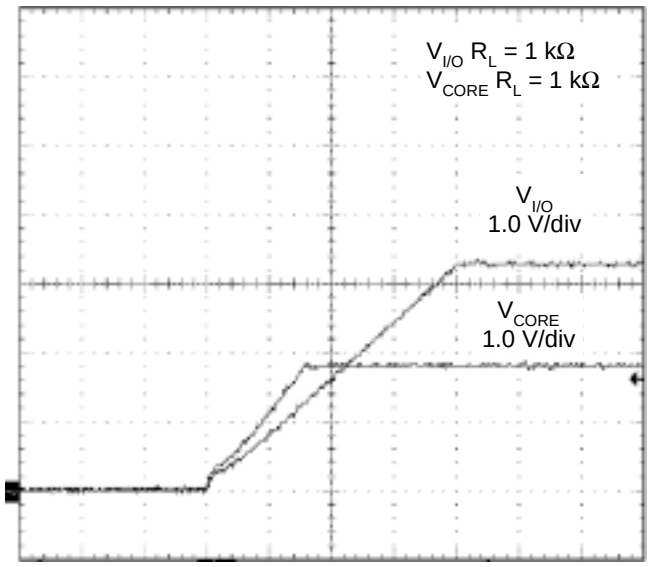


Fig. 37. Power-up (a) and power-down (b) waveforms of Fig. 36.

Simultaneous Sequencing

To minimize voltage differences between supply rails during power-up and down, the TPS54680 can be configured for simultaneous sequencing as shown in Fig. 38. By selecting the TRACKIN voltage divider to have the same ratio as the voltage divider in the feedback compensation loop, the core and I/O supplies power up and down with waveforms similar to Fig. 39. As before, the outputs of the regulators are loaded with 1-kΩ resistors. It can be observed from the waveforms that the voltage difference between the rails is minimal during power down. If the I/O supply is heavily loaded and the core supply is lightly loaded during power down, there may be a voltage difference between the rails. This is because the core supply cannot sink current as fast as the I/O supply is falling. This can be countered by adding more bulk capacitance on the I/O output.

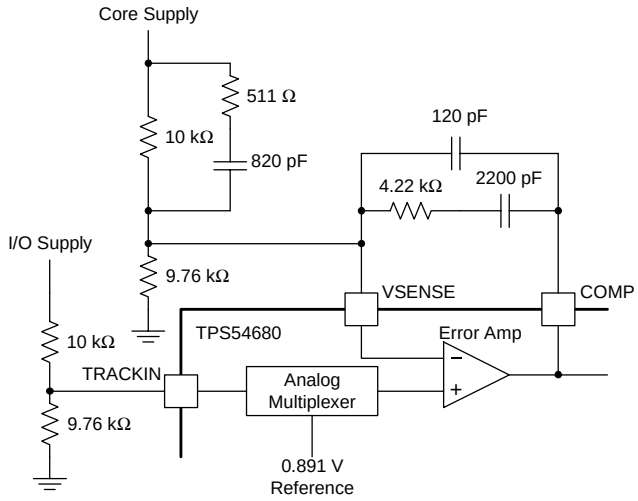


Fig. 38. Simultaneous sequencing with TPS54680 track input.

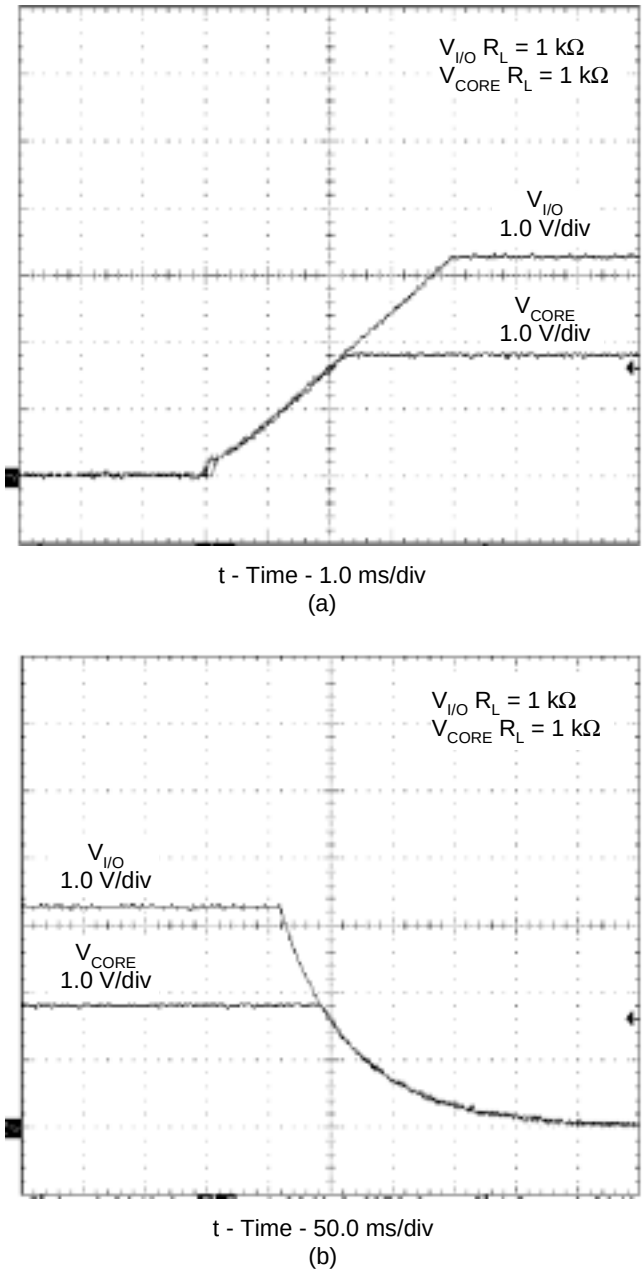


Fig. 39. Power-up (a) and power-down (b) waveforms of Fig. 38.

VI. Summary

Design of a multi-rail power system often involves much more than simply converting input voltages to output voltages and currents. As has been discussed, the power-up and power-down sequencing of these voltages can significantly impact proper system operation and reliability. Three distinct power sequencing schemes have been defined (sequential, ratio-metric and simultaneous) and implementations have been illustrated with a breadth of power devices, ranging from LDOs to PWM controllers and converters to power modules. We've also enlisted control and monitoring devices including supply voltage supervisors and a microcontroller. Of course, these devices can be applied in combination as needed to meet the power sequencing requirements of any given system.

VII. Acknowledgements

The authors wish to thank Joe DiBartolomeo and Chris Thornton for their generous contributions to this work.

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[20] TPS40051 Data Sheet, (SLUS540), Texas Instruments

APPENDIX A
LIST OF MATERIALS FOR FIG. 9.

Reference	Count	Description	Manufacturer	Part Number
IC1	1	LDO, 1.80 V, 1.0 A	TI	TPS79618KTT
IC2	1	LDO, 3.3 V, 1.5 A	TI	TPS78633KTT
IC3	1	SVS	TI	TPS3106K33
C1, C2	2	Capacitor, POSCAP, 100 µF, 10 V, 55 mΩ, 20%, 7343	Sanyo	10TPB100M
C3, C6	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 1210	MuRata	GRM31CR60J106KC01
C4	1	Capacitor, ceramic, 100 nF	Std	Std
C5	1	Capacitor, ceramic, 0.47 µF	Std	Std
R1, R5	2	Resistor, chip, 100 kΩ, 1/16 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 7.5 Ω, 1/16 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 23.2 kΩ, 1/16 W, 1%, 805	Std	Std
R4	1	Resistor, chip, 11 kΩ, 1/16 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 100 Ω, 1/16 W, 1%, 805	Std	Std
Q1	1	P-channel, FET, -12 V, -3 A, SOT-23.	Vishay	Si2333DS

APPENDIX B
LIST OF MATERIALS FOR FIG. 12.

Reference	Count	Description	Manufacturer	Part Number
IC1, IC2	2	IC, LDO Regulator, Available in 1.80-V, 2.5-V, 2.8-V, 3-V, 3.3-V and Adjustable , 1 A, ultralow noise, high PSRR, T0-263	TI	TPS79601KTT
IC3, IC4	2	Single 2.7-V High-Slew-Rate Rail-to-Rail Output Operational Amplifier w/Shutdown , SOT-23	TI	TLV2770CDGKR
CIN1, CIN2	2	Capacitor, POSCAP, 100 µF, 10 V, 55 mΩ, 20%, 805	Murata	GRM21BR60J225KC01
COUT1, COUT2	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 805	Murata	GRM21BR60J225KC01
Q1	1	BSS 138, N-channel enhancement, SOT-23	Fairchild Semiconductor	BSS128
D2	2	Small signal diode, LL-34	Fairchild Semiconductor	1N4148
D3	1	Shottky barrier rectifiers, DPAK	On Semi-conductor	MBRD320-D
C1, C2, C3, C4, C5	5	Capacitor, ceramic, 100 nF, X7R, 10%	Std	Std
R1, R5	2	Resistor, chip, 31.6 kΩ, 1/16 W, 1%, 805	Std	Std
R2	1	Resistor, chip, 30.1 kΩ, 1/16 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 300 kΩ, 1/16 W, 1%, 805	Std	Std
R4, R7	2	Resistor, chip, 4.99 kΩ, 1/16 W, 1%, 805	Std	Std
R6	1	Resistor, chip, 140 kΩ, 1/16 W, 1%, 805	Std	Std

APPENDIX C
LIST OF MATERIALS FOR FIG. 26.

Reference	Count	Description	Manufacturer	Part Number
C1, C7, C10, C1b, C7b, C10b	6	Capacitor, ceramic, 0.1 µF, 25 V, X7R, 10%, 805	Vishay	VJ0805Y104KXXAT
C11, C11b	2	Capacitor, aluminum, 100 µF, 63 V, 20%	Panasonic	EEVFK1J101P
C13, C13b	2	Capacitor, POSCAP, 330 µF, 6.3 V, 10 mΩ, 20%, 7343D	Sanyo	6TPD330M
C14, C14b	2	Capacitor, ceramic, 1 µF, 16 V, X5R, 20%, 805	TDK	C2012X5R1C105KT
C16, C16b	2	Capacitor, ceramic, 470 pF, 50 V, X5R, 20%, 805	Vishay	VJ0805Y471KXAAT
C2, C12, C17, C2b, C12b, C17b	6	Capacitor, ceramic, 2.2 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y222KXAAT
C3, C3b	2	Capacitor, ceramic, 82 pF, 50 V, NPO, 5%, 805	Panasonic	VJ0805A820KXAAT
C4, C4b	2	Capacitor, ceramic, 2.7 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y272KXAAT
C5, C5b	2	Capacitor, ceramic, 10 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y103KXAAT
C6, C6b	2	Capacitor, ceramic, 1.5 µF, 50 V, X7R, 10%, 1210	TDK	C3225X7R1H155KT
C8, C8b	2	Capacitor, ceramic, 100 pF, 50 V, X7R, 10%, 805	Vishay	VJ0805A101KXAAT
C9, C9b	2	Capacitor, ceramic, 1 µF, 16 V, X7R, 10%, 805	Vishay	C2012X5R1C105KT
D1, D1b	2	Diode, schottky, 1 A, 60 V, 45600	IR	10BQ060
D2, D2b	2	Diode, switching, 10 mA, 85 V, 350 mW, SOT-23	Vishay-Liteon	BAS16
L1, L2b	2	Inductor, SMT, 22 µH, 4.5 A, 34 mΩ, 0.85 ξ 0.59	Coiltronics	UP4B-220
Q1, Q2	2	MOSFET, dual N-channel, 60 V, 3.8 A, 55 mΩ, SO-8	Siliconix	Si946EY
R1, R1b	2	Resistor, chip, 1 kΩ, 1/10 W, 1%, 805	Std	Std
R10, R10b	2	Resistor, chip, 4.7 Ω, 1 W, 5%, 2512	Std	Std
R11, R11b	2	Resistor, chip, 20 Ω, 1/10 W, 1%, 805	Std	Std
R12, R12b	2	Resistor, chip, 243 kΩ, 1/10 W, 1%, 805	Std	Std
R13, R13b	2	Resistor, chip, 8.2 Ω, 1/10 W, 5%, 805	Std	Std
R2, R2b	2	Resistor, chip, 165 kΩ, 1/10 W, 1%, 805	Std	Std
R3	1	Resistor, chip, 2.1 kΩ, 1/10 W, 1%, 805	Std	Std
R3b	1	Resistor, chip, 4.99 kΩ, 1/10 W, 1%, 805	Std	Std
R4, R4b	2	Resistor, chip, 30.1 kΩ, 1/10 W, 1%, 805	Std	Std
R5, R5b	2	Resistor, chip, 71.5 kΩ, 1/10 W, 1%, 805	Std	Std
R6, R6b	2	Resistor, chip, 7.87 kΩ, 1/10 W, 1%, 805	Std	Std
R7, R7b	2	Resistor, chip, 100 Ω, 1/10 W, 1%, 805	Std	Std
R8, R8b	2	Resistor, chip, 3.3 Ω, 1/10 W, 5%, 805	Std	Std
R9, R9b	2	Resistor, chip, 20 kΩ, 1/10 W, 1%, 805	Std	Std
IC1, IC2	2	Wide Input Synchronous Buck Controller	TI	TPS40051PWP

APPENDIX D
LIST OF MATERIALS FOR FIG. 28

References	Count	Description	Manufacturer	Part Number
C1	1	Capacitor, aluminum, 470 µF, 6.3 V, 20%, 140CLH series, 1010	BC Components	2222 140 95301
C2, C4	2	Capacitor, ceramic, 10 µF, 6.3 V, X5R, 20%, 1206	muRata	GRM319 R6 0J 106K
C7, C8, C20, C21	4	Capacitor, ceramic, 47 µF, 6.3 V, X5R, 20%, 1210	muRata	GRM42-2 X5R 476K
C3, C14	2	Capacitor, ceramic, 39 nF, X7R, 10%, 603	Std	Std
C6, C19	2	Capacitor, ceramic, 47 nF, X7R, 10%, 603	Std	Std
C9, C11	2	Capacitor, ceramic, 470 pF, X7R, 10%, 603	Std	Std
C10	1	Capacitor, ceramic, 6.8 nF, X7R, 10%, 603	Std	Std
C12	1	Capacitor, ceramic, 1.8 nF, X7R, 10%, 603	Std	Std
C13	1	Capacitor, ceramic, 56 pF, X7R, 10%, 603	Std	Std
C5, C15	2	Capacitor, ceramic, 100 nF, X7R, 10%, 603	Std	Std
C16	1	Capacitor, ceramic, 1.5 nF, X7R, 10%, 603	Std	Std
C17	1	Capacitor, ceramic, 18 nF, X7R, 10%, 603	Std	Std
C18	1	Capacitor, ceramic, 5.6 nF, X7R, 10%, 603	Std	Std
R1	1	Resistor, chip, 76.8 kΩ, 1/16 W, 1%, 603	Std	Std
R2	1	Resistor, chip, 3.83 kΩ, 1/16 W, 1%, 603	Std	Std
R3	1	Resistor, chip, 40.2 kΩ, 1/16 W, 1%, 603	Std	Std
R4, R5	2	Resistor, chip, 330 kΩ, 1/16 W, 1%, 603	Std	Std
R6	1	Resistor, chip, 13.7 kΩ, 1/16 W, 1%, 603	Std	Std
R7	1	Resistor, chip, 105 Ω, 1/16 W, 1%, 603	Std	Std
R8	1	Resistor, chip, 27.4 kΩ, 1/16 W, 1%, 603	Std	Std
R9	1	Resistor, chip, 1 kΩ, 1/16 W, 1%, 603	Std	Std
R10	1	Resistor, chip, 71.5 kΩ, 1/16 W, 1%, 603	Std	Std
R11	1	Resistor, chip, 1.43 kΩ, 1/16 W, 1%, 603	Std	Std
R12	1	Resistor, chip, 14.7 kΩ, 1/16 W, 1%, 603	Std	Std
R13	1	Resistor, chip, 33.2 Ω, 1/16 W, 1%, 603	Std	Std
R14	1	Resistor, chip, 10 kΩ, 1/16 W, 1%, 603	Std	Std
IC1	1	Low Input Voltage 3-A Buck Converter, PWP	TI	TPS54310PWP
IC2	1	Low Input Voltage 6-A Buck Converter, PWP	TI	TPS54610PWP
Q1	1	Bipolar Small Signal, NPN, 50 V, 22 mA, 3.5 Ω, SOT-23	Infineon	BSS138
D1	1	Diode, 100 V, 200 mA, SOT-23	Fairchild	MMBD4148
L1, L2	2	Inductor, CEP125, 7.2 µH, 7.8 A, 14 mΩ, 12.5x12.5 mm	Sumida	CEP125-H-7R2

Topic 3

Design Review: A Step-by-Step Approach to AC Line-Powered Converters

Texas Instruments

Design Review: A Step-By-Step Approach to AC Line-Powered Converters

Ed Walker

ABSTRACT

An offline, three-output, 150-W forward converter is used as an example to illustrate the design process for typical isolated converters. This example emphasizes the basics with a double-ended forward topology using coupled inductors for output accuracy. Design issues and trade-off decisions to optimize power efficiency while keeping costs to a minimum are highlighted. Finally, the presentation of measured performance results confirms the design process.

I. INTRODUCTION

One of the most common power supplies today plugs into the AC wall outlet and provides an isolated single or multiple DC voltage output. While designing this power supply may seem elementary, there are many criteria to consider in order to achieve a well-designed system. And if the power supply is not designed properly, it may well attract too much attention by not working.

An offline design can be made easier if some initial conditions are first established. Since the power supply is the heart of the system, the designer must work with the project engineers to determine the power supply requirements, operating environment, cost, and development schedule.

The designer can then proceed with a "plan of record" and begin establishing the details. This plan of record should include a power supply specification agreed upon by the project team.

II. OVERVIEW

A. *Defining Requirements*

The first step is to define the load. This is an important step, enabling the proper choice of topology, components, and many other details. Output ripple and tolerance are critical to system performance. The output current for each load determines the power requirements, and how that current may vary influences regulation and noise on all outputs.

Load Concerns

- Output voltage(s), tolerance(s) and allowed ripple
- Output current(s), maximum and minimum.
- Transient loading on outputs, di/dt, repetition rate.
- Load capacitance, wiring inductance
- Sequencing of supplied voltages
- Protection features

Input for an offline converter power supply depends upon the countries in which the power supply operates. Input voltage ranges help define the topology, component ratings, and safety certifications. AC line harmonic requirements may require power-factor correction.

Power Train Concerns

- Input voltages for required countries. (Is a 110 V/220 V switch an option?)
- Possible need for power factor correction
- Topology selection
- Control method

And finally, safety and EMI requirements determine the mechanical design, which in turn determines airflow and component temperature. Once all is understood, then the designer can estimate a cost and create a development schedule.

TABLE 1. POWER SUPPLY TOPOLOGY SUMMARY

Topology	Power Level	Benefits	Drawbacks	Cost
Flyback	<100 W	Low parts count Single magnetic Wide input-voltage range Low output power	Poor efficiency at high power levels High peak currents Cross regulation problems High-voltage power switch	Lowest
1 Switch Forward	100 W to 500 W	Medium output power Good cross regulation with coupled inductor Potential for >50% duty-cycle	Limited input range Power Switch = 2 V_{IN} Transformer reset	Moderate
2 Switch Forward	100 W to 500 W	Medium output power Power switch = V_{IN} Coupled inductor Clamped transformer reset	Limited input range Top FET drive circuit required 50% duty-cycle limit Larger inductor value	Moderate
Half-Bridge	100 W to 500 W	Medium output power Power switch = V_{IN} Coupled inductor Max duty-cycle < 100%	Limited input range Top FET drive Volt-second balance of transformer Center-tapped secondary	Moderate
Full Bridge	>500 W	Resonant switching can improve efficiency Power switch = V_{IN} Coupled inductor Very high output power Max duty-cycle < 100% Efficient transformer design	4 power switches Top FET drive Volt-second balance	High
Push-Pull	25 W to 200 W	Good core utilization Coupled inductor Both switches ground referenced Small output inductor Max duty-cycle < 100%	Power switch = 2 V_{IN} Limited input range Center-tapped primary Volt-second balance	Moderate

B. Defining the Topology

There are many possible topologies to consider, including flyback, forward, half bridge, full bridge and push-pull. All have general areas of optimization. Table I summarizes the choices.

C. Defining the Input Configuration

The power supply input, commonly called the "front end" of an offline supply, has several components:

- line cord/receptacle
- power switch
- fuse
- inrush limiting NTC thermistor (SEM-100)
- EMI filter (SEM-1500),
- input bridge (full wave or voltage doubler)
- bulk capacitance (SEM-100)

There is a wide range of input voltages to consider for worldwide operation and tolerances (usually ±10%) must be included! The peak working voltage maximum at the input to the converter is $V_{RMS} \times \sqrt{2}$.

TABLE 2. WORKING VOLTAGES

Area	V_{RMS} (typ)	± 10%	Working Voltage (V_{DC})
Japan	100	90 to 110	126 to 154
US	120	108 to 132	151 to 184
Europe	220	198 to 242	277 to 339
Australia/India	230	207 to 264	289 to 370

The range for a universal input power supply is then 90 V_{RMS} to 264 V_{RMS}. Wide ranging operation without a line-select switch is possible at power levels less than 100 W. While it may be technically possible to operate above 100 W over the wide input-voltage range, circuit losses and

limitations that increase cost usually dictate a 110 V/220 V switch (Fig. 1) to select a full-wave bridge or voltage-doubler configuration. When closed, the switch enables the circuit to double the 110 V/120 V input, thus making the DC working voltage approximately the same as it would be for 220 V/230 V input with the switch open.

TABLE 3. BULK RECTIFIED DC VOLTAGE

With Only Full Wave Bridge (V_{DC})	With Doubler for Low Range (V_{DC})
126 to 154	252 to 308
151 to 184	302 to 368
277 to 339	277 to 339
289 to 370	289 to 370

Thus the DC input range is usually considered to be 252 V_{DC} to 370 V_{DC}.

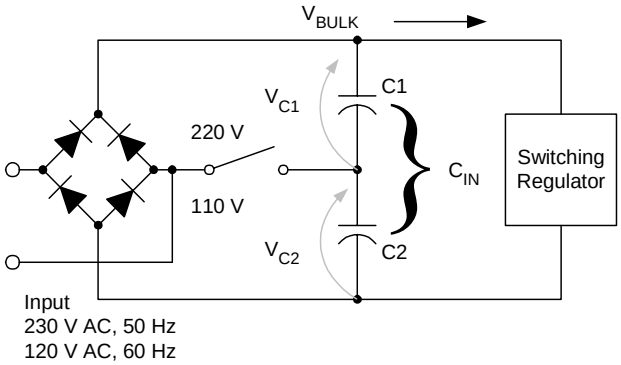

Fig. 1. A voltage doubling input range switch configuration.

D. Transformer Design

After the topology and input configuration are chosen, the transformer is considered. Each topology has different areas of concern that affect the design. Flyback designs may operate in continuous or discontinuous conduction mode, which has an impact on duty cycle and turns ratios. Forward-converter design turns ratios are determined by the input and output voltage ratios. Each has similar core and winding loss considerations

E. Voltage-Mode or Current- Mode Control

There are advantages to both peak current-mode and voltage-mode control in converter design. Average current-mode is seldom used in isolated converters, since it requires a continuous signal usually associated with the current in the output inductor.

The advantages of peak current-mode control include fast response to input variations, inherent current limiting and easier loop compensation. However, voltage-mode control does not have the limitations of minimum load and leading-edge spike that current mode has. That advantage allows stable operation at light loads and is one reason some offline converters requiring large load variances may use voltage-mode control. Also, voltage-mode does not require a current-sense element that may increase the cost. However it is always desirable to have primary-current protection in an offline converter. Since the working DC bulk voltage is on the order of 340 V_{DC}, there is a large amount of primary power available. For this reason, voltage mode PWM's may have added protective features such as voltage feed-forward, current sense, duty-cycle clamp, and volt-second clamps to limit the input power. [2]

F. Output Filter Design

A flyback output filter in its simplest form is simply a storage capacitor which must handle the high charge currents during the flyback period, and also support the entire output during the primary on-time. Designers often add an L-C filter after the first capacitor in order to reduce the high-frequency ripple voltage caused by the high peak current.

A forward converter output filter consists of an inductor (that acts as a current source and averages the secondary winding voltage) followed by a capacitor for storage. The capacitor only sees the ripple current of the inductor and does not need to support the output during the primary on-time.

Both flyback and forward converter specifications must detail the output ripple voltage and the allowable regulation window. A load-step variation on an output causes its output to drop by the resistive effects, output inductance, and loop response time. The load step should be defined in the specification together with the limits of allowable output voltage variation.

III. The Design Process

A simple three-output, 150-W, universal input powered supply is selected to illustrate the design process. This type of power supply is found in many home personal computers, but the description that follows should be helpful for a wide range of similar applications and at different power levels.

A. Defining the Requirements (Plan of Record)

The official power-supply specification document contains the details of what the supply is intended to do. The minimum requirements for this example are:

- 3 outputs required
  - +5 V (±5%) at 18 A (90 W), 5 A typical, 2 A minimum, 3-A load step.
  - +3.3 V (±5%) at 5 A (16.5 W), 2.5 A typical, 1 A minimum, 1-A load step.
  - +12 V (±10%) at 3 A (36 W), 2 A typical, 1 A minimum, 2 A load transient.
- Total maximum power output = 144 W
- Typical power output = 60 W (Typical values reflect a standard configuration.)
- Minimum output power = 25 W
- Efficiency ≥ 80%
- Ripple voltage = 1% p-to-p V_{OUT}, for 5 V and 3.3 V
- Ripple voltage = 2% p-to-p V_{OUT} for 12 V
- Input voltage: Worldwide AC operation, 50/60Hz, voltage select switch acceptable, no power factor required
- Safety approvals: EN 60950, UL, CSA
- EMI: FCC CLASS B, CISPR22
- Frequency <140 kHz for EMI considerations: use 100 kHz

B. Defining the Topology and Control Method

Because the cost benefits of a flyback design begin to diminish at power levels above 100 W, a forward topology appeared an optimal choice particularly in consideration of the savings that a coupled inductor might offer when multiple outputs are required. A single switch or two-switch forward converter are good candidates and either can be implemented at this power level with lower costs that either the half-bridge or the full-bridge.

A single-switch forward converter is usually limited to a 50% duty cycle to allow time for the transformer to reset its volt-second product. In a single-switch design, a reset winding is commonly used to clamp the reset voltage to acceptable levels. The power FET then sees approximately $2\times V_{IN}$. At high input this voltage can exceed 740 V (1000 V likely), leading to an 800-V FET minimum. Push-pull designs also have the problem of at least $2\times V_{IN}$ voltage rating. Since this requirement can be expensive, an alternative "double-ended" approach is preferable.

A two-transistor forward design (as shown in Fig. 2) uses a FET at each end of the transformer primary to connect to the positive rail and ground. When they turn off during the reset period, each end of the primary winding *automatically* traverses to the opposite rail, thus placing the opposite polarity on the winding to satisfy the volt-second equalization. No clamp winding is needed, and instead, only clamping diodes are required. This means that each power-FET can now be rated at the positive rail voltage of 370 V, allowing use of a pair of much less expensive 500-V FETs.

The potential cost saving (per Digi-key 1-k pricing) is shown in Table IV:

Table 4. Power FET Price Comparison

Part	Current (A)	Voltage (V)	Resistance (Ω)	Price ($)
IRF840	8	500	0.85	0.91
IRFPG50	6	1000	2.00	3.98

A two-switch forward design is a reasonable approach for this power level, considering efficiency and cost goals. Its clamped transformer voltage operation, with a maximum duty cycle of 50%, allows easy reset of the transformer core and allow lower-voltage FETs to be used in the power stage.

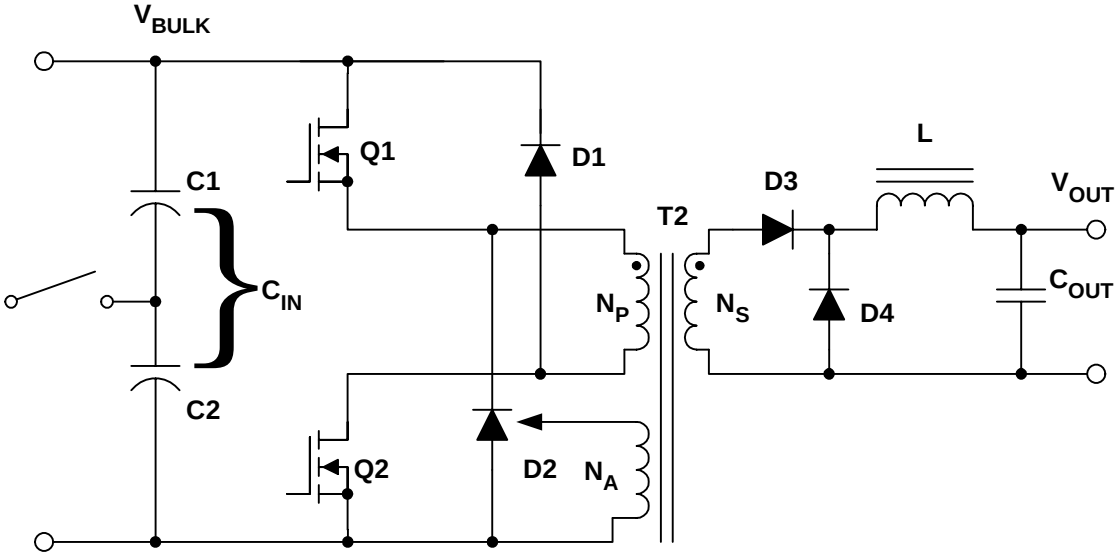

Fig. 2. Two-Switch Forward Converter

The load ratio of 144 W/25 W is 6:1, so at the minimum load there is still enough current ramp for a quality signal into the PWM comparator. This signal allows current-mode control, which includes three advantages: (1) compensation of the output L-C double-pole; (2) input feed-forward; and (3) primary pulse-by-pulse current limit.

C. Defining the Input Section

Voltage Doubler vs. Full-Wave Bridge Input

The justification for the voltage doubler is substantiated by examining the impact of a wide input voltage range on the voltage ratings required for the semiconductors, most notably at the outputs. This analysis starts at the main 5-V output and works backwards to the input, because the control loop is closed on the 5-V output since it is also the highest current output. Allowing for a schottky diode drop in the output stage (0.6 V), this design requires 5.6 V at the transformer output. The duty cycle is 50% maximum (use 45% for margin) at low-line input from which a minimum secondary voltage is derived.

$$V_{SEC(\min)} = \frac{V_{OUT}}{Duty(\max)} = \frac{5.6\,V}{0.45} = 12.44V$$

The estimate of maximum secondary voltage is determined by the ratio of input voltage to V_{SEC}. Without the doubler, a standard AC input bridge produces:

$$V_{DC(\min)} = 90V_{RMS} \times 1.4 = 126\,V(peak)$$

$$V_{DC(\max)} = 264V_{RMS} \times 1.4 = 370\,V(peak)$$

$$V_{SEC(\max)} = \frac{V_{DC(\max)}}{V_{DC(\min)}} \times V_{SEC(\min)} = \frac{370}{126} \times 12.44$$

$$= 36.5V \;\; (with \;\; 2\times derating, 80\,V\; diode\, required)$$

The following equations estimate the maximum secondary voltage using the input voltage doubler with the doubler switch closed for 110-V operation and open for 220-V operation:

$$V_{DC(\min)} = 90V_{RMS} \times 2 \times 1.4 = 255\,V(peak)$$

$$V_{DC(\max)} = 132V_{RMS} \times 2 \times 1.4 = 370\,V(peak)$$

Calculate the lower value for 220-V operation with doubler OFF using (220-10%) = 198 for $V_{DC(min)}$:

$$V_{DC(\min)} = 198 \times 1.4 = 277\,V(peak)$$

Calculate the upper value for 220-V operation with doubler OFF using (200+10%) = 264 for $V_{DC(max)}$.

$$V_{DC(\max)} = 264V_{RMS} \times 1.4 = 370\,V(peak)$$

$$V_{SEC(\max)} = \frac{V_{DC(\max)}}{V_{DC(\min)}} \times V_{SEC(\min)} = \frac{370}{255} \times 12.44\ V = 18.0V$$

$(with\ 2\times derating\ only\ a\ 40\ V\ diode\ is\ required)$

An 80-V, 30-A dual schottky diode typically costs substantially more than a 40-V device. The same premium can generally be applied to the rectifiers for the other two outputs.

TABLE 5. DIGIKEY 1-K PIECE PRICING

Part	Current (A)	Voltage (V)	Price ($)
IR 30CPQ040	30	40	1.83
IR 30CPQ080	30	80	2.93

Other concerns that may increase cost when not using the doubler are

- increased flux density in the transformer due to lower number of primary turns required to meet the Vsecondary minimum at low AC input, resulting in a more expensive and possibly larger core
- larger output inductor value due to the longer off time caused by low duty cycle at high AC input
- higher snubber losses due to higher voltages in the secondary at high AC input
- higher current ratings due to higher primary current at low AC input

When all is considered, it is desirable to design with the doubler switch for 110-V AC operation.

Input Capacitors

SEM-100 Topic 1. [3] provides the guidelines for sizing the input capacitors,

The key concern is the DC voltage decay during the time the input rectifier is not conducting (see Fig. 3). The value of the input capacitor helps reduce the voltage drop, but at the cost of a physically larger capacitor. The final lowest decayed voltage, V_{MIN} must be used as the minimum voltage to calculate the transformer turns ratios. A common standard is a ripple voltage ($V_{PK} - V_{MIN}$) 20% to 30% of the V_{PK}. The design process is the following:

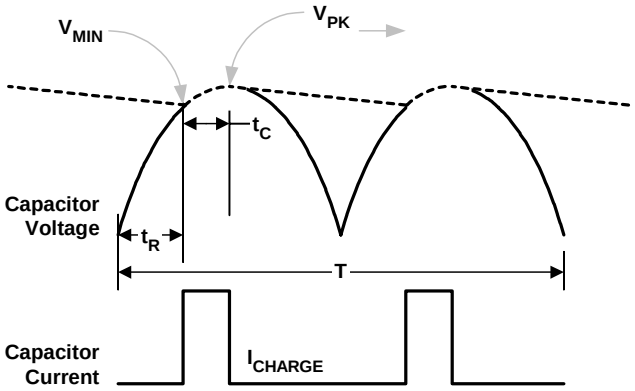

Fig. 3. Input Capacitor Waveforms

Calculate the input power required.

$$P_{IN} = P_{OUT} \times \eta = \frac{144\ W}{0.80} = 180\ W$$

Calculate the input energy required for a full-wave bridge with the doubler switch open.

$$W_{IN} = \frac{P_{IN}}{f_{LINE}} = \frac{\left(\frac{P_{OUT}}{\eta}\right)}{f_{LINE}} = \frac{\left(\frac{144\ W_{OUT}}{0.80}\right)}{50\ Hz}$$
$$= 3.60\ Joules$$

$$C_{IN} = \frac{W_{IN}}{\left[(V_{PK})^2 - (V_{MIN})^2\right]}$$

where V_{PK} is the lowest peak voltage on two bulk capacitors in series in 220-V mode:

$$V_{PK(220V)} = V_{RMS(\min)} \times 1.414$$
$$= (220V - 10\%) \times 1.414$$
$$= 280V (use\ 275\ to\ be\ conservative)$$

$$V_{MIN(220V)} = V_{PK(220V)} - V_{RIPPLE} = (275V \times 0.75)$$
$$(use\ 25\%\ ripple\ to\ be\ conservative)$$
$$= 206V$$

Now, solve for capacitance:

$$C_{IN} = \frac{W_{IN}}{\left[(V_{PK})^2 - (V_{MIN})^2\right]} = \frac{3.60}{(275)^2 - (206)^2}$$
$$= 108\ \mu F$$

Since this design uses a doubler, two 220-µF capacitors would be used in series.

However, in the doubler mode, one capacitor is being charged while the other is discharged at 60 Hz. To determine the value of C1 and C2 needed in this case, use the following equations:

$$W_{IN} = \frac{P_{IN}}{f_{LINE}} = \frac{\left(\frac{144\ W}{0.80}\right)}{60Hz} = 3.00\ Joules$$

$$C1 = C2 = \left(\frac{W}{\left[(V_{CPK})^2 - (V_{C(\min)})^2\right]}\right)$$

where

- V_{CPK} is the lowest peak voltage on the individual bulk capacitors in 110-V mode
- $V_{C(min)}$ is approximated using the same $V_{(min)}$ as the non-doubler and a new V_{CPK}' calculated as

$$\begin{aligned} V'_{CPK(110V)} &= V_{RMS(\min)} \times 1.414 \\ &= (100V - 10\%) \times 1.414 \\ &= 127V\,(use\ 125\ to\ be\ conservative) \end{aligned}$$

$$V_{C(\min)} = \frac{(2V_{MIN} - V'_{CPK})}{3} = \frac{(2 \times 206 - 125)}{3} = 96V$$

$$\begin{aligned} C1 = C2 &= \left(\frac{W}{\left[(V'_{CPK})^2 - (V_{C(\min)})^2\right]}\right) \\ &= \left(\frac{3.00\ J}{\left[(125)^2 - (96)^2\right]}\right) = 470\,\mu F \end{aligned}$$

Therefore, the low-line, doubler-mode storage requirement defines the capacitor selection and, again being conservative, choose the next standard value of 560 µF. More capacitance can be used if missing cycle holdup is required.

Finally, since the capacitors are in series, balancing resistors are needed to keep the voltages divided between them. The balancing resistors override the potential internal capacitor leakage current as specified by the capacitor data sheets. This design uses a 44-kΩ, 1-W balancing resistor for the top capacitor and a 39-kΩ, 1-W balancing resistor in series with the PWM controller on the bottom, to provide a 2-mA balancing current. The 39-kΩ resistor also provides the PWM startup current, as demonstrated later in the paper. The lower resistor is smaller, because it is connected to a 12-V PWM V_{CC} zener clamp, so the voltage across it is less, but it still must sink the same amount of current as the top resistor.

D. Transformer Turns Ratio

Since the currents are highest in the secondary, the goal is to use minimal number of turns to keep resistive I^2R losses to a minimum. Once the minimum number of secondary turns are determined, then proceed to primary turns calculations.

Secondary Turns

Non-fractional turns ratios enable easy construction. Minimum turns on the high-current winding minimize winding resistive loss. Finding integer multiples involves comparing the ratios of the voltages with the number of turns that gets closest to those ratios. The following relation must be followed:

$$\frac{V1}{V2} = \frac{N1}{N2}$$

A common iteration process starts with one turn on the main output, and then (on the basis of volts per turn) calculates the number of turns required for the other outputs. The number of turns is incremented until integer multiples that satisfy the output regulation are found.

This design requires minimum turns on the high current 5-V winding, and good cross regulation to the 3.3-V winding, since these windings have the tightest tolerances. Assuming that 0.6-V V_F schottky rectifiers are used for both, a 5.6/3.9 or 1.46:1 ratio, or inversely a 1:0.70 turns ratio can be used. The following chart shows a winding evaluation:

TABLE 6. TRANSFORMER WINDINGS

5.6 V Turns	V/Turn	Turns To Yield 3.9 V	Effect
1	5.6	3.9/5.6=0.70	fractional
2	2.8	3.9/2.8=1.4	uneven
3	1.867	3.9/1.867=2.09	workable

The last option provides a good ratio, with 3 turns producing 5 V and 2 turns producing 3.3 V. This selection allows low turns on 5 V to get low winding losses, and good regulation for a 3.3 V output.

For a 12-V winding at 1.867 V/T, and using 0.9 V for the diode V_F, the ratio of 12.9/1.867 = 6.9 turns, is calculated, therefore use 7 turns.

Since 1.867 x 7 = 13.07 V, the resultant 12-V output is 13.07 - .9 = 12.17 V, or a +1.4% set point.

Primary Turns

Primary turns are determined by the input voltage range, duty cycle, and peak voltage allowed to the output rectifiers.

The maximum V/T of the secondary is derived from the maximum allowable voltage to the secondary rectifier divided by the number of secondary turns. Minimum V/T is derived from the maximum allowable duty cycle that can regulate the output voltage at the lowest input voltage. This calculation yields two limits where both requirements must be satisfied. Primary turns are then determined by the input voltage range and the peak voltage to be allowed on the output rectifiers.

Based on the earlier discussion of the diode voltage ratings, the maximum voltage on the 5-V diode is 19.8 V. A 40-V diode provides more headroom than necessary, and for purposes of these calculations was derated to 25 V for a 25 V/3 T = 8.3 V/T maximum.

The minimum number of primary turns ($N_{P(min)}$) is determined by dividing the high-line input voltage by the maximum number of volts per turn of the secondary winding.

$$N_{P(\min)} = \frac{V_{IN}}{[V/T]} = \frac{370}{8.3} = 44\,turns\,at\,high\,line$$

Fewer primary turns are not acceptable, because the 25-V limit established for the 5-V diode would be exceeded.

The low-line diode input must be 5.6 V/45% duty cycle = 12.4 V.

The maximum V/T is 12.4 V/3T = 4.13 V/T and the low line input is V_{MIN} = 216 V.

$$N_{P(\max)} = \frac{V_{IN}}{[V/T]} = \frac{216}{4.13} = 52\,turns\,at\,low\,line$$

More primary turns are NOT acceptable because the PWM maximum duty cycle limit could no longer regulate the output voltage.

Therefore, a 52-turn primary winding satisfies the low-line maximum duty cycle limit and remains within the voltage limits of the 5-V output diode. The secondary winding uses three turns for 5 V, 2 turns for 3.3 V, and seven turns for 12 V. However, in the actual transformer, the primary turns were reduced to 51 to fit in the core window area. Adding a 12-V PWM bias winding powers the selected PWM control circuitry with the same number of turns as the secondary 12-V output.

The transformer design should continue per guidelines set forth in the *Unitrode Magnetics Design Handbook*, (MAG100A)[1] and other application material, but that is beyond the scope of this paper. Cooper Coiltronics completed the transformer construction, with the turns ratios, output currents and operating frequency that were derived in the generation of this design.

The following are the final transformer parameters:

- Primary inductance = 2.3 mH
- Primary turns = 51, 2 windings paralleled with secondaries in between.
- 5 V = 3 T, 8.8 mΩ, copper strap
- 3.3 V = 2 T tapped off the 5-V winding, 2.2 mΩ
- 12 V = 2- 7 T windings in parallel. 22 mΩ, bifilar wound
- 12-V bias winding = 7 T
- ERL28 ferrite core
- Coiltronics # CTX16-16690

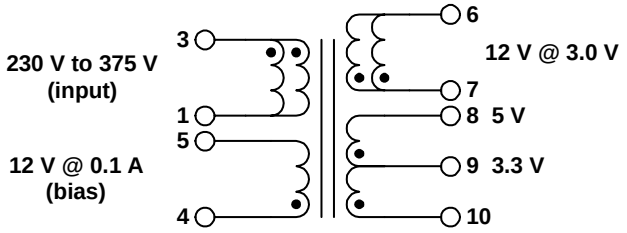

Fig. 4. Transformer schematic.

E. Output Inductor

Forward converters allow a useful technique for improved cross regulation, called the *coupled inductor,* in the output stage. Each output requires an inductor, and building on a common core greatly aids cross regulation and saves space. Regulation and ripple current can be *steered* or *adjusted* by the order of the windings on the core and by leakage inductance. The turns ratio of the coupled inductor must be the same as the transformer turns ratio, or the secondary winding has a shorted turn. Output inductor design methods in (MAG100A), Topic R5[1], base the minimum output inductor value on the minimum load specification of the output toward which the ripple current is steered, in order to maintain continuous current in the inductor. This approach is helpful in maintaining a closed-voltage loop gain for good transient response.

TABLE 7. CURRENT MINIMUM

Output Option	I_{MIN} (A)
3.3 V	1.0
5 V	2.0
12 V	1.0

It is desirable to keep the inductor current continuous for loop response concerns. The inductor operates in discontinuous mode if the minimum average current is less than half the peak-to-peak ripple current. Therefore, the peak-to-peak ripple current must be twice the minimum average current. For this example, the ripple current will be steered to the 12-V output. Here, I_{MIN} is 2 A and the ripple current can be:

$$I_{P-P} = 2 \times I_{MIN} = 2.0\,A$$

The current required during the maximum PWM OFF time determines the inductance value:

$$L = V \times \frac{dt}{di}$$

where

- di is the peak to peak ripple current (2 A)
- V is the applied voltage on the inductor during the OFF time (V_{OUT} of 2 V plus the rectifier drop of 13.07 V as determined earlier
- dt is determined from the worse case minimum duty cycle (maximum OFF time) on the output where the loop closed, in this case, the 5-V output

$$Duty\ Cycle(\min) = \frac{V_{OUT}}{V_{IN(\max)}} \times \frac{N_P}{N_S}$$

$$t_{OFF} = (1 - D_{MIN}) \times \left(\frac{1}{f_{SW}} \right)$$

To calculate the duty cycle at 100 kHz,

$$Duty\ Cycle(\min) = \left(\frac{5.6}{370} \right) \times \left(\frac{51}{3} \right) = 27\%$$

- t = 2.7 µs
- t_{OFF} = 7.3 µs

As seen on the 5-V winding,

$$L = V \times \frac{dt}{di} = \frac{13.07 \times 7.3\,\mu s}{2.0\,A} = 47.7\,\mu H\ \ (use\ 50\,\mu H)$$

Although the minimum inductor value is 50 µH, a larger one can be used to lower the peak-to-peak ripple current and also allow a lower minimum load. Lowering the ripple current benefits the output voltage ripple, since the inductor ripple current times the ESR of the output capacitors largely determines the output ripple voltage. It should be noted that a higher inductor value, while potentially reducing the cost of the output capacitors, comes with the penalty of slower response to sudden load changes.

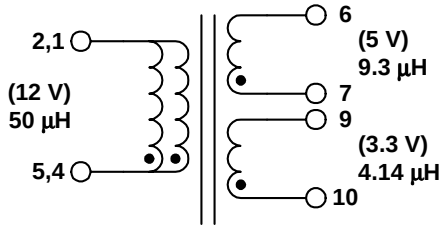

Fig. 5. Inductor schematic.

The order of the windings is determined in order to steer the ripple current to 12 V and to keep the leakage inductance between the 3.3-V and 5-V windings low, ensuring good cross regulation. The inductance for both the 5-V and 3.3-V outputs result from the relationship of the turns ratio squared. The 12-V winding was wound first, a 5-V copper strap was second, and 3.3 V was wound on the outside. The designer can experiment with different winding arrangements to affect ripple current steering and cross regulation.

The final inductor values and winding order are shown in Table VIII. This inductor was made for us by Coiltronics as CTX16-16691.

F. Output Capacitors

Output capacitors are selected on the basis of ESR, required value, physical volume, and the RMS ripple current each can accommodate.

Capacitor Equivalent Series Resistance (ESR)

The major component of the output ripple is the inductor ripple current impressed upon the ESR of the capacitor as:

$$\%V_{RIPPLE} = \frac{I_{RIPPLE} \times R_{ESR}}{V_{OUT}}$$

Since the choice was made to steer the ripple current to the 12-V output, its ripple current will be higher, while that on the other two outputs will be lower than predicted. However, since quantifying this steering function is difficult, the maximum ESR values will be calculated for each output independently as follows. For the 12-V winding, with a minimum load of 1-A_{DC}, (p/p) and a 2% ripple specification:

$$R_{ESR(\max)} = \frac{2\%\ V_{OUT}}{I_{MIN(p-p)}} = \frac{240\ mV}{2\ A}$$
$$= 120\ m\Omega\ \ (12V\ output)$$

$$R_{ESR} = \frac{50\,mV}{4\,A} = 12.5\ m\Omega\ (5V\ output)$$

$$R_{ESR} = \frac{33\ mV}{2\,A} = 16.5\ m\Omega\ (3.3\ V\ output)$$

These are the maximum ESR values that each output capacitance is allowed. ESRs of capacitors in parallel add ESR in parallel, such that a lower ESR value is achieved by placing multiple capacitors in parallel, which may also lower the cost.

TABLE 8. COUPLED INDUCTOR WINDINGS
ER28L FERRITE CORE, 1.45 MM GAP

Winding Order	V_{OUT}	Turns	L Value (µH)	Reistance (mΩ)	Material
1	12 V	21	50	53	4 strands bifilar
2	5 V	9	9.3	6	Copper strap
3	3.3 V	6	4.14	2.5	Copper strap

Capacitor Value

This is a large-signal hold-up time requirement for step-load response.

The 5-V capacitor is determined first because the loop is closed on 5-V winding.

A load variation (ΔI) on an output causes a voltage variance (dV) on the basis of the time it takes the loop to respond (dt) and the output capacitance (C). For simplicity, disregard the ESR and ESL effects.

$$dV = \frac{\Delta I}{C} \times dt$$

The minimum allowable capacitance is determined by the loop response time and allowable output voltage variation as shown below:

$$C = \Delta I \times \frac{dt}{dV}$$

The allowable voltage variation is the total output tolerance minus the error amplifier set-point tolerance. A 1% reference and 1% resistors in the divider, provide a 2% $V_{SETPOINT}$.

The allowable variation ($\%V_{OUT}$) of the 5-V output is 5%.

$$dV = V_{OUT}\left(\%V_{OUT} - \%V_{SETPOINT}\right)$$
$$= 5V\left(0.05 - 0.02\right) = 5V(0.3) = 150\,mV$$

The value dt is the loop response time, during which the capacitor holds up the output voltage until the loop can respond. The reasonable practical maximum that the loop can be crossed over is $f_{SW}/10$. At 100 kHz this is 10 kHz or 100 µs response time. 5 kHz or 200 µs is used for margin.

The load step ΔI is defined in the specification as 3 A.

$$C = \Delta I \times \frac{dt}{dV} = 3\,A \times \frac{200\,\mu s}{150} = 4000\ \mu F$$

This same parameter is harder to calculate on the 3.3-V and 12-V windings, since their regulation is aided by the coupled inductor. The same response time is assumed for initial calculations with a conservative margin.

To calculate the dV for the 3.3-V winding,

$$dV = V_{OUT}\left(\%V_{OUT} - \%V_{SETPOINT}\right)$$
$$= 3.3\,V\left(0.05 - 0.02\right) = 3.3V(0.3) = 100\,mV$$

To calculate the capacitor value for the 3.3-V winding,

$$C = \frac{1A \times 200\mu s}{0.1V} = 2000\,\mu F$$

To calculate the dV for the 12-V winding,

$$dV = V_{OUT}\left(\%V_{OUT} - \%V_{SETPOINT}\right)$$
$$= 12\,V\left(0.10 - 0.02\right) = 12V(0.8) = 960\,mV$$

To calculate the capacitor value for the 12-V winding,

$$C = \frac{2A \times 200\mu s}{0.96V} = 416\,\mu F$$

The correct choice is the closest standard value capacitor, which is 560 µF.

RMS Ripple Current

The root-mean-squared (RMS) current in each output (I_{RMS}) is approximated as a purely triangular waveform:

$$I_{RMS} = \frac{I_{PEAK}}{\sqrt{3}}$$

The derived I_{PEAK} value of 2 A is used to calculate the I_{RMS} for the 5-V winding, use:

$$I_{RMS} = \frac{2A}{1.73} = 1.156\,A$$

The calculation of the I_{RMS} for the 3.3-V winding, uses the derived I_{PEAK} value of 1 A:

$$I_{RMS} = \frac{1A}{1.73} = 0.58\,A$$

The calculation of the I_{RMS} for the 12-V winding uses the derived I_{PEAK} value of 1.0 A:

$$I_{RMS} = \frac{1.0\,A}{1.73} = 578\ mA$$

Final Selection

For the 5-V requirement, finding a 4000-µF, 12.5-mΩ, 1.156 A_{RMS} capacitor was difficult and proved too expensive.

The EEU-FC0J392, 3900 µF, 6.3 V, .030 Ω, 1.95 A_{RMS}, is available for $0.41 (for quantities of 1,000 or more) from Digikey.

The EEU-FC0J222, 2200 µF, 6.3 V, .045 Ω, 1.44 A_{RMS}, is available for $0.28 (for quantities of 1,000 or more) from Digikey

The compromise uses two 2200-µF capacitors in parallel. The choice was determined primarily by the ESR value limitations, and even though the combined maximum ESR is 22.5 Ω, the actual ESR is considerably less.

Table IX gives calculated values and recommended components for the three windings.

Customarily, a ceramic capacitor with a value between 0.1 µF and 1 µF is placed in parallel with the bulk capacitors to reduce high-frequency noise.

G. Output Rectifier Snubbers

Because of the inherent parasitic inductance of the board layout, and the reverse recovery time of the output rectifiers, ringing exists at the input to the inductor on each output. To compensate for this, calculate the parasitic elements and then use the formula for a critically damped L-R-C waveform to control the ringing.[4]

First measure the frequency of the ring at the inductor input. Then place a capacitor across the free wheeling diode such that the frequency of the ring is reduced by a factor of approximately two. Since it is now known that the added capacitor is equal to the parasitic capacitance, calculate the parasitic inductance by using the following equation to solve for L.

$$f = \frac{1}{2\pi\sqrt{LC}}, \text{ where f = ring frequency}$$

Now that L and C are known, calculate the R to use in series with the C to dampen the ring.

$$Q = \frac{1}{R\sqrt{\frac{L}{C}}}$$

For a critically damped circuit set Q equal to 1 so that:

$$R = \frac{1}{Q\sqrt{\frac{L}{C}}} = \frac{1}{\sqrt{\frac{L}{C}}}$$

Losses in the snubber can be minimized by reducing the capacitance needed to dampen the ringing by experimentation. The following equation calculates the snubber resistor losses:

$$P = CV^2 f_{SW}$$

where V is the peak-to-peak (p-p) voltage across the diode

This design requires snubbing the highest power 5-V output. A 33-MHz ring occured at the inductor input. Adding a 2200-pF capacitor in parallel with the free-wheeling diode reduced that to 15 MHz. The inductance of the resonant tank was calculated to be 51 nH, and a 5-Ω, 1-W resistor was used for critical dampening. This configuration provided excellent snubbing of the 5-V winding. It is also was enough to control the ringing on the other two windings due to the interaction of the coupled inductor.

H. Output Rectifiers

The reverse voltage rating for the 3.3-V and 12-V rectifiers is determined using the maximum peak input voltage and transformer turns ratio. The 5-V diode was selected to be a 35-V rated component.

TABLE 9. OUTPUT CAPACITORS: CALCULATED VALUE AND COMPONENTS

Winding Voltage (V)	Calculated Values				Component				
	Capacitance (µF)	Voltage (V)	Resistance (mΩ)	Current (A_{RMS})	Part Quantity and Name	Capacitance (µF)	Voltage (V)	Current (A_{RMS})	Resistance (mΩ)
5	4000	6.3	12.5	1.156	2 Panasonic EEU-FC0J222	(2) 2200	6.3	1.44	45
3.3	2000	6.3	16.5	0.58	2 Panasonic EEU-FC0J102	(2) 1000	6.3	0.755	90
12	560	25	120	0.578	EEU-FC1E561	(1) 560	25	1.2	65

To calculate the reverse voltage for the 12-V rectifier,

$$V_R = \frac{V_{PK(\max)} N_S}{N_P} = \frac{370 \times 7}{51} \cong 51$$

To calculate the reverse voltage for the 3.3-V rectifier,

$$V_R = \frac{V_{PK(\max)} N_S}{N_P} = \frac{370 \times 2}{51} \cong 14.5$$

Rectifier current is the peak inductor ripple current (minimum load current) added to the maximum output current.

To calculate the rectifier current for the 3.3-V rectifier,

$$I_{DIODE} = I_{OUT(\max)} + I_{RIPPLE(peak)} = 5\,A + 1A = 6\,A$$

To calculate the rectifier current for the 5-V rectifier,

$$I_{DIODE} = I_{OUT(\max)} + I_{RIPPLE(peak)} = 18\,A + 2\,A = 20\,A$$

To calculate the rectifier current for the 12-V rectifier,

$$I_{DIODE} = I_{OUT(\max)} + I_{RIPPLE(peak)} = 3\,A + 1\,A = 4\,A$$

This design requires a diode that has a low forward voltage. Diode losses are largely determined by the forward voltage and current.

$$P_{AVG} = I_{PEAK} + V_F \times Duty\,Cycle$$

However, rectifiers are sold in packages of two with a common anode, so eliminating the duty-cycle term allows calculation of the dual diode package loss. The general formula for calculating diode losses is

$$P_{DIODE} = V_F \times I_{PEAK}$$

Using the previously calculated criteria, the following output diodes are chosen.

TABLE 10. DIODE RECOMMENDATIONS

	Output (V)		
	3.3	**5**	**12**
Voltage Rating (V)	30	35	200
Current Rating (A)	30	30	6
Package	TO-220	TO-247	TO-263
Manufacturer	IR	IR	On-Semi
Part Number	32CTQ030	30CPQ035	MURD620

I. Power Switching FETs

The primary-side switching FETs are chosen as IRF840 devices. While there are many device types that can satisfy the requirements for this design, the IRF840, featuring specifications of 500-V, 8-A capability and an $R_{DS(on)}$ of 0.85 Ω, offers good performance at a low cost.

With many IC controllers having an output drive current capability of ±1A, interfacing the low-side FET is very straight-forward. Driving the high-side switch in parallel, however, requires a level-shifting circuit which can be implemented in several ways, but the technique selected for this design is to use an off-the-shelf isolated gate drive transformer as shown in Fig. 6. The circuit is described in considerable detail in SEM-1400, Topic 2, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits* [7], and was chosen for this application because it restores the DC levels of the PWM drive to the isolated FET gate while providing a constant drive voltage independent of duty cycle.

The Coiltronix CTX08-14225 transformer, together with a 0.1-µF coupling capacitor on each winding of the gate drive transformer satisfied the minimum requirements set forth the by the governing equations in [7].

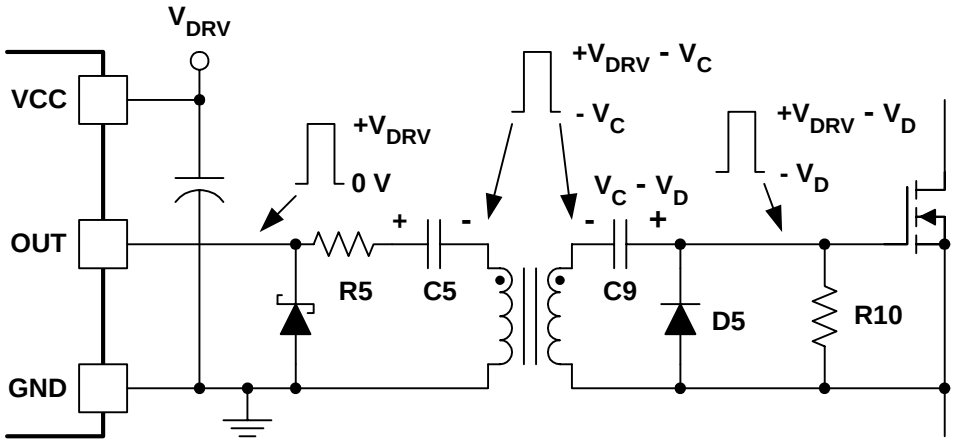

Fig. 6. Isolated gate drive transformer.

J. IC PWM Controller

The UCC3813-1 is chosen for its ease of use, current-mode control capability, and low cost. The UCC3813 is a lower cost version of the UCC3800, with some parameter tolerances widened for better yield in manufacturing. The UCC3813 family is an enhancement of the original Unitrode design, UC3842.

The application note SLUA084 [5], further details the UCC3800/UCC3813 advantages which include

- a wider range of UVLO for the UCC3813 (from 4 V to 12 V)
- internal soft start for controlled turn-on
- leading-edge blanking
- better accuracy for both V_{REF} and frequency
- faster current limit
- lower operating current
- maximum duty-cycle of 50%

PWM Bias Supply and V_{CC} Capacitance

There are two areas of concern when powering the UCC3813-1 PWM. The first is at start-up, when the PWM is attempting to bring all the outputs up to regulation. The second is under steady-state operation. During these periods, the V_{CC} must stay above the UVLO undervoltage lockout turnoff point.

- UVLO start threshold is 8.6 V to 10.2 V, V_{CC} > UVLO, and start PWM current is 1.2-mA maximum.
- UVLO stop threshold is 6.8 V to 8.4 V, V_{CC} < UVLO, and stop PWM current is 230-µA maximum
- Start-to-stop hysteresis is 1.6 V to 2.4 V.

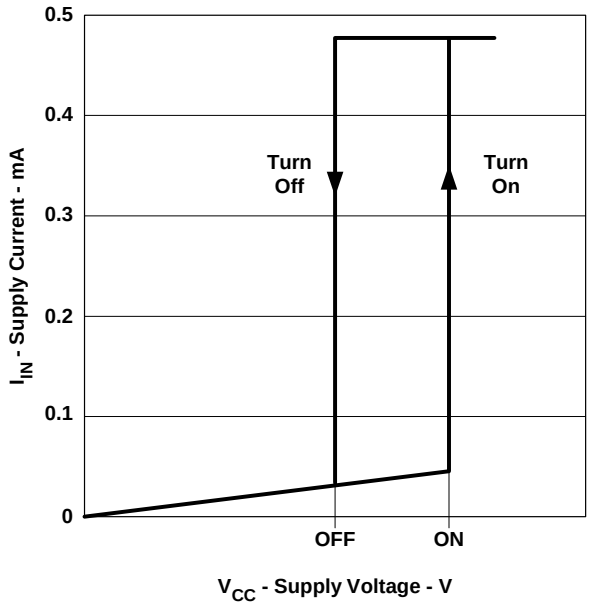

Fig. 7. Input voltage (V_{CC}) hysteresis window

Start-up is a function of the storage capacitance on V_{CC}. Value selection is by the following process:

- Determination of the lowest input voltage at which the supply is expected to turn on. (232 V_{DC})
- Use of the maximum of 230-µA startup current to determine the maximum value of R. (the bleeder resistor across the lower bulk capacitor supplies the *start-up current* listed in the data sheet) This resistor current charges the V_{CC} storage capacitor until the UVLO start threshold is reached.

$$I = \frac{\left[\left(\frac{V_{DC}}{2}\right) - V_{CLAMP}\right]}{39\,k\Omega} = 2.6\,mA$$

  which is more than enough needed for startup.
- The capacitor must power the UCC3813 between the UVLO start and UVLO stop window, or until the bias winding takes over. The assumption is that this time is 10-ms (more than the 4-ms soft-start period of the device).
- Once the device reaches the UVLO start, current in the controller increases to *operating supply current* of 1.2-mA maximum. However, this is only the device current and does not include the current required to drive the power switching FETs which must also come from V_{CC}. Since the gate current is I = Qgf/2 and there are two FETs, then I = Qgf. The IRF840 FETs are characterized by the published data of 63-nC gate charge.

$$I = QgF = 63\,nC \times 100\,kHz = 6.3\,mA$$

$$I_{TOTAL} = I_{MAX} + I_{FETdrive} = 1.2\,mA + 6.3\,mA = 7.5\,mA$$

- For I = 7.5 mA, dt = 10 ms, dV as the minimum UVLO turn-on, and UVLO turn-off hysteresis = 1.6 V, the following equation solves for the capacitor value.

$$C = \Delta I \times \frac{dt}{dV} = 0.075 \times \frac{0.01}{1.6} = 46.8\,\mu F \cong 47\,\mu F$$

Adding a ceramic capacitor with a value between 0.1 µF to 1 µF, in parallel is standard practice to provide high frequency decoupling for the V_{CC} and to provide a reservoir for the peak currents required to turn on the power FETs.

During the second time period the bias winding must provide the PWM power. The bias winding is selected to provide a voltage that stays above the UVLO stop threshold. A 12-V bias winding voltage stays above the UVLO stop threshold and uses the same turns ratio as the 12-V main output. A lower voltage could have been used.

The bias winding is forward derived, like the isolated outputs, so an inductor, two diodes and capacitor are required. The inductor chosen is a low-cost averaging element. The calculated inductance would be very large if continuous conduction was required, approximately 18 mH, however, a smaller 100-µH inductor can be used to average the applied winding pulse and accept some loss in regulation. The 47-µF V_{CC} capacitor provides the holdup during the time the inductor is discontinuous.

Finally, a 12-V zener clamp at the V_{CC} of the PWM prevents the UCC3813 internal 13-V V_{CC} zener clamp from failing because of overcurrent conditions caused by output overloads and short circuits. A 200-Ω resistor limits the current into the 12-V clamping zener. Fig. 8 shows the resultant circuit.

Primary Current Sense Resistor

The primary current is the sum the of 1) the output current with the peak inductor ripple added in normalized to the 5-V winding and reflected to the primary by the turns ratio N_S/N_P and 2) the transformer magnetizing current $I_{MAG,}$ which is derived from the primary magnetizing inductance. Magnetizing inductance is established by placing a small gap in the core so that this value is fixed rather than variable over volume production. A notable consequence of the 2-mH magnetizing inductance is that it adds a slope to the PWM current-sense ramp similar to slope compensation. This slope is beneficial to loop stability, even with duty cycles less than 50%.

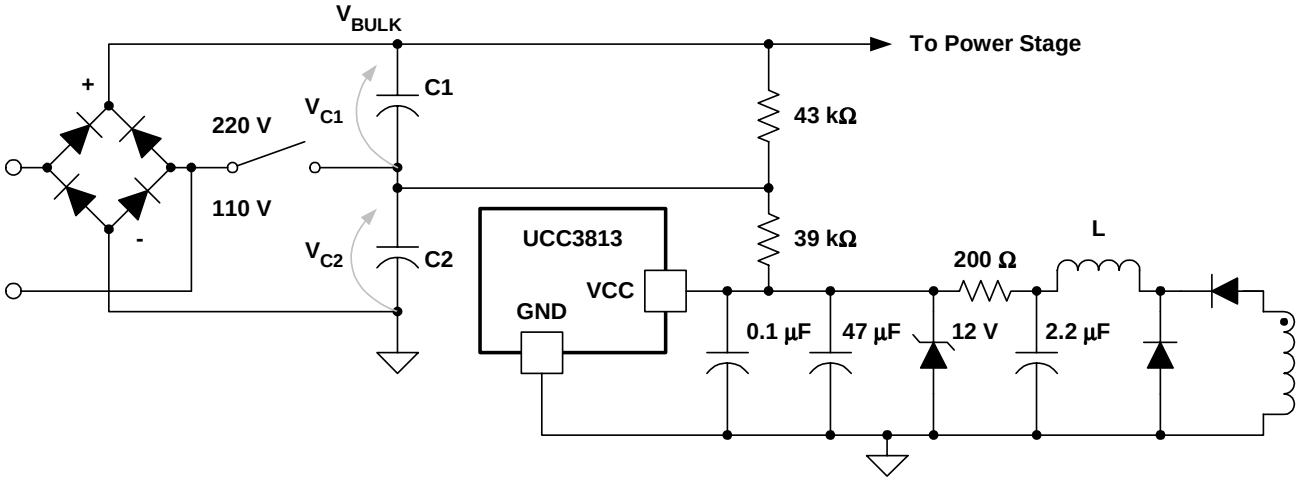

Fig. 8. PWM start-up and bias current.

$$I_P = I_{MAG} + I_S{}' \left(\frac{N_S}{N_P}\right) \text{ where,}$$

$$I_S{}' = I_{PEAK}\left(\frac{N_S}{N_P}\right) \text{ for each output}$$

$$= 20\left(\frac{3}{51}\right) + 6\left(\frac{2}{51}\right) + 4\left(\frac{7}{51}\right) = 1.96\,A$$

$$I_{MAG} = \left(\frac{V_{IN(\max)}}{L}\right)\left(t_{ON(\min)}\right) = \left(\frac{370}{2.3\,mH}\right)(2.5\,\mu s)$$

$$= 0.40\,A$$

$$I_P = I_{MAG} + I_S{}' = 1.96\,A + 0.40\,A = 2.36\,A$$

The UCC3813 has a 0.9-V pulse-by-pulse current limit minimum, and the following equation solves for the primary current sense resistor:

$$R_S = \frac{V_S}{I_S} = \frac{0.9V}{2.36\,A} = 0.381\,\Omega$$

therefore, the appropriate resistor is the one with the closest available standard resistor value, 0.4 Ω.

Note that the current sense resistor also sees the FET gate current and the output rectifier recovery current at the beginning of each power pulse. This leading-edge current spike is blanked within the UCC3813.

K. Setting Up the Loop

Fig. 9 shows an isolated power supply loop being closed in the secondary with the TL431A. As the error signal is generated by the TL431A, there is no need to use the PWM error amplifier. A common practice is to make the PWM error amplifier *current source only*, commanding maximum pulse widths, and use the optocoupler circuit to reduce the duty-cycle by pulling down on the error amplifier output COMP pin. This configuration is accomplished by connecting the PWM feedback input to ground. This connection forces the output of the error amplifier COMP to be high, commanding full duty-cycle.

The COMP source current of the PWM error amplifier is specified in the data sheet as 800 µA maximum. Therefore, the optocoupler circuit must be able to sink that much current and also place COMP to a low-enough voltage to ensure zero duty-cycle. This COMP low voltage is determined by the COMP to CS offset of 0.45 V minimum listed in the UCC3813 data sheet. In other words, when COMP is at 0.45 V, then the duty cycle is zero.

The optocoupler must sink the COMP source current of 800 μA and pull COMP down to .45 V to achieve zero duty-cycle. The optocoupler has a $V_{CE(sat)}$ of 0.3 V, so it could be directly connected to the COMP pin; however, a small resistor is added in series to lessen noise effects. The resistance needed is calculated as R=V/I=0.15 V/800 μA=187 Ω maximum, so the choice is to use 150 Ω.

Another way to help reduce noise is to increase the optocoupler output current by adding a pull-up resistor between VREF and the optocoupler collector (R6 in Fig 8). However, this technique causes $V_{CE(sat)}$ of the optocoupler to increase and is not needed in this design.

It is necessary to sink 800 μA in the optocoupler, and this sink current is determined by the optocoupler diode drive and the current transfer ratio (CTR). This device has a typical 100% CTR, but reduces to 40% at the temperature extremes. Using the 40% value, at least 800 μA/0.4=2 mA is needed to sink through the optocoupler diode. The TL431A can sink a maximum current of 30 mA, so there is enough current to drive the optocoupler and force the PWM to zero duty cycle.

Component D12 in Figure 9 is a 10-V zener diode, the voltage source for the optocoupler drive circuit. Its current is provided from the 12-V output through a current-limiting resistor R18. R16 is calculated by subtracting the V_F=1.5 V of the optocoupler diode, and the TL431A anode voltage of 2.5 V, from the 10-V source. Using a 30-mA maximum and solving for R16,

$$R16 = \frac{(10V - 1.5V - 2.5V)}{0.03A} = 200\,\Omega$$

The TL431A has a specification for minimum cathode current for regulation of 1 mA. This is used to determine R17 in parallel with the optocoupler diode. To maintain some margin, a 2-mA value is used.

$$R17 = \frac{1.5V}{2\,mA} = 750\ \Omega$$

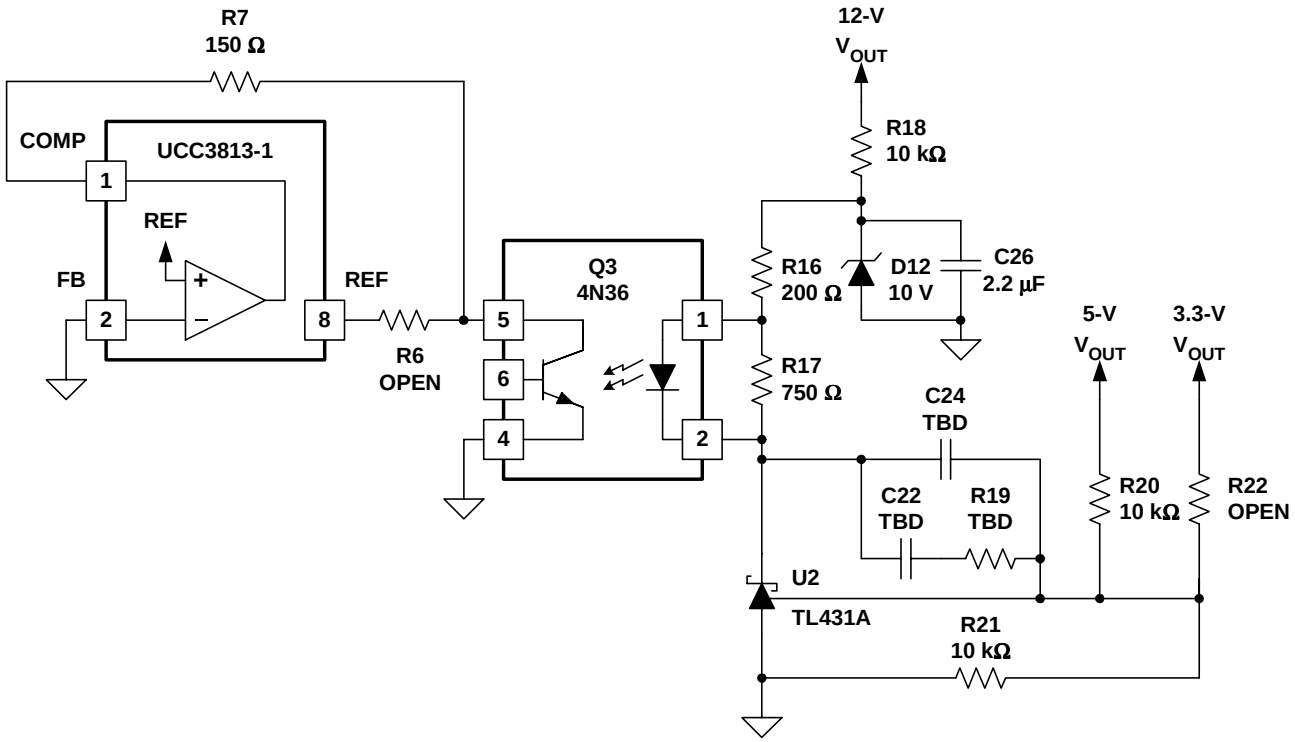

Fig. 9. Isolated power supply loop closed.

Closing the Loop

There are many interactions that a coupled inductor can add when closing the feedback loop which are beyond the scope of this paper. For testing purposes the loop is closed with a low bandwidth by using a 1 µF capacitor for C24. Further optimization is required to determine the values needed for the 5-kHz bandwidth required. For a thorough description of closing an isolated feedback loop using the TL431, see SEM-1500, Topic 3.[6]

L. A Few Optional Ideas

There are some additional ideas that are worth mentioning:

- With the 110 V/220 V selector switch, it is possible to place the switch in the doubler mode and connect to 220 V. This setup would overvoltage the bulk capacitors, probably causing venting and a safety hazard. A common practice is to place metal oxide varistors (MOVs) (or high power zeners), in parallel with each input capacitor, so that in the event of overvoltage, the MOV impedance collapses, causing high-input currents and blowing the input fuse.
- The addition of a schottky diode from the PWM output to V_{CC} clamps the output to V_{CC} and the external zener clamp. In the event of a MOSFET gate to drain short, the gate is pulled high and clamped to the 1-W V_{CC} zener. If a fuseable gate drive resistor is used, it then opens up during this event and prevent the PWM from venting smoke and making loud noises.
- The loop in this design is closed on the 5-V output with a 2.0% tolerance (1% TL431A and 1% resistors). To tighten the 3.3-V regulation, with some accuracy loss to the 5 V it is possible to sum both the 3.3 V and 5 V into the TL431A feedback using R22.
- If this power supply requires powergood or reset signal, there are several methods for meeting this requirement:
  - UC3904, AC line input fail, monitors positive and negative voltages, over and undervoltage, over current functions, power good delay.
  - TPS3514, senses three positive voltages, OV, UV, remote turn-on and turn-off control, and overcurrent.
  - Several methods are in the *supervisory circuits* home page on the TI website.
- Primary R-C snubber components are included in this design. Experience shows that the high dV/dt of the high-voltage primary waveform can be a key source of broadband emissions in the 10 MHz to 100 MHz range. In this design, the dV/dt at high line maximum load is 6.6 V/ns. An R-C filter using a 100-pF capacitor and a 1-kΩ resistor reduced that to 5 V/ns. Even slight reductions such as this can have dramatic improvements on EMI. Placeholders for snubbers and slew rate control should be included on the chance they may be needed.

IV. TEST RESULTS

Fig. 10 represents the final schematic of this forward converter design example.

A. Efficiency

A target efficiency of 80% is obtained when measured with a precision input harmonic/power analyzer that measures true input power. The data coincide very well with expected results. (As a caution, it should be noted that initial measurements, made using a DVM digital voltage meter for input current and voltage, yielded only 60% and very high RMS input currents, caused by the DVM's inability to accurately measure true RMS input current because of the high harmonic content associated with a peak detecting bridge rectifier.)

Fig. 10 shows that at full load, the efficiency was poorest at low input and increased at higher input voltages. This pattern indicates resistive losses in the design, since as the input voltage increases, the power train currents decrease. At full load output (144 W), the efficiency ranged from 79% at 90 VAC input to 81% at 264 V_{AC} input.

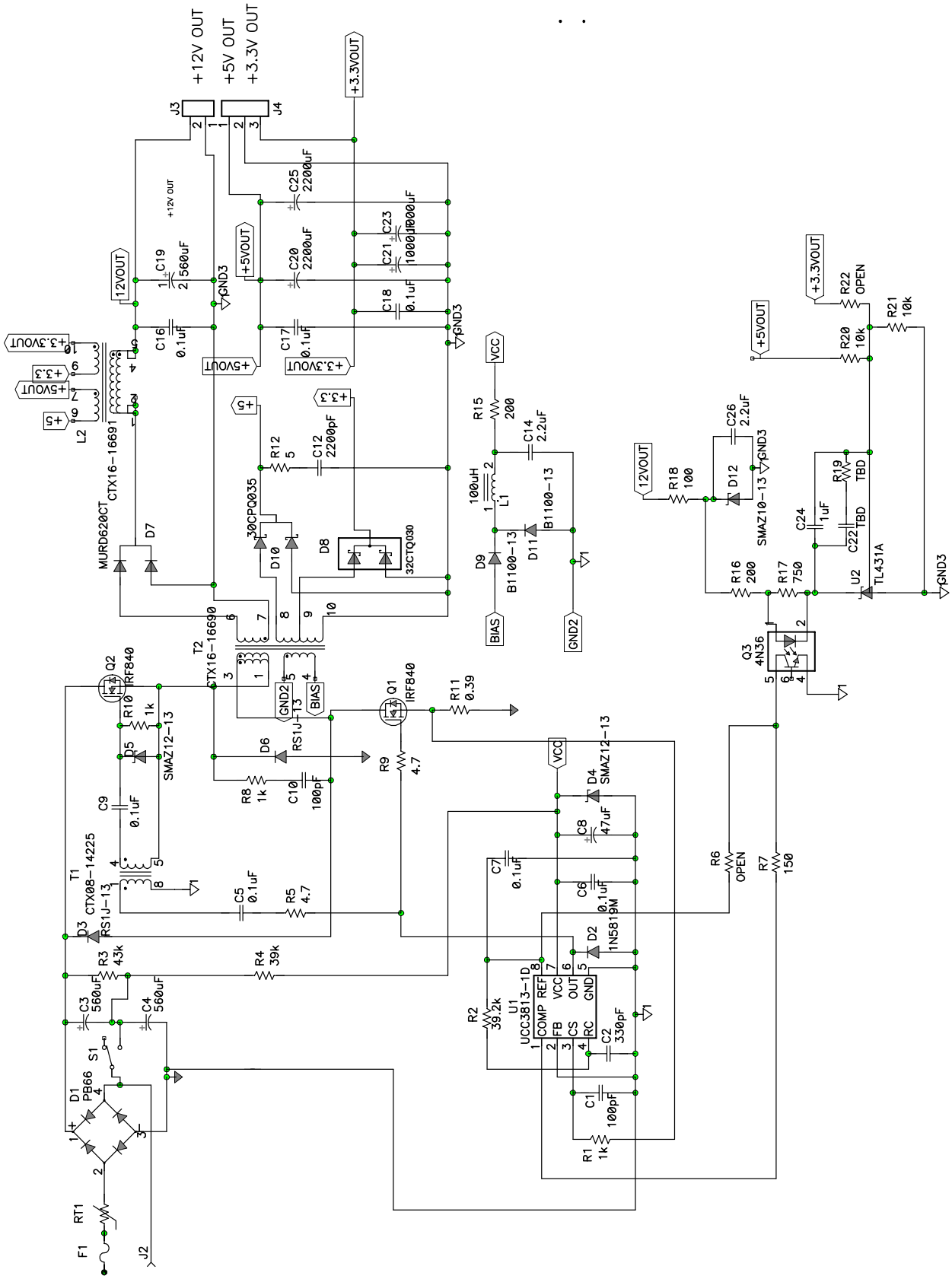

Fig 10. Forward converter schematic.

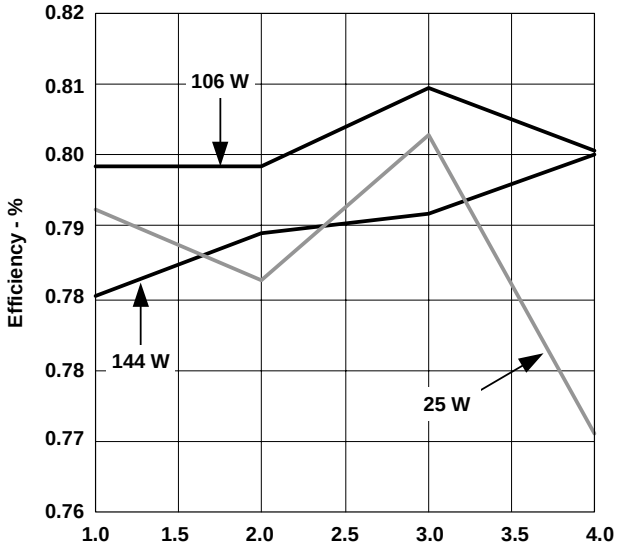

Fig. 11. Efficiency.

Note that at the light load of 25 W, efficiency drops off at the high-input voltage. This dropoff demonstrates capacitive switching losses in the circuit based on $P=CV^2f$.

B. Cross Regulation

The outputs were evaluated for cross regulation by means of the following tests:

- putting the full load on the 5-V output with minimum loads on the other two
- putting minimum load on 5-V output and full load on the others. Since the voltage loop is closed on 5-V output, it remained solid as expected. Fig. 12 shows the results. The following variations occurred:
- 12 V varied by +8% and -5%.
- 3.3 V varied by ± 6%.
- 5V was within 1%.

Both unregulated outputs, at maximum load, were low when the 5-V output was lightly loaded. This result is expected because of resistive losses in the 12-V output and 3.3-V output paths that were not compensated for directly by the voltage loop. Both unregulated outputs were high when they were lightly loaded and 5-V output was at its maximum. Again, the resistive losses in the 5-V output were compensated for by the loop, forcing the other two outputs higher. This is, however, much better regulation than would have been typically obtained using separate inductors.

The 3.3-V output was beyond the ±5% specification, so summing both 3.3-V and 5-V outputs to close the loop brings the 3.3-V within the requirements while allowing the 5-V to have an increased tolerance. This summing can be an iterative exercise since the inductor coupling of the outputs and the resistive losses all contribute to the voltage variance. Treating the TL431A 2.5-V reference as a summing junction allows the adjustment of the contribution that each output has to the 2.5-V set-point and can modify each outputs regulation for a good compromise.

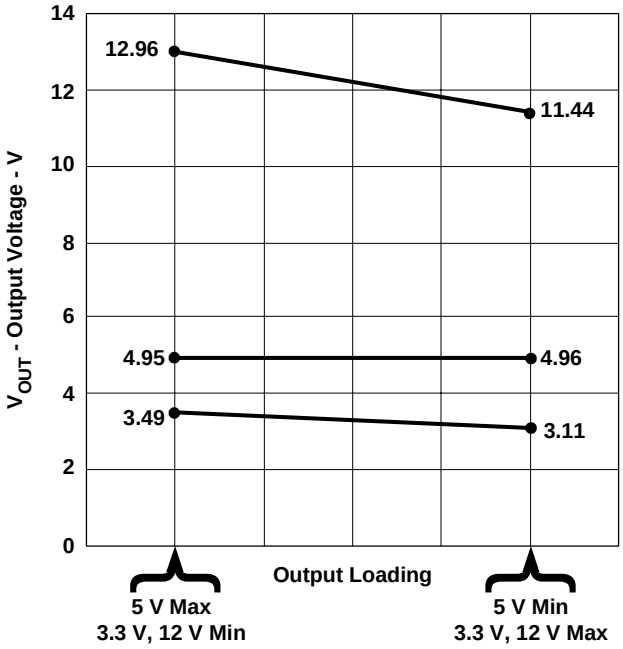

Fig. 12. Cross regulation extremes.

C. Input Capacitor Ripple

Fig. 13 shows the input capacitor ripple at maximum load and low line 90-V_{AC} input.

Two 560-µF capacitors are used for the closest available standard to the 474-µF calculated values.

The peak voltage on the capacitors is 231 V, with 14.2 V of ripple, resulting in a $V_{IN(min)}$ of 216.8 V, higher than the 206-V calculated but explained by the fact that the input capacitors were oversized for the low input range.

The calculations indicated that the peak voltage would be 254 V, but the measured value is less by about 20 V. Understanding the difference between calculated and measured

peak voltage is important because it affects the ability to regulate the output at maximum duty and minimum input voltage. The difference can be attributed to resistive losses in the input, the inrush thermistor, and the bridge rectifier. The peak currents are normally high when using a rectifier/capacitor input from an AC line.

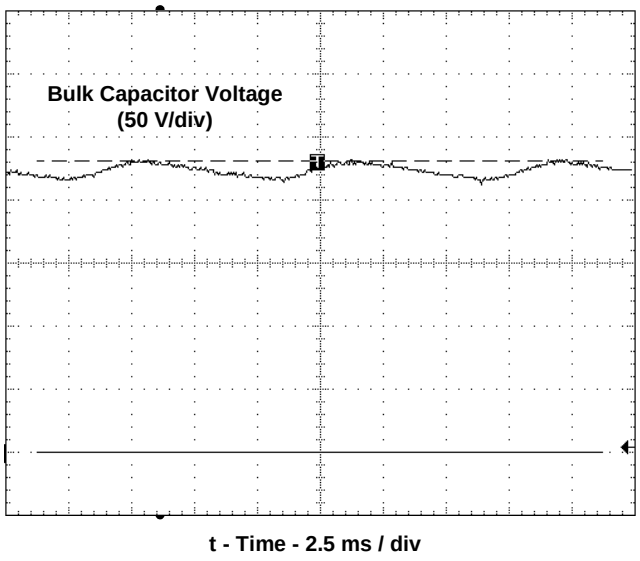

Fig. 13. Bulk capacitor input ripple at 90-V_{AC}, maximum load.

Overall, the input ripple met expectations and allowed duty cycle control over all input voltages.

D. Primary Waveforms

Fig. 14 shows the primary Q1 drain-to-source voltage at maximum load and 90 V_{AC} input, and associated drain current. The current is 2 A per division and reaches approximately 1.9 A. This value agrees with the prediction of 2.36 A primary current.

The switching frequency is 9 µs or 111 kHz. The UCC3813 data sheet graphs were used to determine the R-C values for 100 kHz and were slightly rounded up.

The duty cycle is 4-µs ON and 5-µs OFF for a 44% value. The maximum duty-cycle is required at the lowest input voltage; and with a measured value of 44% it shows some margin available.

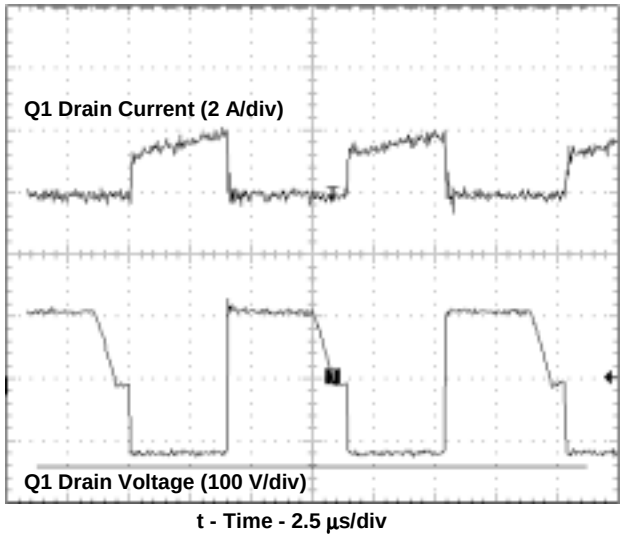

Fig. 14. Q1 drain-to-source voltage and drain current at maximum load and 90-V_{AC} input.

Fig. 15. shows the same waveforms with a 264-V_{AC} input maximum.

The duty-cycle time is 2.5-µs ON and 6.5-µs OFF for a 27% value, exactly agreeing with the calculated number. The maximum FET voltage, 350 V measured, indicates some margin on the 500-V FET rating.

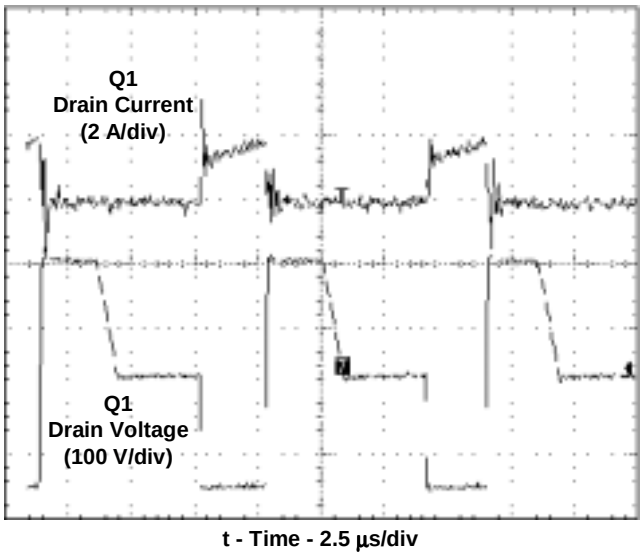

Fig. 15. Q1 drain-to-souce voltage at maximum load and 264 V_{AC} input.

E. Output Ripple Voltage

The figures below show the ripple voltage in the outputs. From this information, and a knowledge of the capacitors' ESR values, you can extrapolate the inductor ripple current. The specifications for ripple voltage were 1% on the 5-V and 3.3-V outputs, and 2% for the 12-V output. The ripple and noise voltages measured on the three outputs of this power supply are given in Table X, and the waveforms are shown in Figures 16, 17, and 18.

TABLE 11. OUTPUT RIPPLE VOLTAGE

Winding (V)	Specified $V_{RPL(p-p)}$ (mV)	Measured $V_{RPL(p-p)}$ (mV)	Peak Noise Spikes (mV)
12	240	130	172
5	50	15	58
3.3	33	100	181

As shown in Table X, better filtering is needed on the 3.3-V output, The major cause of this is the coupled inductor steering mechanism which is affected by the small mismatch in the voltage drops of the 5-V and 3.3-V rectifiers whose effect is difficult to quantify. This is shown in the shape of the waveforms where the triangle wave on the 12-V output demonstrates the success in steering most of the ripple current to that output while the non-perfect ratios to the 5-V and 3.3-V outputs show distorted wave shapes. Without a coupled inductor, each output would have a triangular ripple voltage.

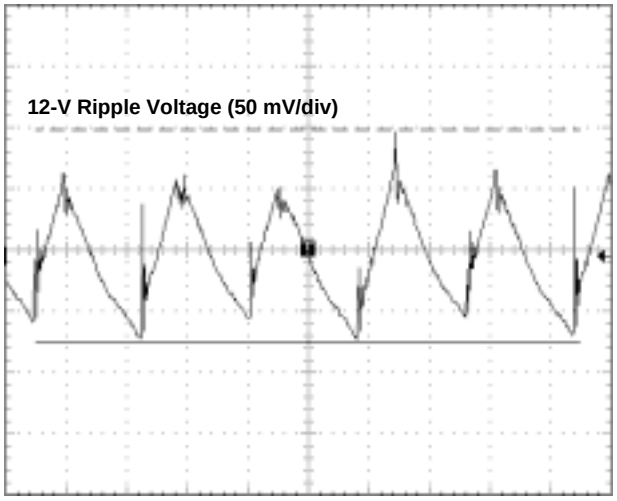

Fig. 16. 12-V Ripple voltage.

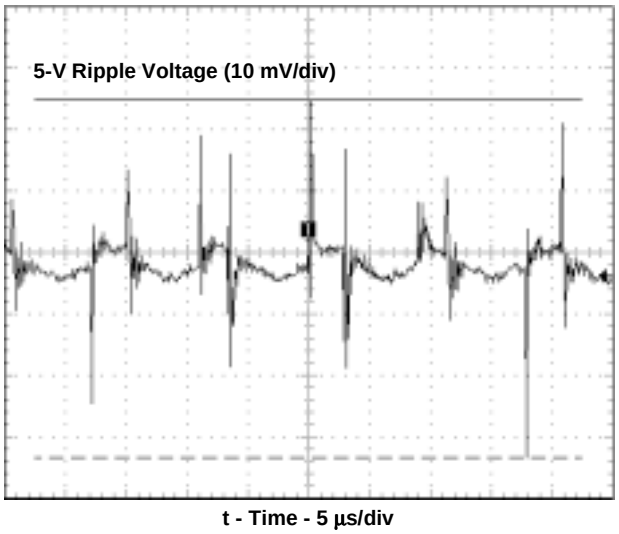

Fig. 17. 5-V Ripple Voltage.

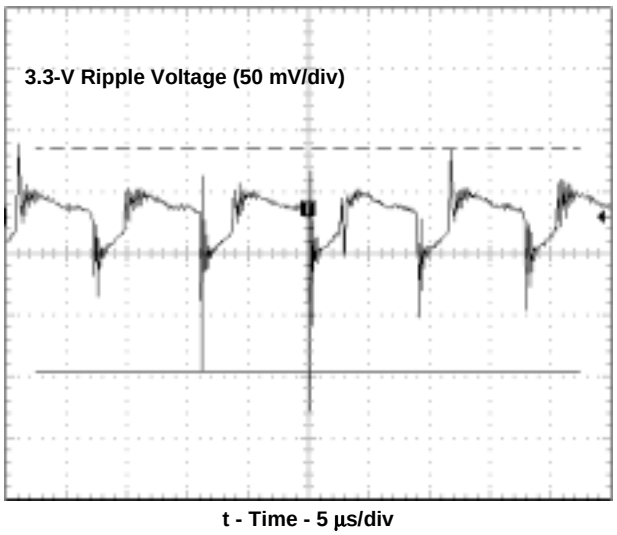

Fig. 18. 3.3-V Ripple voltage.

F. Diode Voltage

A major design factor is the voltage rating of the large 5-V schottky diode. Fig. 19 shows the measured voltage waveform on this diode at the 264 VAC high line input. The diode is conducting during the upper plateau, and the peak inverse voltage is shown at the lower plateau with a measured value of approximately -22 V. The chosen diode, IR30CPQ035 has a 35 V rating, well within the required limits. The ring on the negative portion shows that there may be a need to snub the top diode as well as the free-wheeling diode.

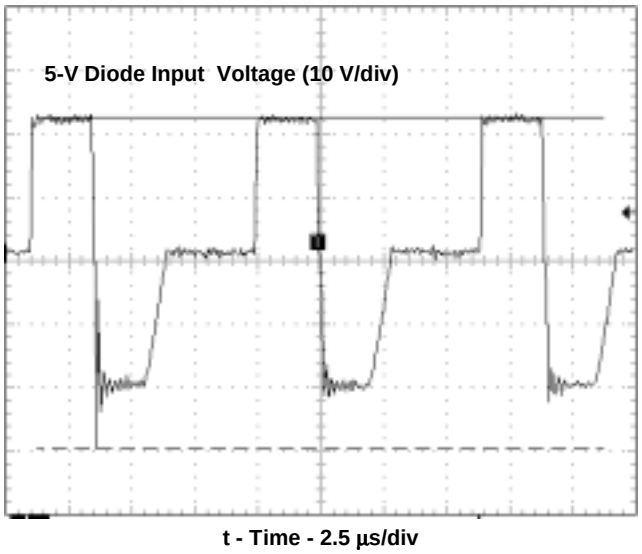

Fig. 19. Diode blocking voltage.

The free-wheeling half of the diode pair blocks the positive voltage, which is about 21 V, also well within the rating, and there is no ringing.

V. CONCLUSION

This paper discussed topics related to the design of an off-line, isolated power supply. A step-by-step process for designing the power supply was presented and followed. As with any design, there are some iterations, trial and error, and experimentation before the design is final and goes to production.

The measured results are extremely close to calculated on a first prototype. That clearly demonstrates the effectiveness of this design procedure.

The hardware demonstration would not have been possible without the help of two individuals. Mike Pantanella of TI-Manchester who created the schematic files, material lists and board layout in PCAD; and Norman Campbell at Coiltronics who crafted the transformer and coupled inductor based on my initial inputs.

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[2] Mammano, Robert, "Switching Power Supply Topology Voltage Mode vs. Current Mode," *Application Note*, April 1994, TI Literature No. (SLUA119)

[3] Dixon, L.H., "Line Input AC to DC Conversion and Input Filter Capacitor Selection," *Unitrode Power Supply Design Seminar SEM-100 Section I1*, pp 8-17 – 8-19, 1980

[4] Dinwoodie, Lisa, "Design Review: Isolated 50-W Flyback Converter Using UCC3809 Primary Side Controller and UC3965 Precision Reference and Error Amplifier," *Application Note*, September 1999, TI Literature No. (SLUA086)

[5] Gaumont, John, "Design Considerations for Transitioning from UC3842 to the New UCC3802," *Application Note*, September 1999, TI Literature No. (SLUA084)

[6] Kollman, Robert, "Achieving High-Efficiency with a Multi-Output CCM Flyback Supply Using Self-Driven Synchronous Rectifiers", *TI Power Supply Design Seminar SEM-1500, Topic* 3, pp 11-15, 2002, TI Literature No. (SLUP180)

[7] Balogh, Laszlo, "Design and Application Guide for High Speed MOSFET Gate Drive Circuits", *TI Power Supply Design Seminar SEM-1400*, Topic 2, TI Literature No. (SLUP160).

Note: References to past Power Supply Design Seminar topics can best be found on the internet at http://power.ti.com/seminars)

APPENDIX I

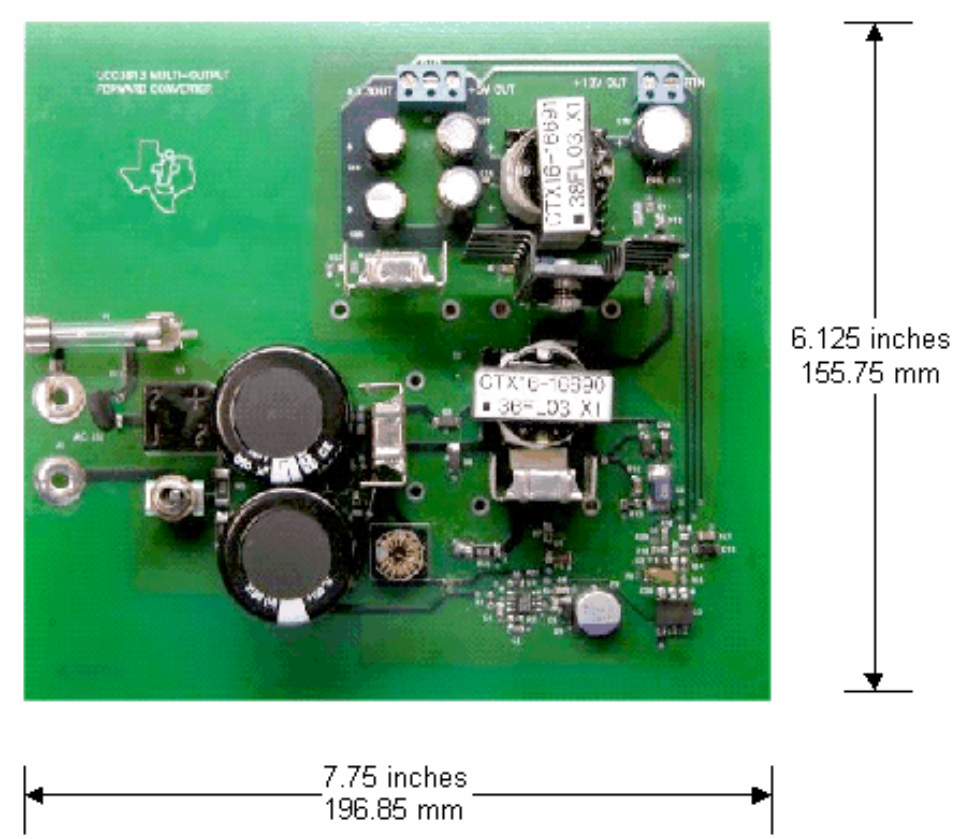


Fig. 20. Design PCB

TABLE 12. LIST OF MATERIALS

Reference Designator	Qty	Description	Size	Mfr	Part Number
C1	1	Capacitor, ceramic, 100 pF, 50 V, COG	805	Std	standard
C10	1	Capacitor, ceramic, 100 pF, 500 V, COG, ±10%	1206	Vishay	VJ1206A101KXEMT
C12	1	Capacitor, ceramic, 2200 pF, 50 V	1206	muRata	GRM42-6yyyxxxKvv
C14, C26	2	Capacitor, ceramic, 2.2 µF, 25 V, X7R	1206	TDK	C3216X7R1E225K
C19	1	Capacitor, aluminum, 560 µF, 25 V, 20%	12.5 × 20mm	Panasonic	EEU-FC1E561s
C2	1	Capacitor, ceramic, 330 pF, 50 V, NPO	805	Std	Std
C20, C25	2	Capacitor, aluminum, 2200 µF, 6.3 V, 20%	0.2	Panasonic	EEU-FC0J222
C21, C23	2	Capacitor, aluminum, 1000 µF, 6.3 V, 20%	0.2	Panasonic	EEU-FC0J102
C22	1	Capacitor, ceramic, TBD- µF, TBD-V	805	muRata	GRM40yyyxxxKvv
C24	1	Capacitor, ceramic, 1 µF, 25 V, X7R	805	Std	Std
C3, C4	2	Capacitor, aluminum electrolytic, 560 µF, 250 V	0.990 dia × 1.400"	Panasonic	EETED2E561DA
C5, C6, C7, C9, C16, C17, C18	7	Capacitor, ceramic, 0.1 µF, 50 V, X7R	805	Yageo America	08052R104K9BB0D
C8	1	Capacitor, OS-CON, 47 µF, 20 V, 45 mΩ, 20%	8.3 mm (E7)	Sanyo	20SVP47M

Reference Designator	QTY	Description	Size	Mfr	Part Number
D1	1	Diode, 6 A, 600 V, bridge rectifier	GBJ series		PB66
D10	1	Diode, dual schottky, 30 A, 35 V	TO-247AC	Int'l Rectifier	30CPQ035
D12	1	Diode, zener,10 V, 1 W	SMA	Diodes Inc.	SMAZ10-13
D2	1	Diode, schottky, 1 A, 40 V	MELF	Diodes Inc.	1N5819M
D3, D6	2	Diode, fast, 1 A, 600 V	SMA		RS1J-13
D4, D5	2	Diode, zener,12 V, 1 W	SMA	Diodes Inc.	SMAZ12-13
D7	1	Diode, dual ultrafast, 200 V, 6 A	D-PAK	Int'l Rectifier	MURD620CT
D8	1	Diode, dual schottky, 30 V, 30 A	TO-220AB	Int'l Rectifier	47CTQ020
D9, D11	2	Diode, schottky, 1.0 A, 100 V	SMA		BYS1100-13
F1	1	Fuse clip	0.205 × 0.220 ×2	Wickmann	520
J1	1	Connector, binding post, insulated, for standard banana plug, red, 15 A	0.425 dia	Johnson	111-0702-001
J2	1	Connector, binding post, insulated, for standard banana plug, black, 15 A	0.425 dia	Johnson	111-0703-001
J3	1	Terminal block, 2 pin, 15 A, 5.1 mm	0.40 × 0.35	OST	ED1609
J4	1	Terminal block, 3 pin, 15 A, 5.1 mm	0.60 v 0.35	OST	ED1610
L1	1	Inductor, SMT, 100 µH, 0.53 A, 1.1 Ω	0.35 × 0.24	Coiltronics	UP1B-101
L2	1	Transformer, 1 primary, 2 seccondary, xx mH, yyA	0.945 × 1,260	Cooper	CTX16-16691
Q1, Q2	2	MOSFET, N-channel, 500 V, 8 A	TO-220AB	Int'l Rectifier	IRF840
Q3	1	Optocoupler, 5300 V, 100% CTR	DIP6	Fairchild	4N36
R1	1	Resistor, chip, 1 kΩ, 1/10 W, 1%	805	Std	Std
R2	1	Resistor, chip, 39.2 kΩ, 1/10 W, 1%	805	Std	Std
R3	1	Resistor, chip, 43 kΩ, 1 W, 1%	2512	Std	Std
R4	1	Resistor, chip, 39 kΩ, 1 W, 1%	2512	Std	Std
R5	1	Resistor, chip, 4.7 Ω, 1/10 W, 1%	805	Std	Std
R6, R19, R22	3	Resistor, chip, TBD- Ω, 1/10 W, TBD%	805	Std	Std
R7	1	Resistor, chip, 150 Ω, 1/10 W, 1%	805	Std	Std
R8	1	Resistor, chip, 1 kΩ, 2 W, 5%	2512	Std	Std
R9	1	Resistor, chip, 4.7 Ω, 1/8 W, 5%	1206	Std	Std
R10	1	Resistor, chip, 1 kΩ, 1/10 W, 1%	805	Std	Std
R11	1	Resistor, chip, 0.39 Ω, 1 W, 1%	2512	Std	Std
R12	1	Resistor, chip, xxx- Ω, ½ W, y%	2010	Std	Std
R15	1	Resistor, chip,200 Ω, 1/8 W, 1%	1206	Std	Std
R16	1	Resistor, chip, 200 Ω, 1/10 W, 1%	805	Std	Std
R17	1	Resistor, chip, 750 Ω, 1/10 W, 1%	805	Std	Std
R18	1	Resistor, chip, 100 Ω, 1/8 W, 1%	1206	Std	Std
R19	3	Resistor, chip, TBD- Ω, 1/10 W, TBD%	805	Std	Std
R20	1	Resistor, chip, 10 kΩ, 1/10 W, 1%	805	Std	Std
R21	1	Resistor, chip, 10 kΩ, 1/10 W, 1%	805	Std	Std
RT1	1	Thermistor, 10.0 to 0.258 Ω, 3 A	0.41 × 0.12	Ametherm	SL10-10003
S1	1	Switch, SPDT, vertical PC-mount	0.500 × 0.270	C & K	7101SYCxE
SH1	1	Short jumper			
T1	1	XFMR, gate drive 1 primary, 1 secondary	0.512 × 0.480	Coiltronics	CTX08-14225
T2	1	Transformer,2 primary, 2secondary, xx mH, yyA	0.945 × 1,260	Cooper	CTX16-16690
U1	1	Low-power BiCMOS current-mode PWM	SO-8	TI	UCC3813-1D
U2	1	Precision adjustable shunt regulator	SOT23-5	TI	TL431ADBVR

Topic 4

Constructing Your Power Supply – Layout Considerations

Texas Instruments

Constructing Your Power Supply- Layout Considerations

Robert Kollman

ABSTRACT

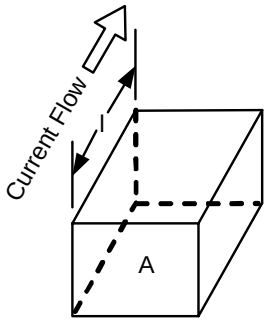
Laying out a power supply design is crucial for its proper operation; there are many issues to consider when translating a schematic into a physical product. This topic addresses methods to keep circuit parasitic components from degrading the operation of your designs. Techniques to minimize the impact of parasitic inductance and capacitance of filter components and printed wire board (PWB) traces is discussed, together with a description of the impact that PWB trace resistance can have on power supply regulation and current capacity. A general overview of thermal design is also included as well as sample temperature rise calculations in a natural and forced-air environment. Finally, some practical examples of power stage and control device layouts are reviewed.

I. INTRODUCTION

There have been numerous articles written on this subject, including Topic 2 of SEM-1500, because of its importance in ensuring a successful design. This article gathers useful guidelines and calculations to enable the neophyte as well as the experienced engineer to understand issues in physically realizing the electrical schematic. The paper covers parasitic components that can create havoc with the design with degradation in efficiency, regulation, high ripple, or just chaotic power supply operation. Included is a short section on grounding and if a more detailed discussion is desired, the reader is referred to "*Noise Reduction Techniques in Electronic Systems*" by Henry Ott [1]. One of the common problems power supply designers are facing is that their power supply is part of a motherboard and the system designers are expecting the power supply construction to be similar to the rest of the motherboard. One of these expectations may be that the power supply employs no heatsink. This means that the engineer needs to understand cooling solely provided by the motherboard surface area. Also included is a large section that discusses practical conduction, convection and radiation heat transfer. Finally, the last section provides some real world layout examples of what to do in the power stage and control section of the power supply.

II. DC PARASITICS (RESISTANCE)

In high current power supplies, resistance of components is always an issue as it degrades efficiency, can create cooling problems, and may also impact regulation. Even with it being a problem, the resistance of the PWB traces is overlooked and adds to the issue. Resistance of a conductor is easily calculated from its resistivity and physical dimensions as shown in Fig. 1. The equation states the longer the path, the more the resistance; or the greater the cross section, the lower the resistance. So a short, large cross section conductor would be desirable to control interconnect resistance. Fig. 1 also presents the resistivity of some common materials that may be found in power supply construction. One interesting point is that plated copper is much more resistive than pure copper. This is important to understand in power supplies because plating is used to form vias to make interconnect in PWBs and also plating is applied to the surface of the PWBs to increase the copper thickness. Many times surface layers are "1 plate 1" meaning the starting copper material is 1-oz (or 1.4 mils or 0.4 mm) thick and an additional 1 oz of copper is plated on to form vias and increase the surface thickness. The surface resistance reduction will only be about 25% of what one may expect. Another interesting point is that solder materials such as tin-lead or other plating materials such as tin are not very good conductors.



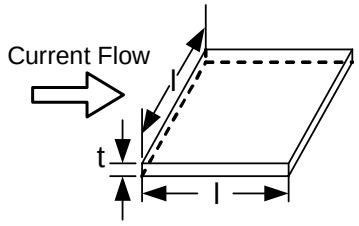
$$R = \frac{\rho l}{A}$$

Fig. 1. Sample resistance calculation and common resistivities.

TABLE 1. SAMPLE RESISTIVITIES (25ºC)

Material	μΩ-cm	μΩ-in
Copper	1.70	0.67
Copper (Plated)	6.0	2.36
Gold	2.2	0.87
Lead	22.0	8.66
Silver	1.5	0.59
Silver (Plated)	1.8	0.71
Tin -Lead	15	5.91
Tin (Plated)	11	4.33

A simple way to estimate the resistance of PWB traces is presented in Fig. 2. The first step is to calculate the resistance across a square of conductor. From the resistance formula, if the conductor width and length are equal, they cancel out and the square resistance is dependent only on thickness and resistivity. Table 1 presents sample calculations for a number of common trace thicknesses and temperature. Note that at 100ºC resistance increases by 30%. The resistance of copper varies linearly with temperature and doubles from 25ºC to 279ºC. Once the square resistance is calculated, the designer can then estimate the number of squares in the PWB trace and multiply by the square resistance to calculate total resistance. Remembering that a square of 1-oz copper has about 0.5 mΩ of resistance is much easier than remembering the resistivity of copper and measuring trace widths and lengths.



$$R = \frac{\rho l}{(tl)}$$

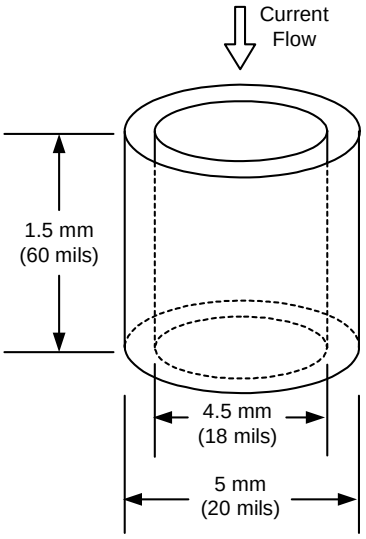
$$R = \frac{\rho}{t}$$

Fig. 2. A PWB trace square has constant resistance.

TABLE 2. PWB TRACE RESISTANCE

Copper Weight (Oz.)	Thickness (mm/mils)	mΩ per Square (25ºC)	mΩ per Square (100ºC)
1/2	0.02/0.7	1.0	1.3
1	0.04/1.4	0.5	0.6
2	0.07/2.8	0.2	0.3

An often overlooked current path is through vias from the front to back of the board and they can have significant resistance. Fig. 3 presents a sample calculation for a via through a 1.5-mm (0.060 in) thick PWB. A plated wall thickness of 0.03 mm (1 mil) and a plating resistivity of 6 μΩ/cm (2.4 μΩ/in) are assumed and a resistance of 2.4 mΩ was calculated. While this may not sound significant, if this were the only path for a 10-A output, it would result in ¼ W of dissipation and in a voltage drop of 24 mV. For a 1.2-V output, this could be 2% load regulation degradation. A typical rule of thumb limits the current through vias to between 1 A and 3 A. Not only should the output path for the power supply be scrutinized, but high-current AC paths around switching devices need to be considered. Note that there can be voltage drops from the point of regulation to the load and a good design will place the point of regulation as close to the load as possible.



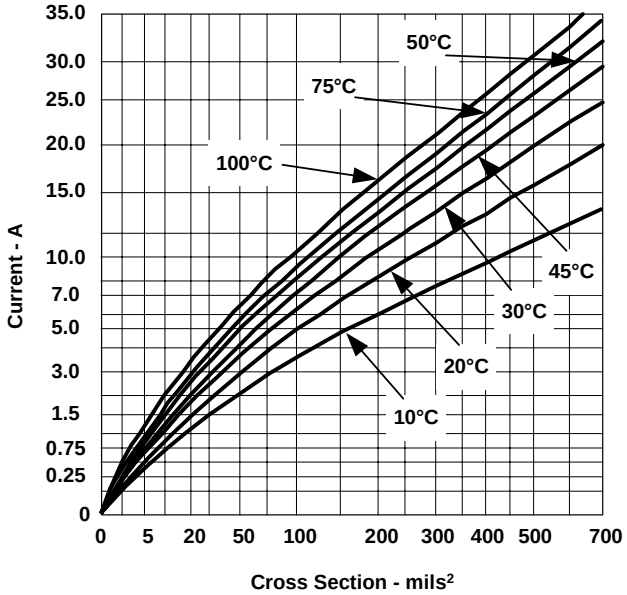
$$R = \frac{\rho l}{A}$$

$$R = \frac{\rho l}{\pi(r_o^{\,2} - r_i^{\,2})}$$

$$R = \frac{2.36\times10^{-6}\times0.06}{\pi(0.01^2 - 0.009^2)} = 2.4\ m\Omega$$

Fig. 3. Vias have resistance too!

A second consideration in sizing PWB traces, in addition to voltage drop, is the temperature rise of the conductor. As discussed with the vias, even a few milliohms of resistance can generate significant power and consequently significant temperature rise. The Institute for Interconnecting and Packaging of Electronic Circuits (IPC) has published Fig. 4 in IPC-2221A to be used as a guideline in determining appropriate conductor widths for a given temperature rise. This data was created in the early 1950's and is very conservative. IPC recognizes that this data is conservative and has a task underway to update and add to this information under IPC 1-10b Current Carrying Capacity Task Group and expects to have review information available during 2003. As a example of the use of the chart, consider a 0.1-inch wide, 1-ounce trace. For 10ºC rise, the conductor current carrying capacity is 4 A, and for 45ºC rise it would be 9 A. These curves show extremes of how much current a trace can carry, but do not comprehend voltage drop. Consider a 1-ounce, 1-inch long by 0.1-inch wide trace. It is 10 squares long and with 0.5 mΩ per square, it has a resistance of 5 mΩ. So 10ºC rise equates to a 20-mV drop and 45ºC rise equates to a 45-mV drop. Usually these types of drops are excessive, particularly in 1-V power supplies, so if the conductor is sized properly for good regulation, temperature rise should not be a problem.



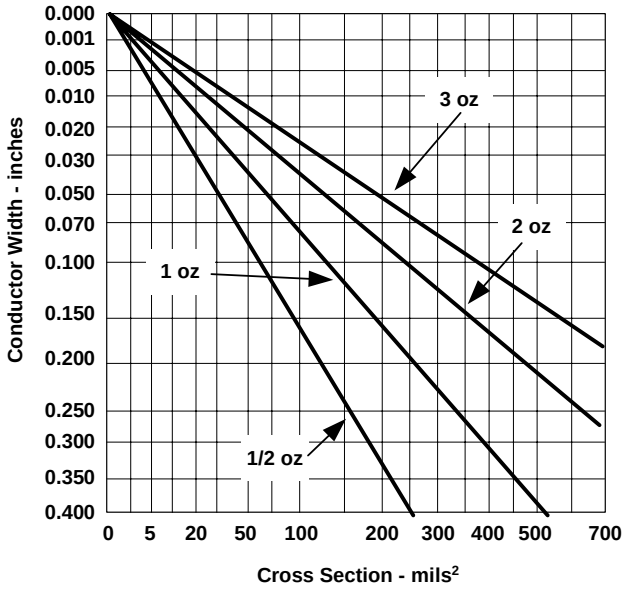


Fig. 4. IPC's conservative current derating guideline.

Some of the printed circuit traces may have large AC current components. Depending upon skin and proximity effects, AC resistance could conceivably be much greater than DC resistance, with high AC losses. Current distribution in these traces is determined by their physical size and proximity of return paths for the current. As an extreme example, a current in a trace far away from the return path tends to gather toward the edges of the conductor at a thickness of one skin depth. So even with a very wide conductor, high-frequency currents may use only a small portion. With a trace over a return path, the current pulls toward the opposing surfaces. If the trace is thicker than one skin depth, AC current flows only on the inner surface of the trace facing the opposing conductor – the outer surface carries little current. However, skin depth in copper is 0.25 mm at 100 kHz, and varies inversely with the square root of the frequency. Thus, even at 1 MHz, AC current penetrates through the entire 0.07-mm thickness of a 2-oz. copper trace. Therefore, in most applications, the AC resistance of a printed circuit trace is not significantly greater than its DC resistance.

III. AC Parasitics

Just as PWB traces add unseen resistors to schematics, they can also add inductors, capacitors, and transformers. Fig. 5 illustrates that parasitics can destroy the performance of a capacitor even before it is mounted. The impedance of four different styles of capacitors was measured. At low frequencies, they all exhibit the expected diminishing impedance as the frequency is increased. However, they each reach a frequency where the impedance no longer decreases, but instead, starts to increase. This increasing impedance is caused by the equivalent series inductance (ESL) of the part which to a first order can be estimated by the physical dimension of the part and the rule of thumb for the inductance of a conductor of 6 nH/cm (or 15 nH/in). For instance, the 10-µF ceramic capacitor is about 0.5 mm (or 0.12 in) long, and would have an estimated inductance of 0.5 mm x 6 nH/mm = 3 nH. The right side of the chart is marked with the impedance of 1-nH and 5-nH inductors and the correlation is good for the ceramic and the larger electrolytic capacitors. Also, note that it doesn't take much printed circuit trace inductance (or length) to further degrade the capacitors.

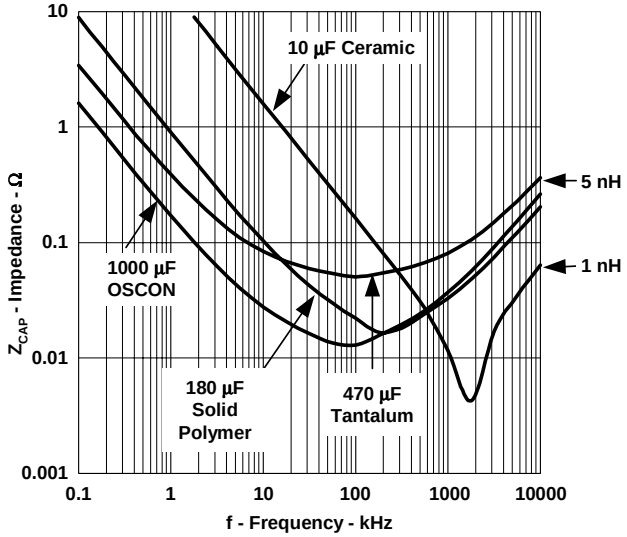
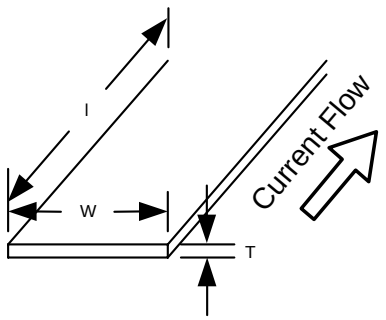


Fig. 5. Before capacitors are even mounted, parasitic inductance is evident.

Fig. 6 provides a precise inductance calculation. This is for a PWB trace in free space and is taken from page 35 of Grover [6]. An important note on all inductance formulas is that many are empirical, and it is very important to understand the allowable extremes of the variables. This particular one is good for large extremes of variables. It calculates the rule of thumb 6 nH/mm (or 15 nH/in). It is interesting to note that due to the natural log relationship, large changes in conductor width have minimal impact on inductance. With a 50-to-1 increase in conductor width, inductance is only decreased by a factor of four. This means it is a real problem trying to drive down the inductance of an isolated trace!



$$L = 2l\left(\ln(\frac{l}{(T+W)}\right) = \frac{1}{2}) \; nH(cm)$$

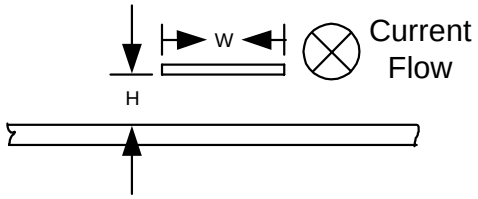
$$L = 5l\left(\ln(\frac{L}{(T+W)}\right) + \frac{1}{2}) \; nH(in)$$

Fig. 6. Self-inductance equation aligns with 6 nH/cm (15 nH/in) rule of thumb.

TABLE 3. INCREASING CONDUCTOR WIDTH REDUCES ITS INDUCTANCE SLIGHTLY

W (mm/in)	T(mm/in)	Inductance (nH/cm or nH/in)
0.25/0.01	0.07/0.0028	10/24
2.5/0.1	0.07/0.0028	6/14
12.5/0.5	0.07/0.0028	2/6

Fig. 7 provides an expression to calculate inductance of a trace over a ground plane from Reference [7]. This is a transmission line calculation and it is only good for large ratios of conductor trace widths to separation from the ground plane. One key point in the formula is that the inductance is proportional to spacing and inversely proportion to conductor width. This means that there is much more control of inductance as compared to an isolated conductor. A second point is that the inductance is proportional to the area enclosed by the conductors. To minimize inductance, one needs to minimize the area enclosed by the current flow. This is generally the case, even in the absence of a ground plane. Fig. 7 also provides a couple of sample calculations. The first is representative of a trace in a multi-layer board over an adjacent ground plane. Note when compared to Fig. 6, the inductance has been reduced by a factor of thirty. It could be further reduced by widening the conductor. The second example inductance is that of a typical two sided board, one side ground plane and the second the conductor. Note that even in this case, the ground plane provides a 5-to-1 reduction in interconnect inductance.



$$L = \frac{2Hl}{W} \text{ nH/cm}$$

$$L = \frac{5Hl}{W} \text{ nH/in}$$

Fig. 7. Trace over ground plane significantly reduces inductance.

TABLE 4. CONDUCTOR OVER PLANE DRAMATICALLY REDUCES INDUCTANCE

MetricC			English		
H (cm)	W (cm)	Inductance (nH/cm)	H (in)	W (in)	Inductance (nH/in)
0.25	0.25	0.2	0.01	0.1	0.5
0.15	2.5	1.2	0.06	0.1	3.0

It should be noted that the effectiveness of the ground plane depends upon it being significantly wider than the trace above it. For example, if the ground plane were the same width as the trace above it in Fig. 7, the resulting symmetrical conductor pair has a total inductance per unit length slightly greater than the value calculated by the formula of Fig. 7. However, this total inductance value is distributed so that one half appears in series with each conductor. Thus, the lower conductor is no longer an effective ground plane. When the lower conductor is made significantly wider, the asymmetrical structure causes almost all of the total inductance to appear in series with the smaller conductor, thereby minimizing the impedance in series with the wider ground plane.

For capacitors to be effective, whether they are bypass or output capacitors, they need to be connected with minimal lead inductance. As the first step of the layout process, the designer should draw the schematic so the layout person knows the critical routes. The second step is the power supply designer should either plan the connections or review them. The designer should use minimum lengths on high di/dt paths; use ground planes where possible, bring current paths across capacitor terminals, and minimize bypass loop area. If a multilayer PWB is used, a ground plane is a very good idea and it should be as close to the surface of the board as possible to further minimize bypass loop area.

The designer should also consider paralleling different capacitor types for reduced impedance across the frequency band. Fig. 8 provides a good example of the advantage of this approach. It shows three impedance curves versus frequency, the first is an aluminum electrolytic capacitor, the second is a ceramic and the third is the parallel combination of the two. The electrolytic capacitor has low impedance at low frequency, but it quickly runs into its equivalent series resistance (ESR) and its impedance does not decline any further. The ceramic capacitor has a relatively high impedance at low frequencies, but since it has little ESR, its impedance is less than the ESR of the electrolytic. By paralleling the two capacitors, one can obtain low impedance across a wide frequency band. A side benefit is that the ESR of the electrolytic capacitor can damp circuit resonances. Note that the impedance does start to increase at the higher frequencies due to the ESL of the ceramic capacitor. One could consider paralleling different ceramic capacitors values to reduce impedance in the 2-MHz to 20-MHz frequency range (0.1 μF and 0.01 μF). However, this reduction will only be possible if the inductance of the smaller value capacitors is less than the large one and, in general, this means that the higher frequency capacitors need to be physically smaller.

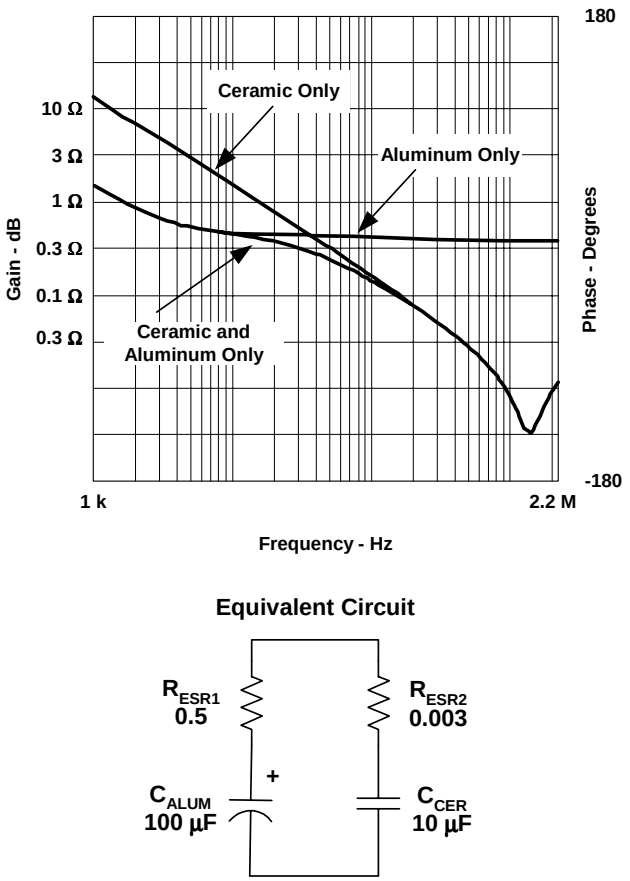


Fig. 8. Paralleled capacitors minimize impedance over frequency.

Fig. 9 presents the impedance of a common mode inductor versus frequency. At low frequency, the impedance rises as expected but at high frequency, the inductor impedance takes on a capacitive response. This is called *distributed capacitance* and is a result of winding to winding capacitance. This is an extreme example but any inductor has a similar response. It may not turn capacitive at as low of a frequency but typical distributed capacitances are in the 10-pF to 100-pF range. Just as in the case of capacitors, one can further degrade an inductor's characteristic by mounting it on a PWB.

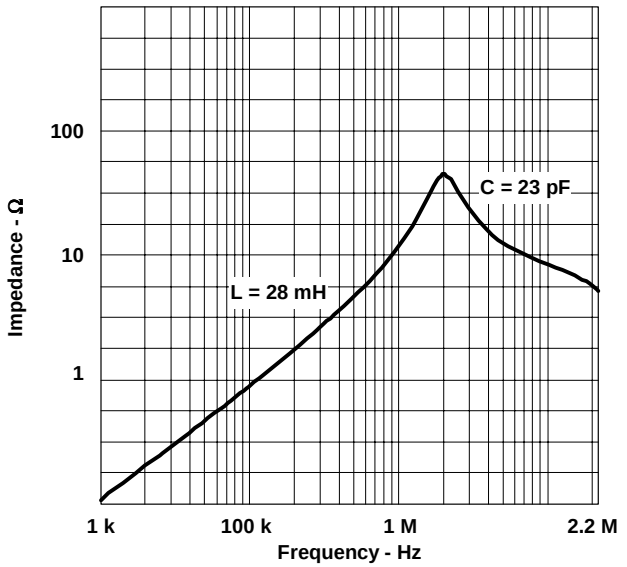


Fig. 9. At high frequencies, inductors turn into capacitors.

Fig. 10 provides a formula to calculate the capacitance from layer to layer in a PWB. The capacitance is related to the permittivity, relative permittivity, area, and thickness. Permittivity is a constant equal to $1/36\pi\times10^{-9}$ F/m whereas relative permittivity is material related. For typical PWB material, relative permittivity is about 5 F/m. The only real variables the designer has at his control is area and spacing. For low capacitance between conductors, the area should be minimized and spacing should be maximized. It can be seen from the sample calculation that 0.25 mm (10-mil) conductors crossing each other in a multi-layer board have a minimal amount of capacitance.

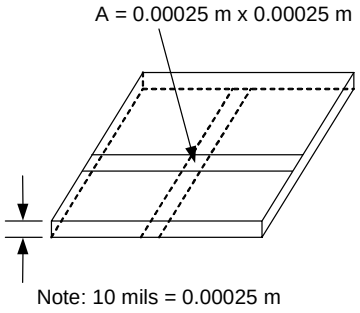


Fig. 10. Sample area to visualize capacitance calculation.

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

$$C = 5\left(\frac{10^{-9}}{36\pi}\right)\left(\frac{0.00025^2}{0.00025}\right)$$

$$C = 0.01\ pF$$

Crossing traces are generally not an issue due to the small capacitance. Capacitance coupling issues usually involve planes, a number of component pads or parallel conductors. For instance, Fig. 11 shows how plane capacitances can further degrade a common mode inductor. In this example, the ground plane is continuous under the inductor and there are large planes connecting the power to the inductor. This creates a significant amount of capacitance from input to ground and then to output, and adds appreciably to the distributed capacitance of the common mode inductor. To properly connect this inductor, the ground plane should not extend past the inductor, and the area connecting the leads should be minimized to avoid induced currents.

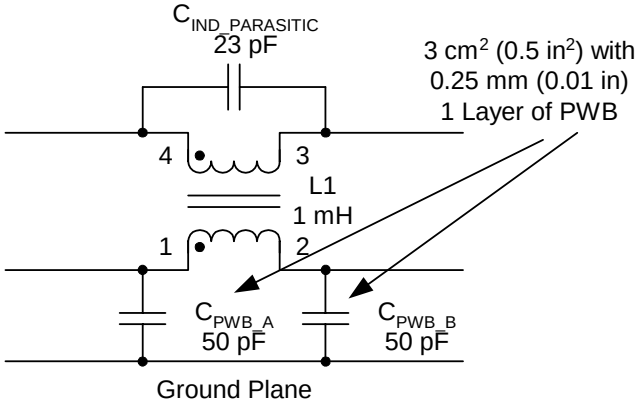


Fig. 11. Ground plane capacitance shorts common mode inductor.

The most serious parasitic capacitance issue usually involves connecting the feedback (FB) voltage and compensation of the error amplifier. This is due to the fact that it involves a high-impedance node, a lot of gain in the error amplifier and a large number of components connected to this node. Fig. 12 shows this trouble spot in a typical controller and one of the more likely coupling nodes. The connection between Q1 and D1 has very high slew rates in the order of 0.1 V to 1 V per ns and can create 1 mA of current with only 1 pF of parasitic capacitance. Typically, the impedance on the feedback and compensation nodes are on the order of 1 kΩ to 10 kΩ so this current can create significant voltage perturbations on the error amplifier input. This is usually manifested as erratic gate drives or a perceived oscillation as the power supply tries to correct for the error injected from the noise source. The most successful designs recognize this fact and draw the schematic so that the compensation components are shown in the vicinity of the error amplifier to imply a recommended routing. Then the power supply designer needs to make sure that the components are compactly placed near the error amplifier and that the traces that connect them are short. Also, the designer needs to make sure that there is not a high dV/dt trace in the vicinity of these components; this includes the switch node and gate drive signal. Finally, there is a preferred connection for the resistors and capacitors in the compensation circuit as shown in Fig. 12. It is best to connect the resistors to the FB pin because they can provide a little attenuation of an injected signal. For instance, if R9 and C7 were reversed, and a high frequency signal was applied to their common node, it would also show up on the FB pin with little attenuation. In the proper connection, R9 working against the other resistors in the compensation circuit and the input impedance of the error amplifier will provide some attenuation and a little less noisy power supply.

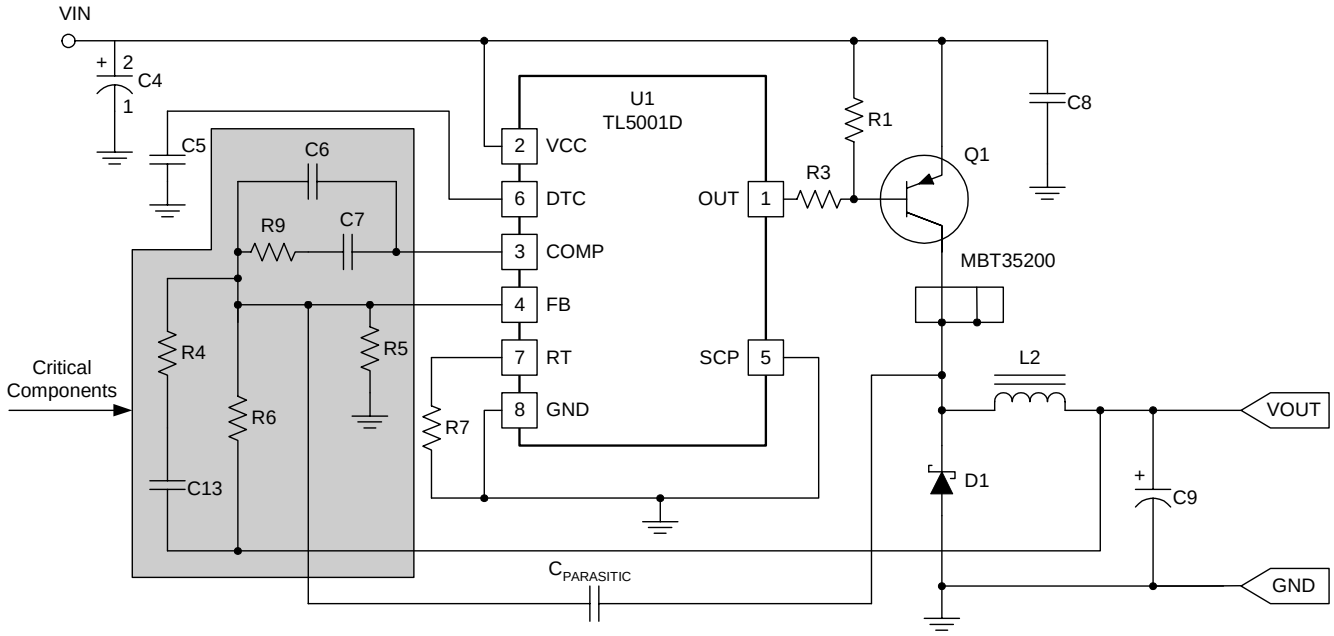


Fig. 12. FB and comp connections are the most critical route in the power supply.

Fig. 13 illustrates magnetic coupling between circuits. In this case, it is between two toroidal inductors. Each inductor represents a single loop of wire with a diameter about equal to the diameter of the inductor. Current flowing in one induces a current flow in the second. Normally, this is not an issue if these are both power components in a topology like SEPIC. However, it can become quite an issue if these are filter inductors. In a filter, it may be desirable to have 100 dB of current reduction between the two inductors and it would not be physically realizable with this layout. To improve the situation, the inductors should be oriented such that flux generated in one can not link into the second one. Shields or different core geometries are also alternative solutions. Similar situations can also occur in poorly constructed power stages. If care is not exercised to minimize the inductance of the power stage and input capacitor connections, single turn inductors with large loop areas can be created. They generate a magnetic field that couples into other loops like toroid inductors and EMI measuring devices.

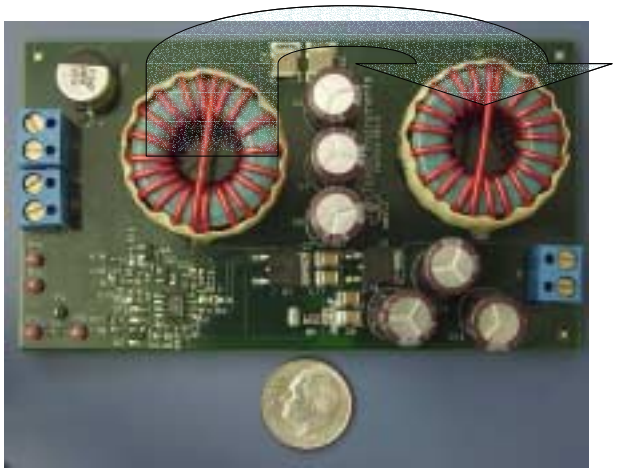


Fig. 13. Coupling between inductors can degrade filter response.

In summary, the layout of the power supply is crucial to maintaining the high frequency characteristics of the power components, thus providing a satisfactory design. Unintended inductance can ruin the filtering effects of capacitors and is especially important in low impedance circuits such as filters, power switching, and timing. To minimize inductance, use ground planes and wide conductors and strive to minimize the loop area of all high di/dt circuits. Unintended capacitance can also ruin the high-frequency performance of inductors and is especially important in high-impedance circuits such as filters and amplifiers. To minimize capacitive effects, use careful layout techniques and also shielding. Pay particular attention to error amplifier inputs and their physical relationship to high dV/dt traces on the board. A ground between a noisy circuit and a sensitive circuit can help divert parasitic currents; this is especially true if multilayer PWBs are used. In this case, power connections can be made on one side of the ground plane and low level connections can be made on the other. The final coupling mechanism is magnetic which is created by high di/dt currents flowing through circuit loops. These effects are best minimized by minimizing loop areas and by providing some shielding with ground planes. Also, watch out for emissions from devices such as toroid inductors as they can couple into other parts of the circuits. If multiple toroids are involved in a filter design, orient them at right angles (ie; horizontal and vertical) so they can not couple.

IV. GROUNDS AND GROUNDING

As with layout, grounding is one of those things that must be done correctly for a functioning system. It is very important to start a system design with a plan for grounding in the form of a system ground chart. This chart should contain the various subsystems and a plan for connecting their various grounds together. This paper introduces concepts and makes recommendations for handling the ground within the power supply portion of the system. For a thorough discussion on grounding, refer to [1].

The reason grounding is such an important topic is that there is current flow between the various elements of the system and if there is an impedance (and there always is), a voltage drop is generated. This voltage drop can degrade system performance by reduced noise tolerance for digital systems, or voltage offsets in analog systems leading to sensing errors. The currents between the subsystems can take a number of forms, it can simply be DC current as power is distributed throughout the systems, it can be common mode current that is generated by power supply, it can be lower frequency AC current either from the mains or motors or solenoids, or it can be radio frequency created by transmitters. Whatever the source, the ground plan should comprehend the current's nature and plan for a low impedance return path.

Fig. 14 presents two common ground schemes for a system. In the series connection, the subsystems are daisy chained together to provide the current return path. In this plan, ideally, box 1 would represent the highest current draw followed by box 2 and then box 3. In this manner, the highest current draw and presumably highest voltage drop would be eliminated from common current paths. This is the simplest grounding scheme but has the drawback that the additive effect of the ground currents from each subsystem generates differential voltages between the subsystems. Also, the inductance of these connections can be quite high. The parallel connection helps to mitigate some of these issues. In this scheme, the subsystems are connected to single point ground in a star arrangement. Current flow in these ground connections are only from the subsystem itself. This reduces the current flow in the ground connections and thereby reduces some of the differential voltage differences between the subsystems. This is a more complicated wiring scheme and has the drawback that the wiring can be high impedance at high frequency.

The ideal case for a ground system is presented in Fig. 15. In this approach, the various subsystems are interconnected through a very low-impedance ground plane. The ground plane is made significantly thick enough to eliminate differential low-frequency voltages and interconnect inductance is minimized much in the same way inductance of a conductor is minimized when it is put over a ground plane. This is the preferred approach for a power supply layout whether it is a two-sided PWB or multilayer.

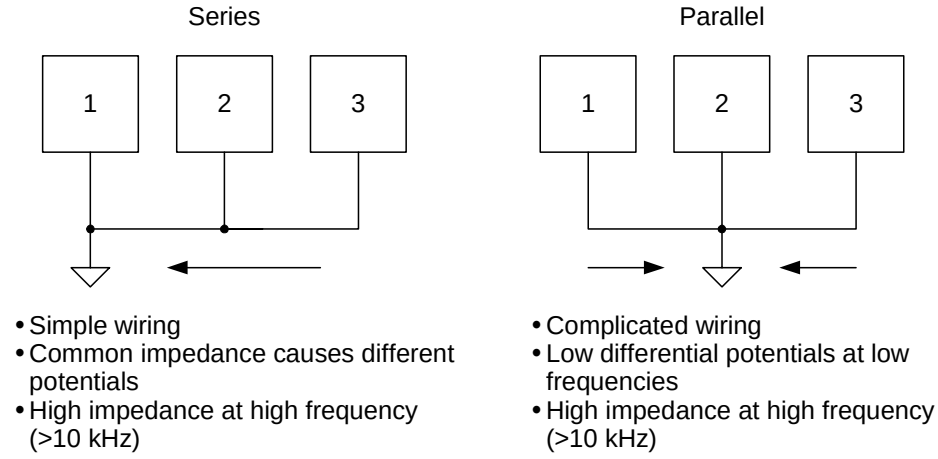


Fig. 14. Two different single point grounds.

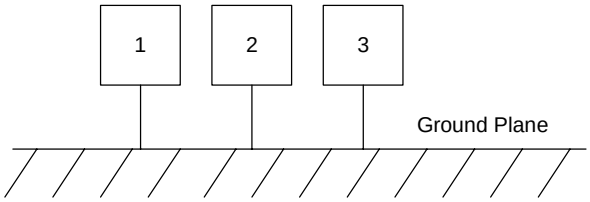


Fig. 15. Ground plane provides near ideal single point ground.

Fig. 16 shows the AC current path in a buck power stage. It is important to recognize that while the ground plane impedance is low, it is not zero so any current flowing in the ground plane generates voltages that may cause problems. In this case, it is desirable to minimize the path length between pin 2 of Q4 and the negative terminal of C3. A second high frequency current path not shown is from the control IC's gate drive terminal through Q4 gate to source and back to the control IC. Inductance in the source connection to the control IC slows switching time appreciably so that the best design would take the Q4 source connection directly to the ground plane and locate the IC as close as physically possible.

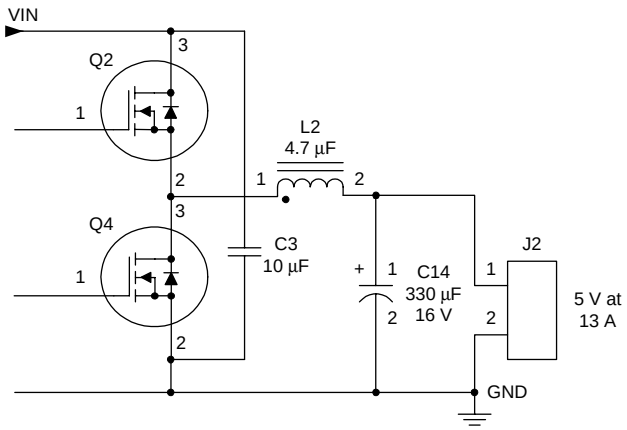


Fig. 16. Minimize high AC currents in ground plane.

An often overlooked feature of many control ICs is that pins are selected with a plan. Fig. 17 illustrates this point. All the pins on the left side of the IC are analog with a degree of noise sensitivity. If these pins are inadvertently routed near some of the more noisy pins on the right side of the control IC, sufficient noise pick-up could happen to create chaotic converter performance. So for this IC, layout all the low level passive components to the left, and place the power stage to the right of the IC. Other ICs split the analog power lengthwise, and work best with power stage and power split accordingly. A second point is that this IC has a signal ground (SGND) and power ground (PGND) to minimize interaction between the noisy power circuits and the sensitive analog circuits and best performance is found with a direct connection of both pins to the ground plane. The same thing is true for connections of bypasses and timing components, place them close together and take them directly to the ground plane.

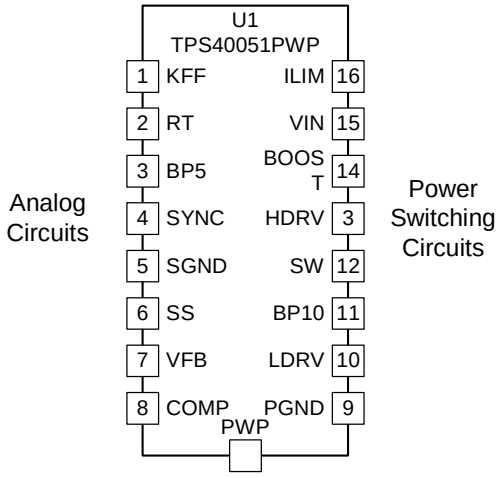


Fig. 17. Most control ICs have a planned layout.

V. THERMAL CONSIDERATIONS

One of the key layout considerations in a power supply is removing the heat from components. Historically, that meant figuring out which components generated significant heat and mounting them to a heatsink. But as the power supply becomes integrated with the system, mounting components to a heatsink is becoming less attractive and there is a move to have the PWB act as the heatsink.

There are a number of ways to move heat including conduction, convection and radiation and the power supply design uses all three. For electrical engineers, it is useful to translate the cooling process into an electrical circuit analogy. Heat can be thought of as a current source, temperature as a voltage, and conduction, convection and radiation paths can be thought of as resistances. Fig. 18 shows the electrical analog of a semiconductor dissipating heat and its cooling path. The heat, which is treated as a current source, flows from the semiconductor die through the package to an interface and then into a heatsink. Traditionally, this was a fairly easy circuit to analyze. The heat could be calculated, the semiconductor manufacturer provided the thermal resistance of the package (in ºC/W), there was characterization data on the package to heatsink interface available and the heatsink manufacturer provided its thermal resistance. So the engineer simply needs to multiply power times the sum of the thermal resistances to calculate temperature rise above ambient.

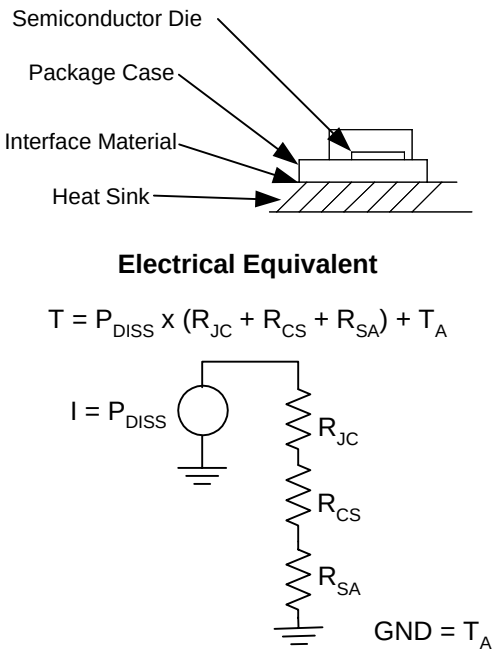


Fig. 18. Electrical equivalent circuit of heat transfer problem.

- R_{JC}: junction to case thermal resistance, usually specified
- R_{CS}: interface resistance, specified for heat sink insulators, neglectable for solder connections
- R_{SA}: sink to ambient resistance, specified for heatsinks otherwise very nebulous
- T_A = ambient

Things are changing as the power supply is tending to be integrated within a system. Fig. 19 provides a cross section of such an implementation. Rather than mounting to a heatsink, the power device is mounted to a multilayer PWB. Heat flows from the power device into the PWB where it is conducted laterally through copper conductors within the board. Cooling is provided by the surface of the PWB with both convection and radiation heat transfer. The analytical problem is greatly complicated as the only known quantities are the heat within the power device and its thermal resistance from junction to its case or to its leads. The following section provides some insight into this cooling strategy by discussing conduction heat transfer within the PWB and then convection and radiation from its surfaces.

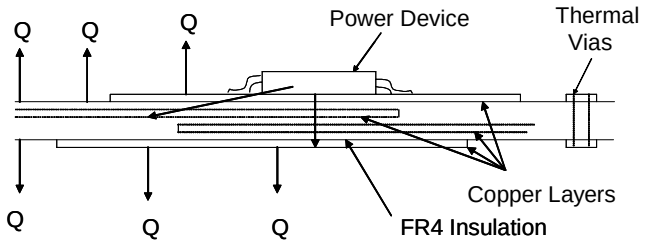


Fig. 19. Heat flow in a multilayer PWB.

To start to understand the problem, consider a typical thermal environment of an ambient temperature of 70ºC, a maximum semiconductor junction temperature of 125ºC, and a semiconductor loss of 2 W. If this semiconductor were in a power pad SO-8, its junction-to-board thermal resistance might be specified as 2.3ºC/W by the manufacturer and the calculated maximum allowable PWB temperature under the semiconductor is 5ºC – 2 W × 2.3ºC/W = 120ºC. Then consider where the heat goes from there. To a first approximation, temperature rise is proportional to power dissipation (P) and inversely proportional to surface area (Sa). The proportionality constant, h, is called the heat transfer coefficient and is about 0.001 W/cm^2/ºC (or 0.006 W/in^2/ºC) for still air. So temperature rise can be calculated using the following expression:

- Metric (cm, W, ºC)

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.001)}$$

$$\Delta T = \frac{1000 \times P}{Sa}$$

$$R_{SA} = \frac{1000}{Sa}$$

- English (in, W, ºC)

$$\Delta T = \frac{P}{(Sa \times h)} = \frac{P}{(Sa \times 0.00)}$$

$$\Delta T = \frac{166 \times P}{Sa}$$

$$R_{SA} = \frac{166}{Sa}$$

We also solved for an equivalent thermal resistance (R_{SA}) as function of surface area. Note that 0.1 W of power distributed over a square centimeter, single sided surface yields about 100ºC rise (or 1 W over 1 square inch gives 166ºC rise). Applying our simple formula and solving for the area to needed to provide a 50ºC rise (120ºC – 70ºC):

- Metric (cm, W, ºC)

$$\Delta T = \frac{P}{Sa \times 1000}$$

$$Sa = \frac{P}{\Delta T \times 1000}$$

$$Sa = \frac{2}{50 \times 100}$$

$$Sa = 40$$

- English (in.,W, ºC)

$$\Delta T = \frac{P}{Sa \times 166}$$

$$Sa = \frac{P}{\Delta T \times 166}$$

$$Sa = \frac{2}{50 \times 166}$$

$$Sa = 7$$

The package is much smaller than this dimension and something must be done to provide a larger cooling surface. Either a heatsink must be used or the heat must be spread laterally in the PWB and convected through its surface.

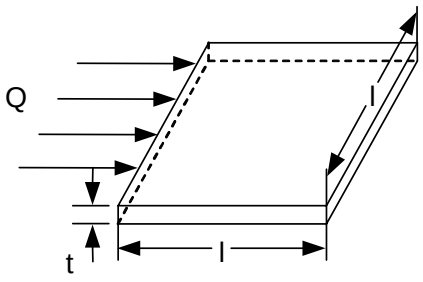


Fig. 20. Lateral heatflow is through copper conductors rather than board material.

TABLE 5. LATERAL THERMAL RESISTANCE OF A COPPER PLANE AND PWB MATERIAL

Metric	English
2-oz, 0.07-mm thick copper	**2-oz, 2.8-mils thick copper**
$R = \frac{l}{(\sigma \times l \times t)} = 1/(\sigma \times t)$ $R = \frac{1}{(0.4 \times 0.07)}$ $R = 40^{o}C/W$	$R = \frac{l}{(\sigma \times l \times t)} = \frac{1}{(\sigma \times t)}$ $R = \frac{1}{(9 \times 0.0028)}$ $R = 40^{o}C/W$
1.5-mm FR4	**0.06-inch FR4**
$R = \frac{1}{(0.00028 \times 1.5)}$ $R = 2400^{o}C/W$	$R = \frac{1}{(0.007 \times 0.06)}$ $R = 2400^{o}C/W$

Lateral thermal resistance is much like electrical resistance and can be calculated as shown in Fig. 20. (For reference other thermal conductivities can be found in the appendices). The resistance is increased by length and reduced by cross sectional area and thermal conductivity. Two possible paths are presented in the figure, through the PWB material and through a copper layer in the PWB. A 1.5-mm (0.06-in) PWB is compared to a 0.07-mm (0.0028-in) thick copper plane. Even though the PWB material is much thicker then the copper, the high copper thermal conductivity makes it a much lower resistance path for heat flow. The strategy to use the PWB surface as the cooling surface must include making use of the copper within the board to spread the heat. Also, note that just as with the electrical resistance of conductors, you can count squares of thermal conductors to estimate the thermal resistance from point to point.

The next possible path to consider is through the PWB to the other surface. Fig. 21 shows the calculation for two 2.54-cm (1-in) square planes separated by 1.5-mm (60-mil) PWB thickness, (board front to back). The low thermal conductivity of the board is offset by the large area and short path length and thermal resistance of 8ºC/W is calculated. This number is small compared to the 166ºC/W board to air resistance so heat is dissipated from both sides of board.

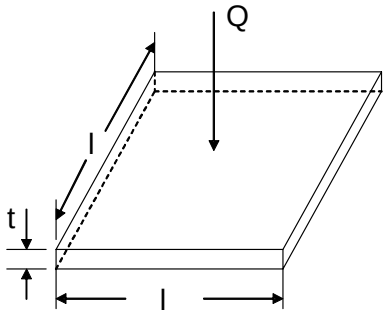


Fig. 21. Specific thermal resistance through board is much less than board-ambient.

$$R = \frac{t}{(\sigma \times A)}$$

$$R = \frac{1.5}{(0.00018 \times 2.54 \times 2.54)} \quad \text{Metric}$$

$$R = \frac{0.06}{(0.007 \times 1)} \quad \text{English}$$

In some cases, a heatsink is affixed to the backside of the PWB and heat is transferred through the board into the heatsink. Sometimes this thermal resistance may be too high. Vias offer a method to further reduce the side-to-side thermal resistance. A few vias can halve the thermal resistance from board front to back, and a large number can reduce the thermal resistance down to the 1ºC/W range. Fig. 22 shows a typical via and provides the calculation of its thermal resistance. For this sample via, thermal resistance is about 100ºC/W and it only takes 12 of these in parallel to halve the thermal resistance through the PWB board material. Solder filling or further plating can yield significant improvement over this number.

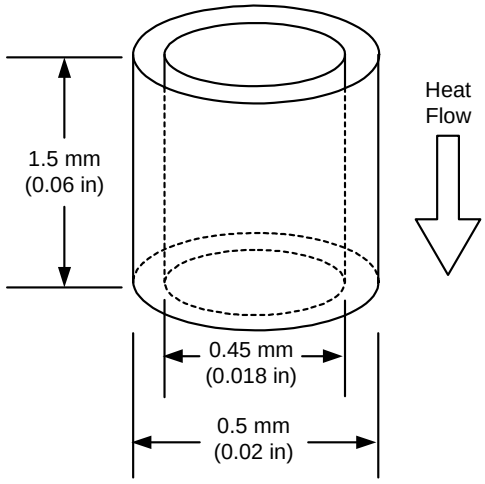


Fig. 22. A single via has about 100ºC/W thermal resistance and they can be paralleled.

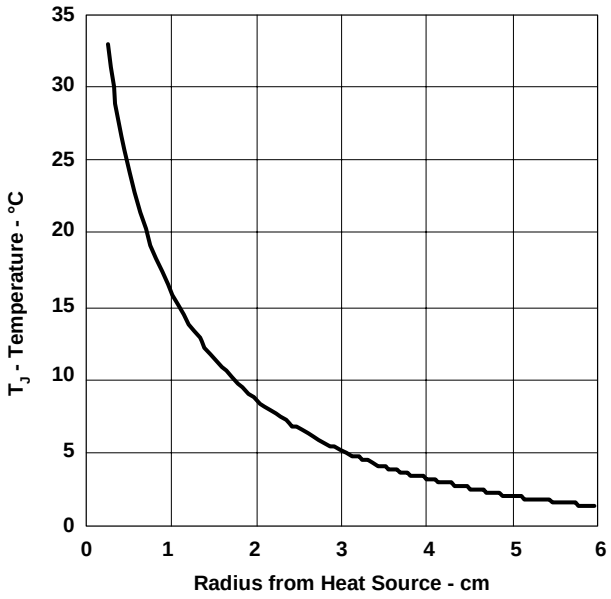
$$R = \frac{l}{(\sigma \times A)}$$

$$R = \frac{l}{(\sigma \times \pi \times (r_o^{\,2} - r_i^{\,2}))}$$

$$R = \frac{1.5}{(0.4 \times \pi \times (0.25^2 - 0.225^2))}$$

$$R = 100^o C/W$$

The general formula for conduction and convection heat transfer can be combined to solve for the temperature rise. The following calculations were based on a 2-W heat source with 5 mm (0.2 in) diameter which mimics a power pad S0-8 device. To solve for the heat rise, the use the axial symmetry of the situation and construct a ladder network of resistors driven by a current source of 2 W. The current source drives a series resistance determined by the lateral thermal resistance of the board which can be calculated as $R_{CON} = \ln(Ro/Ri)/(2 \times \pi \times 0.4 \times 0.07)$ Metric or $R_{CON} = \ln(Ro/Ri)/(2 \times \pi \times 9 \times 0.0028)$ English. The 2 in the equation assumes that there is a copper plane on top and bottom of the board, the expression neglects front-to-back thermal resistance. At the output of the resistor are two more resistors, one connected to ground (or really ambient temperature) and the second representing the thermal resistance of the next annulus. The resistance to ground is calculated from the heat transfer expression as $Rconv = 1000/(Ro^2 - Ri^2) \times \pi/2$ Metric or $Rconv = 166/(Ro^2 - Ri^2) \times \pi/2$ English. The circuit was then put in Excel and the temperature rise was calculated as shown in Fig. 23. A calculated temperature rise about 35ºC is shown and even on infinite board most of the heat is dissipated in the first inch from heat source. This is consistent with our calculated needs of seven square inches of dissipating area to control temperatures. This is also about the best one can do with PWB surface cooling with no air flow. The calculated thermal resistance is about 15ºC/W in this case. Practical experience tends toward a more conservative 20ºC/W to 30ºC/W.



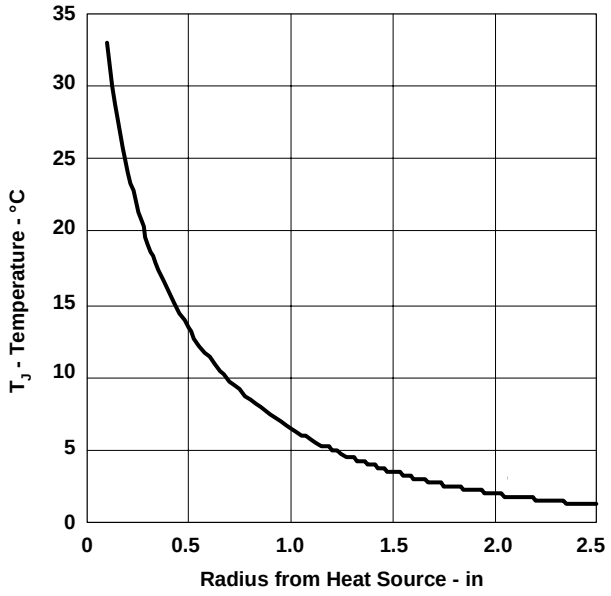


Fig. 23. 2 W of dissipation on double sided board calculates 30ºC rise.

One more thermal path that needs to be considered is across a break in a plane. Fig. 24 presents an approximation. It provides the thermal resistance of a 0.25-mm (0.01-in) break that is 2.54 cm (1 in) wide and the conclusion is that very little heat takes this path. One way around this issue is to use buried planes or a plane on the other side of the board to bridge this gap. The vertical heat flow can be good if there are large areas involved on both sides of the board.

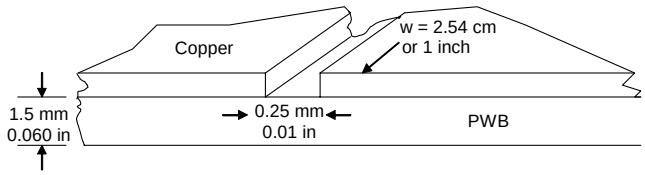


Fig. 24. Thermal resistance gap significantly adds to temperature rise.

$$R = \frac{l}{(\sigma wt)}$$

$$R = \frac{0.25}{(0.00018 \times 25.4 \times 1.5)} \text{ Metric}$$

$$R = \frac{0.01}{(0.007 \times 1 \times 0.06)} / \text{English}$$

$$R = 36^{o}C/W$$

There are more precise expressions for convection heat transfer. One of the more popular one recognizes that h is not constant but is a function of size and temperature rise as shown in the following. With a little manipulation, the equation can be resolved for temperature rise.

$$\Delta T = \frac{Pd}{(h \times A)}$$

$$h = K\left(\frac{\Delta T}{\sqrt{A}}\right)^{1/4}$$

$$\Delta T = \frac{Pd}{\left(K\left(\frac{\Delta T}{\sqrt{A}}\right)^{1/4} \times A\right)}$$

$$\Delta T^{1.25} = \frac{Pd}{(KA^{7/8})}$$

$$\Delta T = Pd^{0.8} \times \frac{K'}{A^{0.7}}$$

$$\Delta T = P^{0.8} Sa^{-0.7} \times 650^{o}C \ cm,W$$

$$\Delta T = P^{0.8} Sa^{-0.7} \times 100^{o}C \ in,W$$

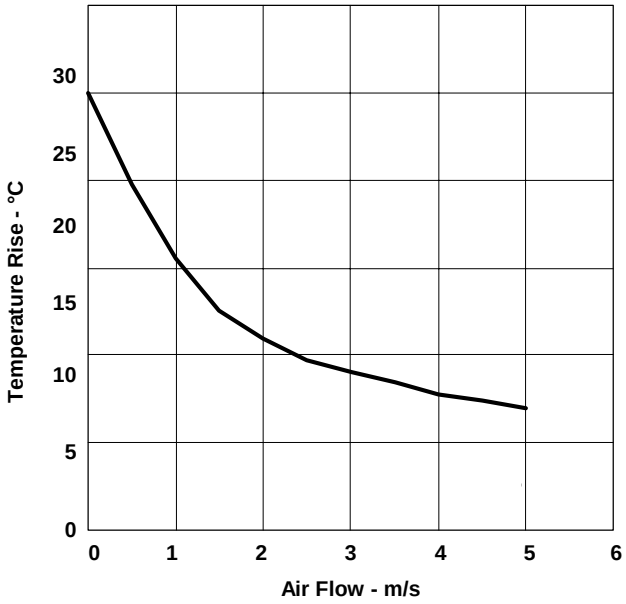
Finally, *h* is not constant with orientation. A vertical surface cools better than a horizontal surface, as shown in Table 6.

TABLE 6. VALUES OF K′ FOR VARIOUS ORIENTATION

Surface Orientation	K′ (In cm. ºC, and W)	K′ (In in. ºC, and W)
Vertical	650	100
Horizontal plane, top surface	675	104
Horizontal, bottom surface	1375	204

To summarize, to make use of the PWB as a cooling surface, a low-lateral thermal resistance is needed. It can be obtained with large, thick copper planes to distribute heat across PWB surface. It is best to minimize the thermal resistance with as much copper on each layer as practical. The thermal resistance from side to side of the PWB is low enough that it is practical to count on both sides of the board to cool. If further reduction of thermal resistance through the board is needed, substantial improvements can be made with thermal vias. Also, minimize breaks in planes as they substantially degrade lateral heat flow. Adjacent planes bridging the necessary breaks can also improve the lateral heat flow.

So far only natural convection has been discussed, but many systems incorporate fans to provide improved heat transfer. And the impact can be dramatic as shown in Fig. 25. Even a whisper of air can reduce temperatures. This curve was generated from heat sink data and shows that a 25ºC rise can be diminished to 5ºC with airflow. Airflow is measured in meters/second (or linear feet per minute) over the surface. For reference for those using our confusing English dimensions, 1 mile per hour is 88 feet per minute. Typical system airflows in the 0.5 ms to 2 ms (100 to 400 feet per minute) can provide a 2-to-1 temperature reduction at the pace of a leisurely walk!



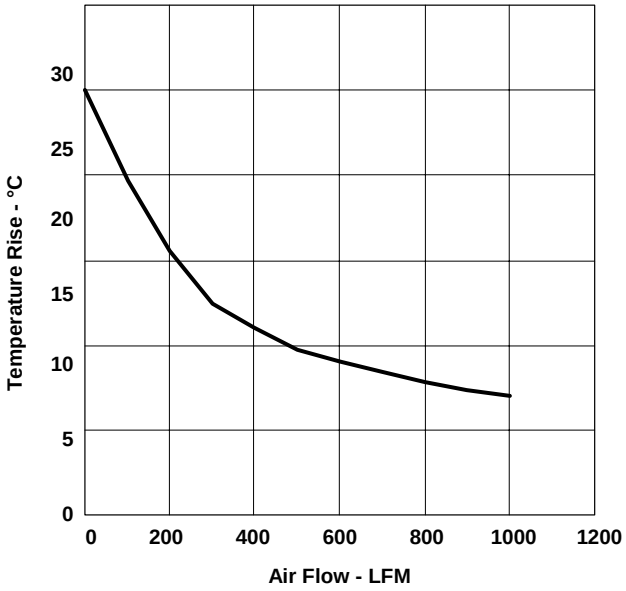


Fig. 25. Even a whisper of airflow can dramatically lower temperature rise.

Radiation may also take some heat out the board, but for this to occur, the board must "see" a lower ambient temperature. An interior PWB with adjacent boards of similar temperatures is unable to dissipate heat by radiation. The heat radiated can be calculated with the following general formula. This calculates the radiation heat transfer between two surfaces of temperature T1 and T2. Note that these are absolute temperatures so that room temperature is 273 + 25 = 298ºK. The first constant contains emissivity and a unit's correction factor. "*A*" represents the surface from which the heat is transferred; *Fz* is an emissivity factor which is the ratio of the materials ability to radiate heat compared to a black body. (Note that one can not visually inspect a surface to determine if it is a black body as most of the heat will be radiated at infrared frequencies). And *Fa* is a configuration factor, or form factor, that relates to how the two surfaces see each other.

$$q = \sigma \times A \times F_{\varepsilon} \times F_{a} \times (T_1^4 - T_2^4)$$

- σ = constant
- A = area
- F_Z = emissivity factor
- F_A = configuration factor
- T = temperature degress kelvin

This equation was then set up for a unit area, 0.6 emissivity radiator in a very large room at 70ºC. The temperature of the radiator was varied and the heat transfer was calculated as shown in Fig. 26. The heat transfer is almost linear with temperature. This can be explained by expanding the expression $(1+x)^4$ and making the assumption that x is small compared to 1. All the higher order terms drop out and the expression is linear in x or temperature rise or:

$$(1+x)^4 = 1 + 4x + 6x^2 + 4x^3 + x^4$$

$$x << 1$$

$$(1+x)^4 \approx 1 + 4x$$

This allows the calculation of an equivalent thermal resistance per unit area of 55ºC/0.04 = 1400ºC/W/cm^2 (or 55ºC/0.25 W = 220ºC/W/in^2) which is approximately twice natural convection cooling or simply put, radiation cooling at typical board temperatures is about ½ as effective as natural convection. Rather than complicating the convection calculations by adding this in, most designers choose to use this as a safety factor.

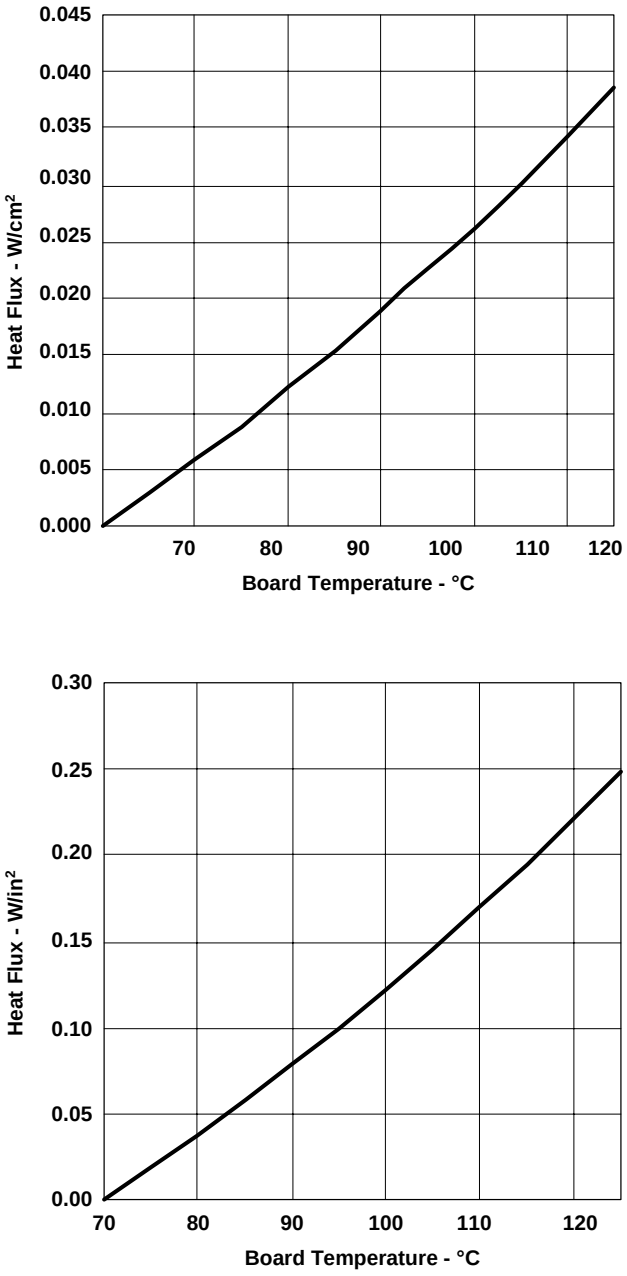


Fig. 26. Radiation heat transfer provides safety factor over convection calculations.

VI. Design Examples

The following figures provide some real world examples of what to do and not to do when laying out your power supply. Fig. 27 presents a good EMI filter layout. The points to be noted are; the integrity of the common inductor is maintained by not having board capacitance short it out, in other words, T2 inputs pins do not cross outputs pins. Also there is no ground plane under EMI filter to short across the common mode inductor. Also, wide, short trace are used to minimize losses and wide spacing between traceses meets high voltage requirements and minimize coupling capacitance.

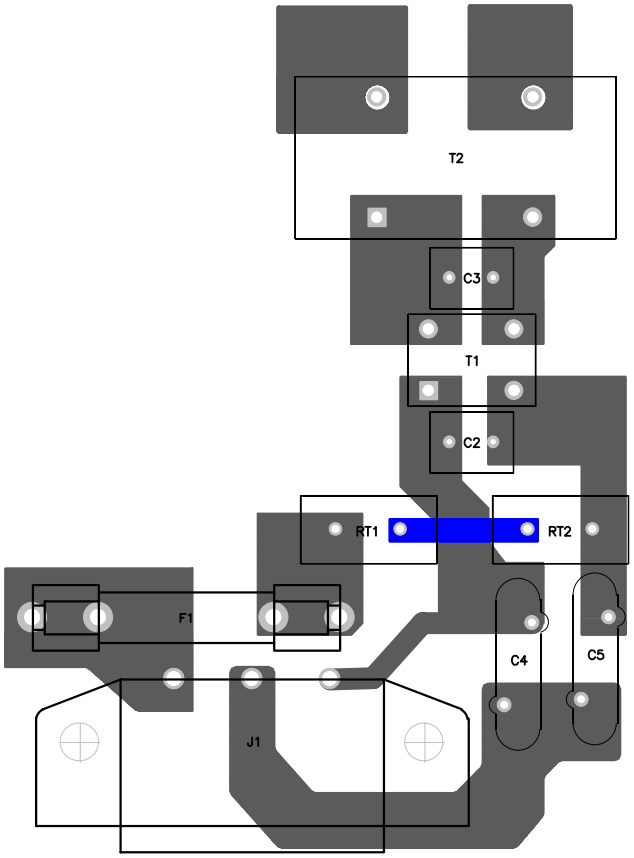


Fig. 27. Example EMI filter layout.

Fig. 28 and Fig.29 shows both a right way and a wrong way to connect output capacitors. The right way minimizes the series inductance of the output filter capacitors. Current is routed directly under the high frequency capacitor, C39. Lead lengths connecting the capacitors are minimized to reduce series inductance. Although not apparent on these pictures, numerous vias were dropped into the ground plane on the bottom of the board.

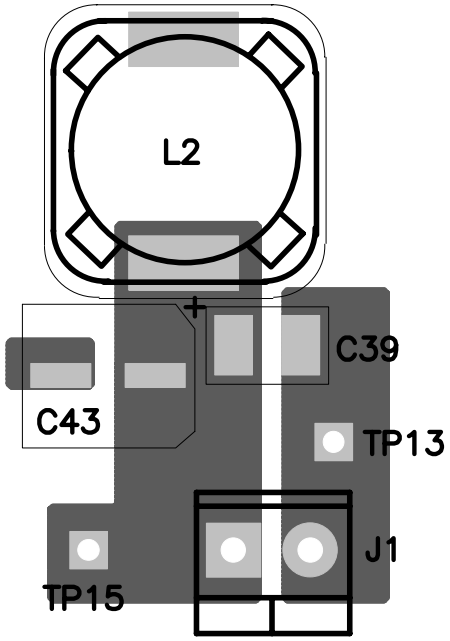


Fig. 28. Proper output filter routing reduces high frequency ripple (low series inductance).

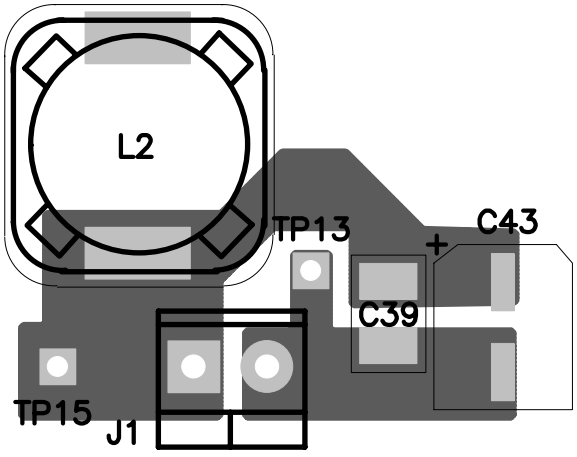


Fig. 29. Proper output filter routing reduces high frequency ripple (low series inductance).

Fig. 30 and Fig. 31 shows the right and wrong way to connect the output voltage sense point. In the right way, shown on the left, the sense point is connected as close to the load as possible. The wrong way just connects to the most convenient point. With current flow between this connection and the load, there is voltage drop in the PWB which degrades regulation. A careful designer will review this connection closely as most layout people go for convenience every time.

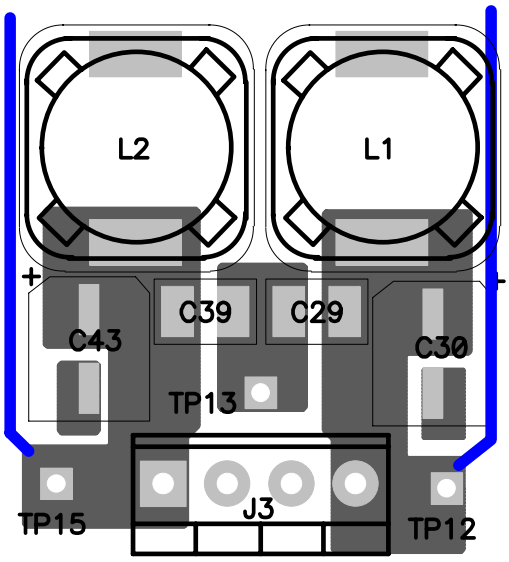


Fig. 30. Proper sensing improves load regulation.

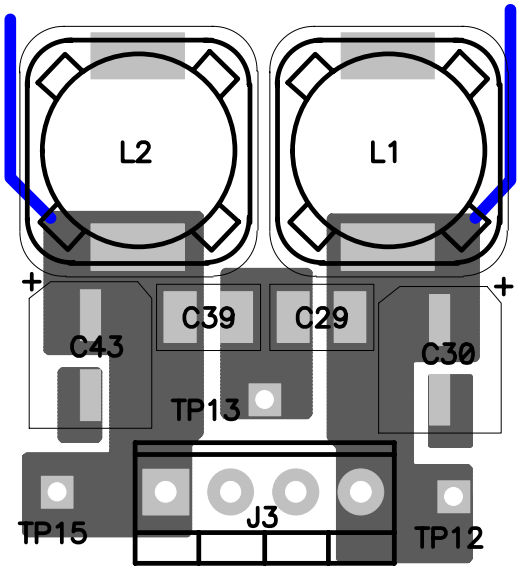


Fig. 31. Proper sensing improves load regulation.

Fig. 32 shows a good layout for the error amplifier and low level components on the left side of the controller. It has very short trace runs to minimize parasitic capacitance and switching noise pick-up. Very close attention is paid to the error amplifier connections (pins 7, and 8) which are extremely noise sensitive and were routed carefully. This is a multilayer board and the second layer is ground plane to minimize pick-up and inductance. The design drops returns into the ground plane without long traces. Feedback from the output voltage is routed well away from switching power signals.

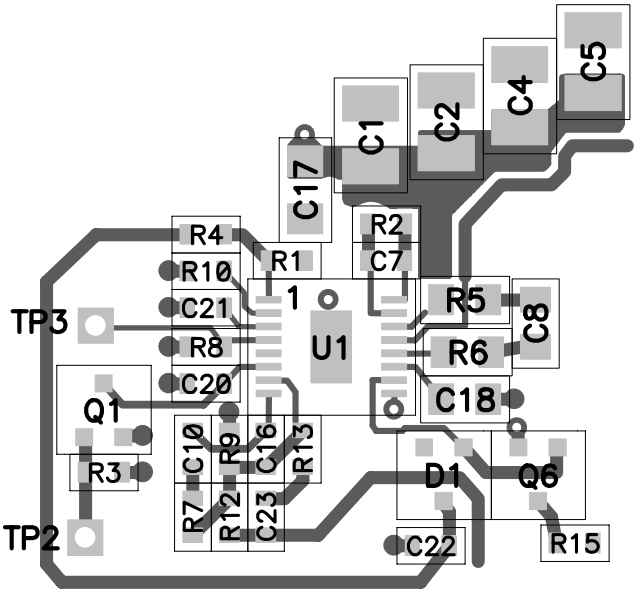


Fig. 32. Proper layout control minimizes checkout issues.

Fig. 33 is an example of good input bypass capacitor layout. C2 and C100 input caps, ground side drops into the ground plane through multiple vias. Also, the bottom FET (Q6) ground drops into the ground plane through multiple vias. And on the bottom layer, there is a solid uninterrupted ground plane. Also, note that the ground connections for these two power parts are made in close proximity to minimize high AC current in the ground plane.

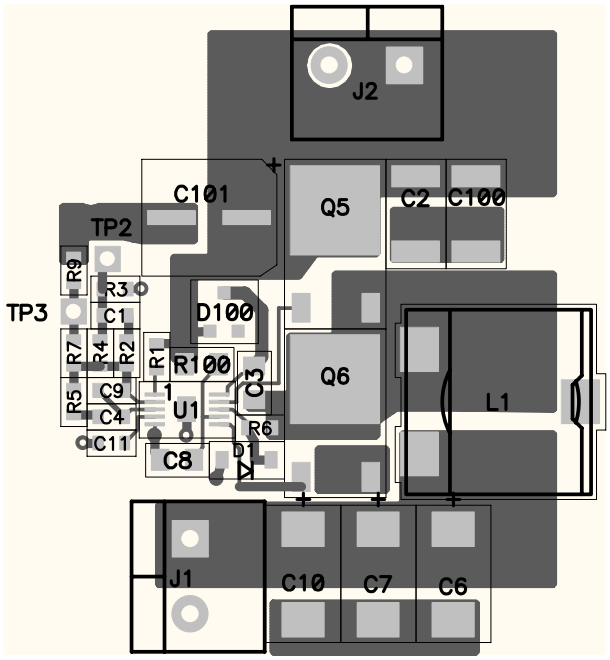


Fig. 33. Proper input capacitor placement provides short path for AC current.

Fig. 34 presents a high dissipation example. Here, a large surface was used to dissipate the heat from the power components. Spreading the heat required the designer to maximize copper in the available space. This was a multilayer board and this copper pattern was duplicated on several layers. There were very few breaks in the copper leading to good lateral spreading. Thermal vias were located near and under heat sources to help spread the heat to the back of the board and internal layers.

Fig. 34. Massive copper pours help spread heat.

Fig. 35 presents a successful job of cooling a power supply through the PWB surface. FETs with about 1 W of dissipation were cooled to a 50 degree rise by using the methods presented in this article. Copper planes helped to stabilize temperatures across the board surface and a large number of vias provided a good front to back thermal path. Power components and their dissipations were spread out over the board surface to help equalize the heat flow from the board surface to the ambient FETs closest to the edge of the board were the hottest as they had the least available board area for cooling.

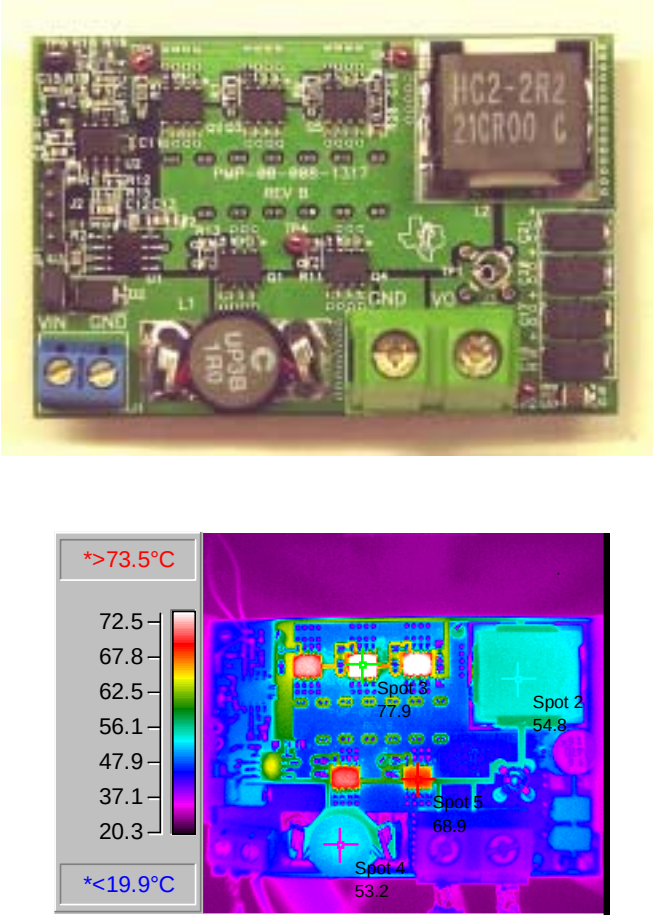


Fig. 35. Attention to details yields a well cooled design.

VII. Summary

Power supply layout is as important as any other design consideration. The power supply engineer must be involved in the parts placement and routing. An understanding of AC and DC parasitics, grounding, and cooling makes a successful design.

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APPENDIX A.
THERMAL CONDUCTIVITY OF OTHER MATERIALS

Material	W/(cm ºC)	W/(in ºC)
Air	0.0002	0.0007
Alumina	0.2	0.9
Aluminum	1.8	4.4
Beryllia	1.6	4
Copper (OFC)	3.6	9
Epoxy (PC board)	0.003	0.007
Ferrite	0.04	0.10
Steel	0.15	0.60
Tin-lead	0.4	1.00

APPENDIX B.
SAMPLE EMISSITIVITIES

Material	Emissitivity (e)
Bare aluminum	0.08
Polished copper/tin	0.04
Glass	0.9
Anodized aluminum	0.8
Lacquer	0.8
Water	0.95
White alumina	0.88
Machined copper	0.7
Dull nichel plate	0.11

Topic 5

Interleaving Contributes Unique Benefits to Forward and Flyback Converters

Texas Instruments

Interleaving Contributes Unique Benefits to Forward and Flyback Converters

Brian Shaffer

ABSTRACT

A 200-W interleaved forward converter design example illustrates how an interleaved topology can reduce the size and cost of power filtering components and also enhance dynamic load response. In this comprehensive design review, the converter operates from a standard 48-V telecom input voltage and outputs 12 V at 200 W in a half-brick footprint. Operating at a switching frequency of 500 kHz per phase, over 90% efficiency is achieved without the use of synchronous rectifiers. The two-inductor interleaved forward converter is compared against a one inductor interleaved forward converter, a push-pull converter, and a half-bridge converter. A 200-W interleaved flyback converter with an isolated regulated output voltage is also presented. This flyback topology has the potential for operation over the universal AC line voltage range, with the added benefit of achieving a high power-factor input characteristic without additional PFC circuitry.

I. INTRODUCTION

In recent years the usefulness of interleaving power stages has become apparent. The best known application is in powering microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications, the converters are non-isolated from input to output. This paper presents the benefits of interleaving power stages for isolated applications. It shows that the two-inductor (2L) interleaved forward converter topology or the interleaved flyback converter topologies are appropriate choices for many high-power applications.

The forward converter shown in Fig. 1 is one of the most studied topologies. Derived from the simple buck converter, the forward converter delivers energy from the input source to the output filter inductor during the on time of the main switch. In contrast, the flyback converter shown in Fig. 3 delivers energy to the output filter capacitor only during the off-time of the main power switch. This different power transfer characteristic has a dramatic impact on the transfer function and the power levels at which a flyback converter is applicable.

The concept of interleaving enables these converter topologies to operate at increased power levels. The benefits of interleaving include:

- Reduced RMS current in the input capacitors enabling the use of less expensive and fewer input capacitors
- Ripple current cancellation in the output capacitor, enabling the use of less expensive and fewer output capacitors
- Reduction of peak currents in primary and secondary transformer windings (2L interleaved forward converter)
- Improved transient response as a result of reduced output filter inductance and higher output ripple frequency
- Separation of heat generating components allowing for reduced heatsink requirements.
- Improved form factor for low profile solutions
- Reduced EMI as a result of reduced peak currents (2L interleaved forward converter)

II. SINGLE FORWARD CONVERTER

For the single forward converter shown in Fig. 1 the following quantities are evaluated and compared to "1L" or "2L" interleaved forward converters, push-pull converters, and half-bridge converters.

Comparison Quantities:

- Transformer peak currents
- Transformer RMS currents
- Minimum transformer turns ratio
- Input capacitor AC RMS current
- Output inductor peak-to-peak ripple current
- Output capacitor AC RMS current
- Power switch peak voltage
- Output rectifier peak voltage
- Output rectifier peak current.

Table 1 summarizes the equations for the above quantities. In Table 6 these equations are evaluated for a 200 W design example and compared to the results from the other topologies listed above. In Table 7, 500 W design examples are compared.

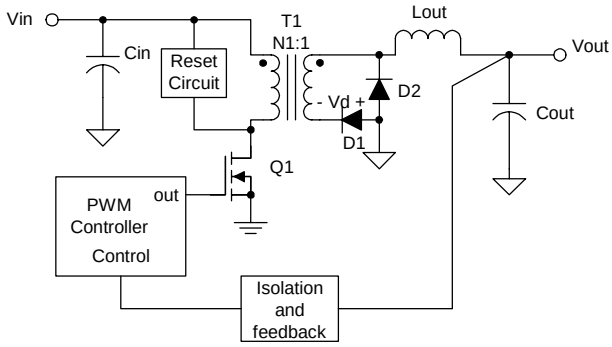

Fig. 1. Single forward converter power stage.

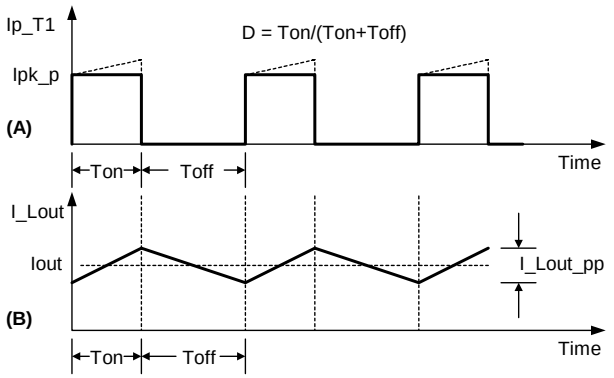

Fig. 2. Forward converter waveforms, (A) Primary transformer current, (B) output inductor current (D = 0.4).

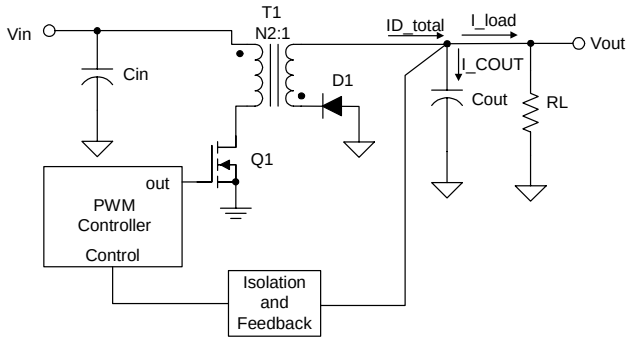

Fig. 3. Single flyback converter.

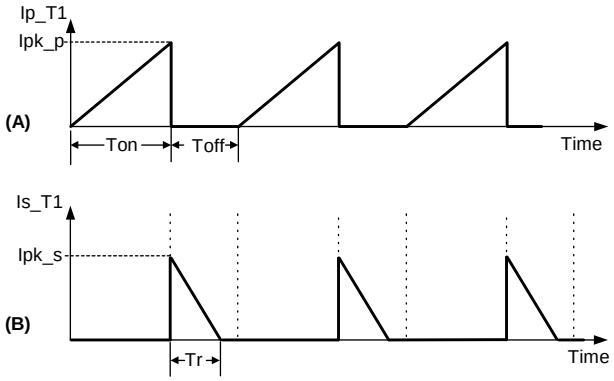

Fig. 4. Flyback converter waveforms, (A) Primary transformer current, (B) secondary transformer current (D = 0.6).

TABLE 1. SINGLE-FORWARD CONVERTER EQUATIONS

Parameter	Single Forward
Ipk_s_T1	Iout
Ipk_p_T1	$\frac{Iout}{N1}$
Irms_s_T1	$Iout * \sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{N1} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N1} * \sqrt{D * (1 - D)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1 - D\max}$ or $\frac{Vin\_\max}{1 - D\min}$
Vpk_D1	$Vin\_\min * \frac{D\_\max}{1 - D\_\max} * \frac{1}{N1}$
Vpk_D2	$\frac{Vin\_\max}{N1}$
Ipk_D1	Iout

III. INTERLEAVED FORWARD CONVERTERS

Fig. 5 contains a representation of two power stages in an interleaved configuration where two output inductors (2L) are used which allows the duty cycle of each power stage to go above fifty percent. This is beneficial in many reset techniques presently being used today such as, resonant reset, RCD clamps, or active reset techniques. By allowing the duty cycle of the converter to be centered around 50%, it is possible to minimize the AC RMS ripple currents in the input and output capacitors at the expense of higher peak voltages on the power switches. This leads to a fewer number of and less expensive input and output capacitors. In general, semiconductor devices are more reliable and cost effective than capacitors, so the increased voltage stress on the power switches and output rectifiers is considered desirable when compared to having more expense and a lager number of input and output capacitors. Fig. 7 depicts an alternative configuration for interleaved forward converters where only one output inductor (1L) is required. It is shown that the 1L topology has higher peak and RMS transformer currents than the 2L topology.

In Fig. 5 the term "phase" is defined as any one of the individual power stages in the interleaved configuration. Fig. 6 contains the operating waveforms for the 2L interleaved forward converter of Fig. 5 operating at a duty cycle of 0.4. By examining Fig. 6 it becomes clear how to write the expressions for the input and output capacitor ripple currents when the duty cycle of each phase is less than or equal to 0.5 or one divided by x (1/x) where x is the number of phases being interleaved. The effect of interleaving on the duty cycle is to increase the effective duty cycle by the number of phases in the circuit and reduce the peak current by the same factor. In Fig. 5 there are two phases so the effective duty cycle is increased by a factor of two and the peak currents are reduced by the same amount. Another way of describing this phenomenon is to realize that the frequency of the input and output currents are increased by a factor of two over the switching frequency of each individual phase and the power throughput of each phase is inversely proportional to the number of phases.

For the interleaved forward converters shown in Figs. 5 and 7 the same quantities that were evaluated for the single forward converter are again evaluated and used to compare these interleaved converters against each other and to push-pull converters, or half-bridge converters.

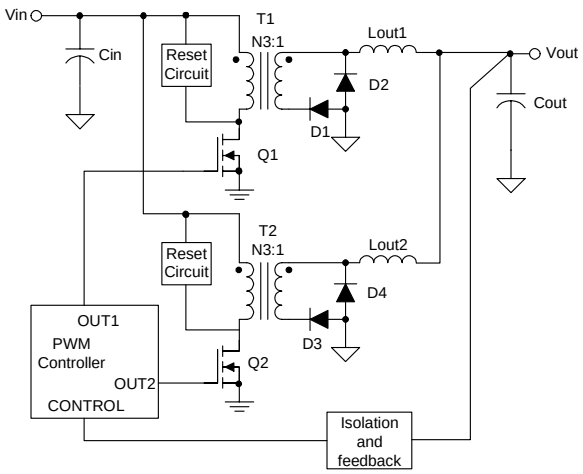

Fig. 5. "2L" interleaved forward converter (Dmax ≥ 0.5).

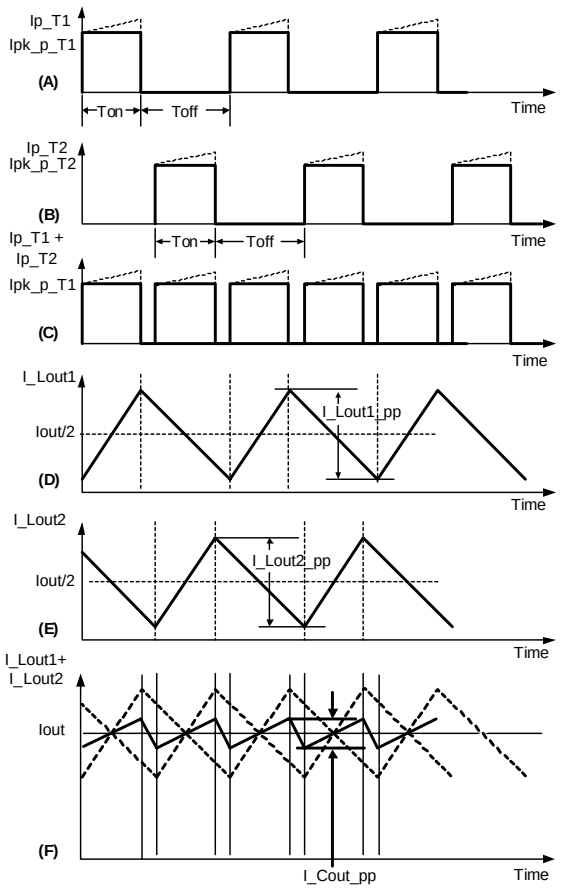

Fig. 6. 2L interleaved forward waveforms, D = 0.4 (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.

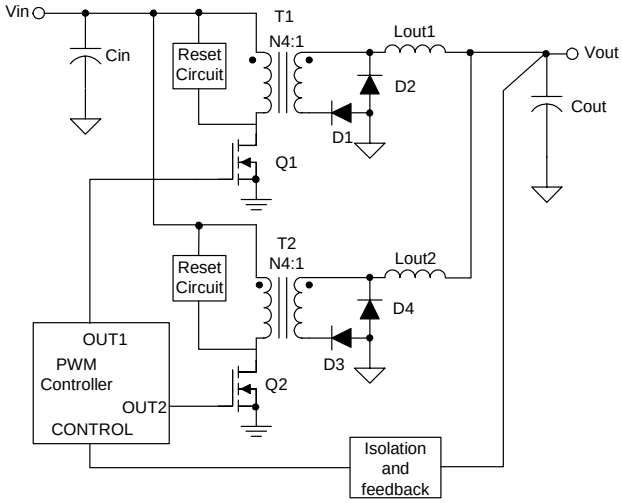

Fig. 7. "1L" interleaved forward converter (Dmax < 0.5).

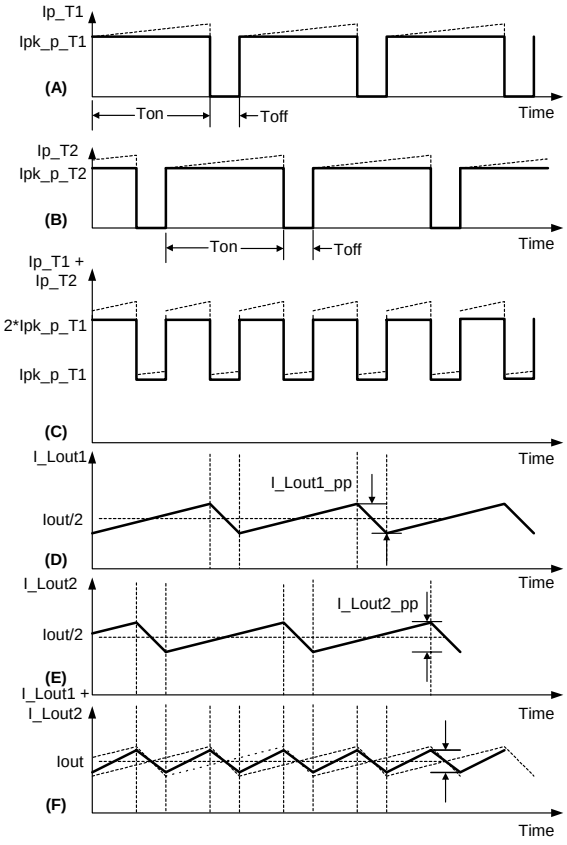

Fig. 8. 2L interleaved forward waveforms, D = 0.8, (A) Primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms (A) and (B) seen at the input capacitor, (D) output inductor current of phase 1, (E) output inductor current of phase 2, (F) sum of output inductor currents.

Interleaved Forward Converter with Two Output Inductors (2L)

Primary and Secondary Transformer Windings Peak Currents (D ≤ 0.5)

In Fig. 5, the peak secondary current, Ipk_s_T1, is cut in half for two phases.

$$Ipk\_s\_T1 = \frac{Iout}{2}$$

The peak current in the primary winding is then calculated by transforming the secondary current to the primary winding, by dividing it by the turns ratio of the transformer.

$$Ipk\_p\_T1 = \frac{Ipk\_s\_T1}{N3} = \frac{Iout}{2*N3}$$

Transformer RMS Currents (D ≤ 0.5)

The equivalent RMS current of the waveform in Fig. 6A, Irms_p_T1, equals:

$$Irms\_p\_T1 = Ipk\_p\_T1 * \sqrt{D}$$
$$= \frac{Iout}{2*N3} * \sqrt{D}$$

The secondary winding RMS current is then,

$$Irms\_s\_T1 = \frac{Iout}{2} * \sqrt{D}$$

Minimum Transformer Turns Ratio

The equation for calculating the turns ratio for the 2L interleaved forward converter is no different than that for the single forward converter. In the following equation and throughout this paper the quantity Dmax represents the maximum duty cycle of each phase. In the cases where the effective duty cycle is a multiple of the number of phases, a multiplier is added to the equation.

$$N3\_\min = \frac{Vin\_\min * D\max}{Vout + Vd}$$

Input Capacitor AC RMS Current (D ≤ 0.5)

The AC RMS current in the input capacitors is calculated for two different operating conditions. The initial analysis that follows presents the equations for the case where the maximum duty cycle of each phase is less than 0.5 and then, the case where the duty cycle is greater than 0.5 is presented in a later section. For the following calculations refer to Fig. 6C, which is the summation of the input current waveforms in the primary of transformers T1 and T2. In general, the AC RMS current in the input capacitor as a result of the transformer's input current waveform is:

$$Iacrms = \sqrt{Irms^2 - Idc^2}$$

where Irms = The RMS equivalent of the transformer current – [A]

Idc = The DC equivalent of the transformer current – [A]

hence,

$$Icin\_acrms$$
$$= Ipk\_p\_T1 * \sqrt{2*D*(1-2*D)}$$

$$Icin\_acrms$$
$$= \frac{Iout}{2*N3} * \sqrt{2*D*(1-2*D)}$$

Output Inductor Peak-to-Peak Ripple Current (D ≤ 0.5)

The output inductor ripple current for each of the phases is calculated in the same manner as with a single forward converter. By factoring in the off time and the output voltage the peak-to-peak ripple current for each output inductor is given by:

$$I\_Lout\_pp = \frac{(Vout + Vd) * (1 - D)}{Lout * Fs}$$

where, Lout = Lout1 = Lout2

Fs = The switching frequency of each phase in Hertz

Output Capacitor AC RMS Current (D ≤ 0.5)

The following discussion refers to Fig. 6F, which is the sum of the individual output inductor ripple currents shown in Figs 6D and 6E. Assuming that each of the phases is 360/x degrees offset from one another with equal duty cycles the effective duty cycle of the summed inductor current waveform is x times the individual duty cycle of each phase. The output capacitors are exposed to this summed current waveform and the resultant AC RMS current is the portion of the waveform that causes heating in the output capacitors. The peak-to-peak ripple current of the summed inductor current waveform is expressed by the following equation.

$$ILout\_total\_pp = \frac{(Vout + Vd) * (1 - 2 * D)}{Lout * Fs}$$

The AC ripple current in the output capacitors for the 2L interleaved forward topology, Icout_acrms, is then:

$$Icout\_acrms = \frac{ILout\_total\_pp}{2} * \sqrt{\frac{1}{3}}$$

Output Capacitor RMS Ripple Current Cancellation (D ≤ 0.5)

Taking the ratio of the output capacitor AC RMS current in the 2L interleaved case and the AC RMS current of the single forward converter reveals an important reason why interleaving is beneficial. For all values of D less than 0.5, the following equation is less than one which means that the peak-to-peak ripple current seen by the output capacitors is less than the non-interleaved case. The same is true for the cases where D > 0.5.

$$\frac{Icout\_acrms\_2L}{Icout\_acrms\_FWD} = \frac{1 - 2 * D}{1 - D}$$

Power Switch Peak Voltage

The peak voltage on the power switch is a result from the requirement that the volt second product on the primary transformer winding average to zero. The longer the on-time the more negative the reset voltage must be in order to maintain a volt second balance. Assuming that the reset voltage is a square wave and that the reset voltage is present throughout the entire off time of the main switch, the volt second balance equation is expressed as:

$$Vin * D - Vreset * (1 - D) = 0$$

$$Vreset = \frac{Vin * D}{1 - D}$$

From Fig. 5, the peak voltage on the power switch, Vpk_Q1 is equal to the sum of the input voltage and the reset voltage.

$$Vpk\_Q1 = Vin + \frac{Vin * D}{1 - D} = \frac{Vin}{1 - D}$$

Fig. 9, Vpk_Q1/Vin, depicts the penalty that is paid as the duty cycle is increased. When the duty cycle has reached 0.5 the peak voltage on the switch is equal to twice the input voltage.

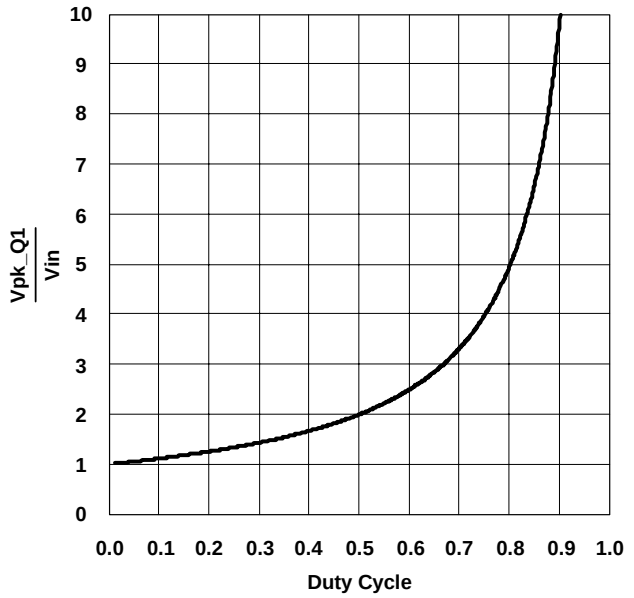

Fig. 9. Normalized peak voltage on the main switch vs. duty cycle.

Fig. 9 which shows the normalized peak voltage on the main switch applies to interleaved converters as well as non-interleaved converters. In Fig. 5 where the duty cycle is allowed to go above 0.5, it is expected that the peak voltage on the main switch is greater than that seen by the main switch for the complementary design using Fig. 7. For example, consider the case where the maximum duty cycle for the 2L design is allowed to go to 0.8 and the corresponding maximum duty cycle for the 1L design is limited to 0.4, then the peak voltage on the switch in the 2L design is 2.86 (5/1.75) times greater than that for the 1L design. The drawback in peak voltage stress for designs using the 2L configuration is immediately obvious, but the reduction in the input and output capacitor AC RMS currents outweighs this disadvantage.

Output Rectifier Peak Voltage and Current

The peak voltage on the output rectifiers in the 2L interleaved case is given by,

$$Vpk\_D1 = \frac{Vin * D}{1 - D} * \frac{1}{N3}$$

The peak current in the output rectifiers for the 2L interleaved forward configuration is equal to one half of the load current because the output current is made up of the sum of the individual phase currents.

Transformer RMS Currents (D > 0.5)

In the 2L interleaved flyback converter, the equations for determining the RMS current in the transformer windings when the duty cycle is greater than 0.5 are the same as the case where the maximum duty cycle is less than 0.5. The RMS current in the transformer windings increases proportionally to the square root of the increase in duty cycle. For example, a doubling in the maximum duty cycle only increases the RMS current in the winding by forty-one percent. This increase is offset by the reduction in AC RMS current in the input and output capacitors. Because the failure rate of capacitors due to overheating is much more of a concern than heat in a magnetic component, the tradeoff of increased RMS current in the transformer for a reduction in AC RMS currents in the input and output capacitors is worthwhile.

Input Capacitor RMS Current (D > 0.5)

As was stated earlier, the circuit configuration of Fig. 5 is allowed to go above 50% duty cycle. In such an operating mode, the equations for determining the input and output ripple currents change slightly. Referring to Fig. 8, the total RMS equivalent current of the waveform in Fig. 8(C), Iin_rms, equals:

$$Iin\_rms = Ipk\_p\_T1 * \sqrt{2 * (D - 0.5)} + Ipk\_p\_T1$$

The DC equivalent current of the current waveform in Fig. 8(C), Iin_dc, equals:

$$Iin\_dc = Ipk\_p\_T1 * (2 * (D - 0.5)) + Ipk\_p\_T1$$

The AC RMS current in the input capacitor as a result of the transformer's input current waveform is then:

$$Icin\_acrms = Ipk\_p\_T1 * \sqrt{4 * (D - 0.5) * (1 - D)}$$

Substituting Ipk_p_T1 from above yields:

$$Icin\_acrms = \frac{Iout}{2 * N3} * \sqrt{4 * (D - 0.5) * (1 - D)}$$

Fig. 10 depicts the normalized AC RMS input current for the circuit shown in Fig. 5 for duty cycles from zero to one. The normalization factor defines the AC RMS current in the input capacitors as a function of the peak current in the primary windings, Iout/(2xN3).

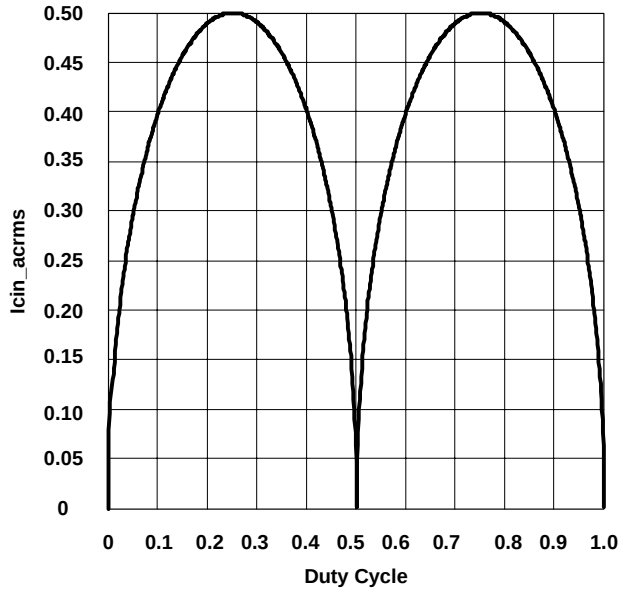

Fig. 10. Normalized AC RMS ripple current seen by the input capacitor vs. duty cycle.

Output Inductor Ripple Current (D > 0.5)

The equation for determining the individual phase ripple current is not changed from the case where the maximum duty cycle is limited to 0.5. It is still directly proportional to the output voltage and off time and inversely proportional to the value of the output inductor.

Output Capacitor RMS Ripple Current (D > 0.5)

In order to develop the expression for the output capacitor ripple current it must first be understand how the output inductor ripple currents sum for this case where the duty cycle is allowed to be greater than 0.5. The summation of the individual output inductor phase currents, which is the total peak-to-peak ripple current in the output capacitor as a function of duty cycle is given by the following equation [9]:

$$ILout\_total\_pp = (I\_Lout\_pp) * (KI)$$

$$I\_Lout\_pp = \frac{(Vout + Vd) * (1 - D)}{Lout * Fs}$$

$$KI = \frac{x * \left(D - \frac{m}{x}\right) * \left(\frac{m+1}{x} - D\right)}{D * (1 - D)}$$

where x = number of phases (2 for our example)

m = floor(x*D) is the maximum integer that does not exceed the product of x and D.

I_Lout_pp = peak-to-peak inductor ripple current in each phase. [A]

KI = cancellation effect of interleaving on the individual peak-to-peak inductor ripple current.

Normalizing the equation for ILout_total_pp to the amount of ripple current per phase gives the cancellation effect, KI that is present as a result of interleaving power stages at various operating duty cycles.

For x = 2,

$$KI = \begin{cases} \dfrac{(1-2D)}{1-D} \; if \; D \le 0.5 \\ \dfrac{(2D-1)}{D} \; if \; D > 0.5 \end{cases}$$

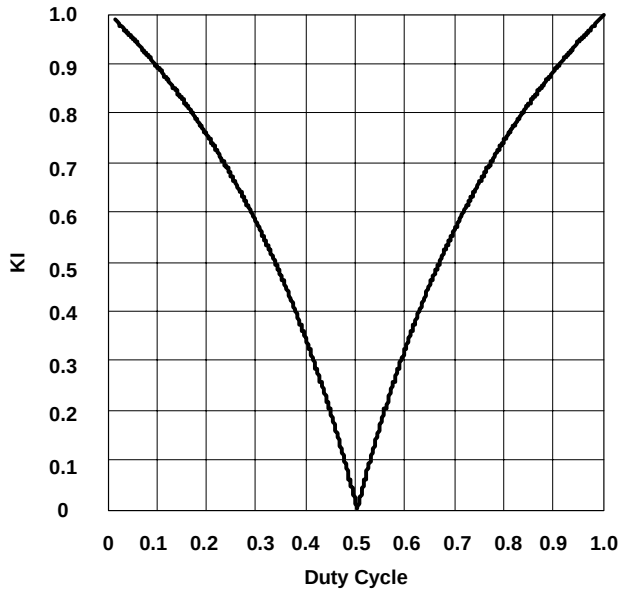

Fig. 11. Cancellation effect on output capacitor ripple current normalized to the ripple current of a single phase vs. duty cycle.

By examining the preceding graphs for the entire range of possible duty cycles, it becomes clear that the optimal operating point for each phase is at a duty cycle equal to one divided by the number of phases with a phase relation of 360 degrees divided by x (360/x). The optimal operating point is not always achievable given a wide input range and semiconductor limitations, but the closer the circuit operates near the optimal point the lower the RMS currents in the input and output capacitors will be. At any operating point, Fig. 11 is used to determine the actual amount of peak-to-peak ripple current in the output capacitors given the peak-to-peak ripple current of each individual phase and the operating duty cycle. Because the current waveform after the summation of the individual ripple currents is still a triangle wave, the AC RMS component which flows through the output capacitor is calculated as follows:

$$Icout\_acrms = \frac{ILout\_total\_pp}{2} * \sqrt{\frac{1}{3}}$$

Power Switch Peak Voltage (D > 0.5)

The equation for determining the peak voltage on the power switches is the same as for the single case and the condition where the duty cycle is less than 0.5.

Output Rectifier Peak Voltage (D > 0.5)

The equation for determining the peak voltage on the output rectifiers is the same as for the single case.

Output Rectifiers Peak Current (D > 0.5)

The peak current in the output rectifiers does not change as a function of duty cycle. It is still equal to half of the load current.

Appendix B contains the empirical circuit waveforms for a 200-W 2L interleaved forward converter design. Figs B7, B8, and B9 demonstrate the ripple current cancellation effect with two interleaved power stages. Figs. B10 and B11 show the improvement in the output transient response which is achievable by interleaving power stages.

A. Interleaved Forward Converter with One Output Inductor (1L)

The circuit configuration in Fig. 7 does not allow for an operating duty cycle greater than 0.5. As a result D4 and Lout2 are removable from Fig. 5 provided that the secondary of T2 is connected to the input side of the remaining output inductor. If the duty cycle were to go above 0.5 in Fig. 7, the forward diodes D1 and D3 would create a short across the secondary of the transformers. With the removal of D4 and Lout2 the resultant peak secondary transformer current is now equal to the full load current. The current waveforms for the 1L configuration are depicted in Fig. 12. Table 3 summarizes the equations that are used in Table 6 to compare the 1L interleaved forward converter to the other topologies listed in this paper.

TABLE 2. "2L" INTERLEAVED FORWARD CONVERTER EQUATIONS

Parameter	Interleaved Forward (2L)
Ipk_s_T1	$\frac{Iout}{2}$
Ipk_p_T1	$\frac{Iout}{2*N3}$
Irms_s_T1	$\frac{Iout}{2}*\sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{2*N3}*\sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * D\max}{Vout+Vd}$
Icin_acrms	$D \le 0.5$; $\frac{Iout}{2*N3}*\sqrt{2*D*(1-2*D)}$ $D>0.5$; $\frac{Iout}{2*N3}*\sqrt{4*(D-0.5)*(1-D)}$
I_Lout_pp	$\frac{(Vout+Vd)*(1-D\max)}{Lout*Fs}$
ILout_total-pp	$\frac{(Vout+Vd)*(1-D)}{Lout*Fs} * \frac{2*\left(D-\frac{m}{2}\right)*\left(\frac{m+1}{2}-D\right)}{D*(1-D)}$ *where* $m = floor\,(2*D)$
Icout_acrms	$\frac{ILout\_total\_pp}{2}*\sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1-D\max}$ or $\frac{Vin\_\max}{1-D\min}$
Vpk_D1	$Vin\_\min * \frac{D\_\max}{1-D\_\max} * \frac{1}{N3}$
Vpk_D2	$\frac{Vin\_\max}{N3}$
Ipk_D1	$\frac{Iout}{2}$

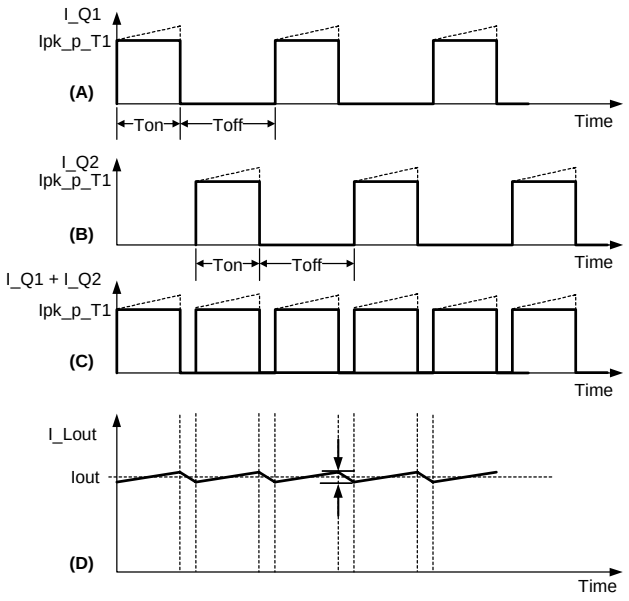

Fig. 12. 1L interleaved forward converter waveforms (A) primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms "a" and "b" seen at the input capacitor, (D) output inductor current (D = 0.4).

Comparison of 2L and 1L Transformer RMS Currents

One major benefit of using two output inductors as opposed to one output inductor is that the resulting RMS currents in the transformers are significantly reduced. Consider the following comparison:

2L primary input RMS current:

$$Irms\_p\_T1\_2L = \frac{Iout}{2*N3}*\sqrt{D\max\_2L}$$

1L primary input RMS current:

$$Irms\_p\_T1\_1L = \frac{Iout}{N4}*\sqrt{D\max\_1L}$$

Ratio of 2L RMS transformer current to 1L RMS transformer current:

$$\frac{Irms\_p\_T1\_2L}{Irms\_p\_T1\_1L} = \frac{1}{2}*\frac{N4}{N3}\sqrt{\frac{D\max\_2L}{D\max\_1L}}$$

As a specific example, consider the case where the load current is equal in both circuits and the duty cycle for the 2L power stages is 0.8 with the duty cycle for the 1L power stages equal to 0.4. In this example the turns ratio, Nx_min, for each of the transformers is equal, then:

$$\frac{Irms\_p\_T1\_2L}{Irms\_p\_T1\_1L} = \frac{1}{\sqrt{2}}$$

By configuring the circuit with two output inductors it allows operating duty cycles of greater than 50%, reducing the RMS currents in the transformer by a factor of the square root of two, and reduces the conducted EMI produced because the peak currents are reduced.

TABLE 3. "1L" INTERLEAVED FORWARD CONVERTER EQUATIONS

Parameter	Interleaved Forward (1L)
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N4}$
Irms_s_T1	$Iout * \sqrt{D\max}$
Irms_p_T1	$\frac{Iout}{N4} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N4} * \sqrt{2 * D * (1 - 2 * D)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - 2 * D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$\frac{Vin\_\min}{1 - D\max}$ or $\frac{Vin\_\max}{1 - D\min}$
Vpk_D1	$\frac{Vin}{N4} * \frac{1}{1 - D\_\max}$
Ipk_D1	$Iout$

Summary of 2L vs. 1L Interleaved Forward Converters

Advantages of 2L interleaved forward topology vs. 1L interleaved forward topology:

- Reduced transformer peak currents
- Reduced RMS transformer currents by $\sqrt{2}$
- Reduced transformer heating by a factor of 2
- Reduced input capacitor RMS currents
- Reduced output capacitor RMS currents
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward topology vs. 1L interleaved forward topology:

- Increased component count
- Possible increase in area of components
- Increased peak voltage stress on primary switch when duty cycle is greater than 0.5
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

B. Push-Pull Circuit Topology

Fig. 13 shows a push-pull converter. In general, a push-pull converter would be considered for the same applications as the interleaved forward converter. The same quantities as defined above are presented here for the push-pull topology and are used to identify the drawbacks of the push-pull converter when being compared to the 2L interleaved forward converter. For the push-pull topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the push-pull topology are depicted in Fig. 14. Table 4 summarizes the equations for the push-pull topology.

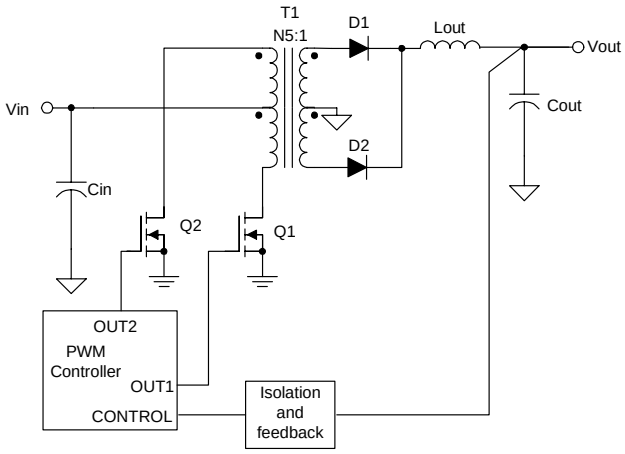

Fig. 13. Push-pull converter.

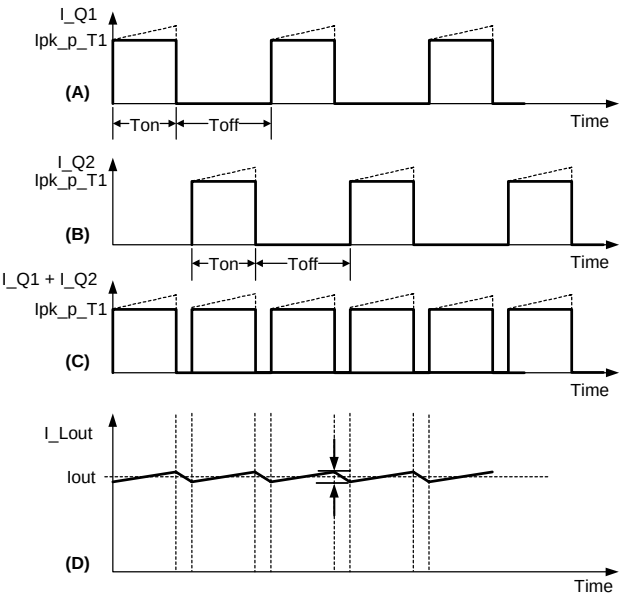

Fig. 14. Waveforms for push-pull converter (D = 0.4).

TABLE 4. PUSH-PULL CONVERTER EQUATIONS

Parameter	Push Pull
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N5}$
Irms_s_T1	$Iout * \sqrt{D\max} + \frac{Iout}{2} * \sqrt{1 - 2 * D\max}$
Irms_p_T1	$\frac{Iout}{N5} * \sqrt{D\max}$
Nx_min	$\frac{Vin\_\min * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N5} * \sqrt{2 * D\max * (1 - 2 * D\max)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1 - 2 * D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$2 * Vin\_\max$
Vpk_D1	$\frac{2 * Vin\_\max}{N5}$
Vpk_D2	$\frac{2 * Vin\_\max}{N5}$
Ipk_D1	$Iout$

Summary of Push-Pull vs. 2L Interleaved Forward Converter

Advantages of 2L interleaved forward converter vs. push-pull topology:

- Reduced transformer peak currents
- Reduced transformer RMS secondary current
- Reduced peak voltage stress on primary switches
- Reduced peak voltage stress on output rectifiers
- Reduced inductor currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. push-pull topology:

- Increased component count
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

C. Half-Bridge Circuit Topology

The main benefit of the half-bridge topology over the previous topologies is that the peak voltage on the power switches is only equal to the input voltage. Referring to Fig. 15, the same quantities listed above are compared against the 2L interleaved forward converter. In the half-bridge topology the maximum duty cycle for each switch is limited to 0.5 in order to avoid cross conduction between the switches. Typical waveforms for the half-bridge topology are depicted in Fig. 16. Table 5 summarizes the equations for the half-bridge topology.

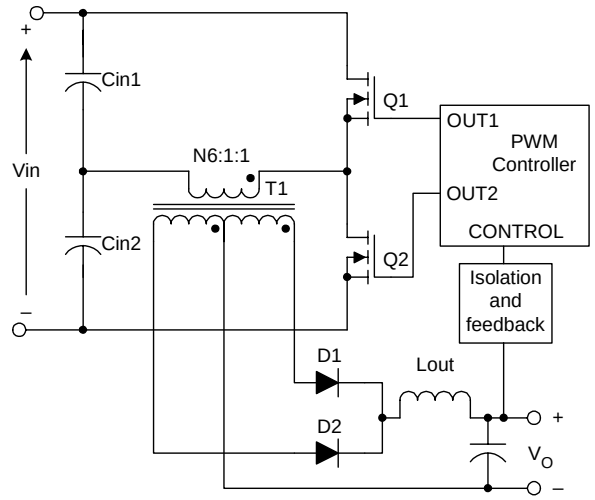

Fig. 15. Half-bridge converter.

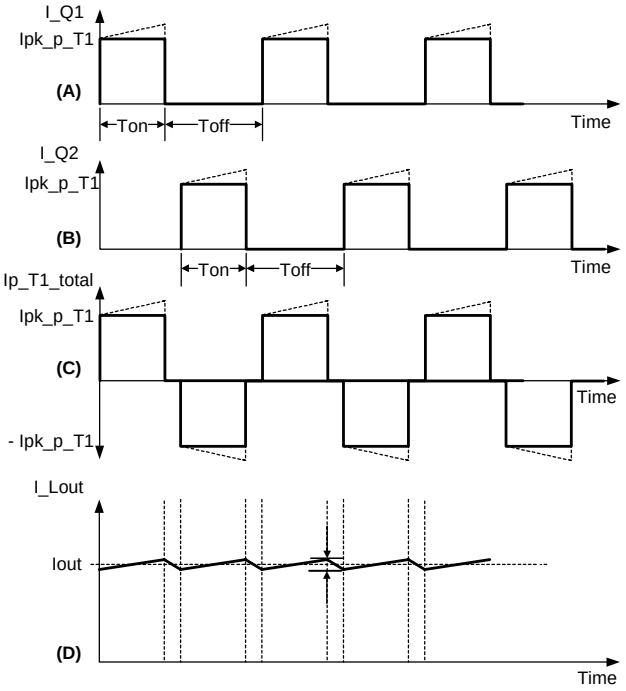

Fig. 16. Waveforms for half-bridge converter power stage (D = 0.4).

TABLE 5. HALF-BRIDGE CONVERTER EQUATIONS

Parameter	Half Bridge
Ipk_s_T1	$Iout$
Ipk_p_T1	$\frac{Iout}{N6}$
Irms_s_T1	$Iout * \sqrt{D\max} + \frac{Iout}{2} * \sqrt{1-2*D}$
Irms_p_T1	$\frac{Iout}{N6} * \sqrt{2*D\max}$
Nx_min	$\frac{\frac{Vin\_\min}{2} * 2 * D\max}{Vout + Vd}$
Icin_acrms	$\frac{Iout}{N6} * \sqrt{D\max * (1-D\max)}$
I_Lout_pp	$\frac{(Vout + Vd) * (1-2*D\max)}{Lout * Fs}$
Icout_acrms	$\frac{I\_Lout\_pp}{2} * \sqrt{\frac{1}{3}}$
Vpk_Q1	$Vin\_\max$
Vpk_D1	$\frac{Vin\_\max}{N6}$
Vpk_D2	$\frac{Vin\_\max}{N6}$
Ipk_D1	$Iout$

Summary of HB vs. 2L Interleaved Forward Converter

Advantages of 2L interleaved forward converter vs. half-bridge topology:

- Reduced transformer peak currents
- Reduced transformer RMS currents
- Reduction of EMI energy due to lower peak currents
- Reduced peak voltage stress on output rectifiers
- Reduction of EMI energy at higher frequencies due to longer allowable on times
- Reduced inductor currents
- Distribution of heat generating elements

Disadvantages of 2L interleaved forward converter vs. half-bridge topology:

- Increased component count
- Increased peak voltage stress on primary switches
- Possible increase in area of components
- Control complexity of interleaved drive signals, requires greater than 50% duty cycle per switch

Table 6 contains 200-W design examples for each of the buck derived topologies and Table 7 contains 500-W design examples. The following assumptions were made:

- The output inductance values are equal for all topologies (2L output inductors carry only half the load current).
- The duty cycle for the 1L interleaved forward converter is ½ of that for the 2L interleaved forward converter
- The switching frequency is equal to 500 kHz
- The input range is 36 Vdc – 75 Vdc
- The output voltage is 12 V for all topologies.

TABLE 6. COMPARISON TABLE FOR 200-W DESIGN EXAMPLES

200 W	Topology				
Parameter	**Forward**	**Interleaved Forward (2L)**	**Interleaved Forward (1L)**	**Push Pull**	**Half Bridge**
Dmax	0.52	0.52	0.26	0.45	0.45
Lout – (µH)	3.20	3.20	3.20	3.20	3.20
Ipk_s_T1 – (A)	16.7	8.3	16.7	16.7	16.7
Ipk_p_T1 – (A)	11.6	5.8	11.6	6.7	13.4
Irms_s_T1 – (A)	12.0	6.0	8.5	13.8	13.8
Irms_p_T1 – (A)	8.3	4.2	5.9	4.5	12.7
Nx_min	1.44	1.44	1.44	2.49	1.25
Icin_acrms – (A)	5.8	1.1	5.8	2.0	6.7
I_Lout_pp – (A)	3.9	3.9	3.9	0.8	0.8
Ilout_total_pp – (A)	N/A	0.3	N/A	N/A	N/A
Icout_acrms – (A)	1.1	0.1	1.1	0.2	0.2
Vpk_Q1 – (V)	75.0	75.0	48.6	150.0	75.0
Vpk_D1 – (V)	27.1	27.1	33.8	60.2	60.2
Vpk_D2 – (V)	52.1	52.1	52.1	60.2	60.2
Ipk_D1 – (A)	16.7	8.3	16.7	16.7	16.7

TABLE 7. COMPARISON TABLE FOR 500-W DESIGN EXAMPLES

500 W	Topology				
Parameter	**Forward**	**Interleaved Forward (2L)**	**Interleaved Forward (1L)**	**Push Pull**	**Half Bridge**
Dmax	0.52	0.52	0.45	0.45	0.45
Lout – (µH)	3.20	3.20	3.20	3.20	3.20
Ipk_s_T1 – (A)	41.7	20.8	41.7	41.7	41.7
Ipk_p_T1 – (A)	28.9	14.5	16.7	16.7	33.4
Irms_s_T1 – (A)	30.0	15.0	28.0	34.5	34.5
Irms_p_T1 – (A)	20.9	10.4	11.2	11.2	31.7
Nx_min	1.44	1.44	2.49	2.49	1.25
Icin_acrms – (A)	14.5	2.8	5.0	5.0	16.6
I_Lout_pp – (A)	3.9	3.9	0.8	0.8	0.8
Ilout_total_pp – (A)	N/A	0.3	N/A	N/A	N/A
Icout_acrms – (A)	1.1	0.1	0.2	0.2	0.2
Vpk_Q1 – (V)	75.0	75.0	65.5	150.0	75.0
Vpk_D1 – (V)	27.1	27.1	26.3	60.2	60.2
Vpk_D2 – (V)	52.1	52.1	30.1	60.2	60.2
Ipk_D1 – (A)	41.7	20.8	41.7	41.7	41.7
For this example the max duty cycle for the 1L interleaved forward converter was increased to 0.45.					

IV. Single Flyback Converter in Discontinuous Conduction Mode (DCM)

Fig. 3 shows a single flyback converter. Table 8 summarizes the design equations that are used to compare it against its interleaved counterpart shown in Fig. 17. More detail on how to derive these equations is given in the following section dealing with the interleaved flyback topology.

Table 8. Single Flyback Converter Equations

Parameter	Flyback
Ipk_s_T1	$N2 * Ipk\_p\_T1$
Ipk_p_T1	$\frac{Vin\_\min * Ton\_\max}{Lp}$
Irms_s_T1	$N2 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right)}$
Irms_p_T1	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right)}$
Nx_min	$\frac{Vpk\_Q1 - Vin\_\max}{Vout + Vd}$
Icin_acrms	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right) * \left(1 - \frac{3 * D}{4}\right)}$
Icout_acrms	$N2 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right) * \left(1 - \frac{3 * Tr}{4 * Ts}\right)}$
Vpk_Q1	$Vin\_\max + N2 * (Vout + Vd)$
Vpk_D1	$\frac{Vin\_\max}{N2} + Vspike$
Ipk_D1	$N2 * Ipk\_p\_T1$

D. Interleaved DCM Flyback Converter

The circuit depicted in Fig. 17 is an interleaved flyback converter. The duty cycle for each phase of an interleaved flyback is not limited to less than 50% because the secondaries inherently have high output impedance and resemble a current source. Fig. 18 shows the input and output ripple currents and their intended overlap at an individual phase duty cycle of 60 percent. This section and the following example show that the interleaved flyback converter is applicable to power levels twice as high as the single flyback converter.

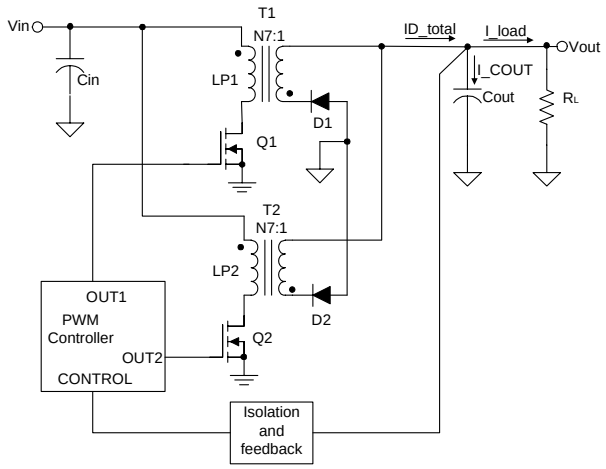

Fig. 17. Interleaved flyback converter.

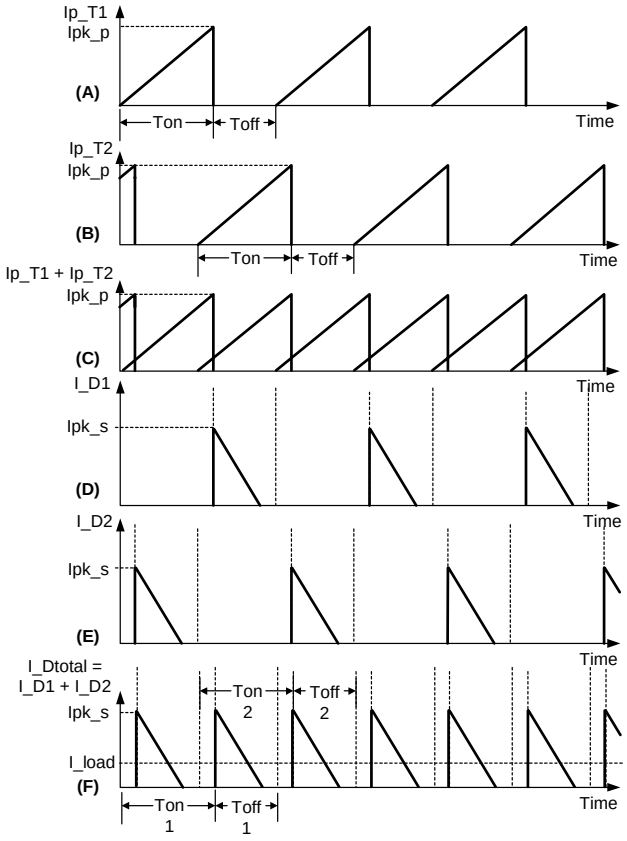

Fig. 18. Interleaved flyback converter waveforms, (A) primary transformer current of phase 1, (B) primary transformer current of phase 2, (C) sum of current waveforms "a" and current waveform "b" seen at the input capacitor, (D) secondary transformer current of phase 1, (E) secondary transformer current of phase 2, (F) sum of current waveforms "d" and current waveform "e" just prior to the output capacitor (D = 0.6).

E. Design Equations for an Interleaved DCM Flyback Converter

As with the single interleaved flyback, the first step is to understand the balance equations that allow the DCM flyback converter to regulate its output voltage. Fig. 17 shows an interleaved flyback circuit and Fig. 18 the associated current waveforms for DCM operation. Line regulation is achieved by varying the duty cycle of the power switch such that the product of the switch on time and the input voltage is a constant. This results in constant peak inductor current which translates to a constant output power. During the period when Q1 or Q2 is on, energy is transferred from the input capacitor, Cin, to the primary inductance, Lp, of the transformer. The magnitude of this stored energy per phase is given by:

$$Win = \frac{1}{2} * Lp * (Ipk\_p)^2$$

where Ipk_p is the peak primary current for each phase.

No energy is transferred to the secondary circuit during this period. When Q1 is off, all the energy stored in the flyback transformer is delivered, by way of the secondary winding, to the output filter capacitor and load. Because there are two power stages in parallel, each power stage only needs to deliver one half (½) of the total input power. The average input power is given by:

$$Pin = \frac{Win1}{Ts} + \frac{Win2}{Ts}$$

where,

$$Win1 = \frac{Lp1 * Ipk\_p\_T1^2}{2}$$

$$Win2 = \frac{Lp2 * Ipk\_p\_T2^2}{2}$$

$$Ts = \frac{1}{Fs}$$

With the assumptions that Lp1 = Lp2 and Ipk_p_T1 = Ipk_p_T2, the above equation simplifies to:

$$Pin = \frac{Lp1 * Ipk\_p\_T1^2}{Ts}$$

The peak primary current (Ipk_p_T1) is dependent on the input voltage (Vin), the primary inductance, Lp, and the on time of Q1 (Ton):

$$Ipk\_p\_T1 = \frac{Vin * Ton}{Lp}$$

The average power output is related to the output voltage and load resistance, by:

$$Po = \frac{Vo^2}{RL}$$

Taking into account the efficiency of the power converter gives a more accurate calculation for the peak input current.

$$Pin = \frac{Po}{\eta}$$

where η is the efficiency of the power converter.

Substituting for pin and Ipk_p_T1 in the above equations yields:

$$\frac{Vo^2}{\eta * RL} = \frac{(Vin * Ton)^2}{Lp * Ts}$$

The DC output voltage is therefore:

$$Vout = Vin * Ton * \sqrt{\frac{\eta * RL}{Lp * Ts}}$$

or

$$Vout = Vin * D * \sqrt{\frac{\eta * RL * Ts}{Lp}}$$

$$D = \frac{Ton}{Ts}$$

Note that for a discontinuous flyback converter, the output voltage varies directly with both Vin and the square root of RL.

Because of the parallel power stages the transformer peak and RMS currents are reduced by a factor of 2.

F. Power Switch Peak Voltage

The turns ratio of the transformer is determined by setting an upper limit on the peak voltage seen by the primary switch, Vpk_Q1 = Vpk_Q2, with some ample margin to accommodate any leakage inductance spikes that may be present on the drain waveform. In general, the peak voltage on the main switches is selected to fit into the lowest voltage rated switches possible.

$$Vpk\_Q1 = Vin + N7 * (Vout + Vd)$$

G. Primary Inductance Selection to Ensure DCM

In order to guarantee that the power stage remains in the discontinuous conduction mode throughout the entire input voltage range the maximum on time is selected according to the following equation, at Vin_min.

$$Ton\_\max = \frac{(Vo + Vd) * N7 * 0.8 * Ts}{Vin\_\min + N7 * (Vo\_Vd)}$$

$$D\max = \frac{Ton\_\max}{Ts}$$

The primary inductance is then calculated as:

$$Lp = \frac{(Vin\_\min * Ton\_\max)^2}{\frac{Pout}{2 * \eta} * 2 * Ts}$$

Here, the output power is divided by two because the above equation is setting the inductance for each power stage and each power stage only needs to deliver half of the total input power.

H. *Transformer Primary Peak Current*

The transformer primary peak current is equal to:

$$Ipk\_p\_T1 = \frac{Vin\_\min * Ton\_\max}{Lp}$$

I. *Transformer RMS Currents*

Calculate the primary RMS current, Irms_p_T1:

$$Irms\_p\_T1 = Ipk\_p\_T1 * \sqrt{\frac{D}{3}}$$

The DC component of the primary transformer current, Idc_p_T1, is:

$$Idc\_p\_T1 = Ipk\_p\_T1 * \frac{D}{2}$$

The secondary currents have the same shape as the primary current. The only adjustments in the equations are to replace the primary peak current with N7*Ip_pk and change D to Tr/Ts where Tr is the ramp down time of the secondary current. Because the circuit was designed to operate in DCM, Tr is required to be less than Toff and hence it is not valid to simply replace D by 1-D as would be the case for the continuous conduction mode (CCM).

$$Tr = Ipk\_s\_T1 * \frac{L\sec}{V\sec}$$

where,

$$Ipk\_s\_T1 = N7 * Ipk\_p\_T1$$

$$L\sec = Lp * \left(\frac{1}{N7}\right)^2$$

$$V\sec = Vout$$

hence,

$$Tr = \frac{Ipk\_p\_T1 * Lp}{N7 * Vout}$$

The secondary RMS current is then:

$$Irms\_s\_T1 = N7 * Ipk\_p\_T1 * \sqrt{\frac{Tr * Fs}{3}}$$

The DC component of the secondary transformer current, Idc_s_T1, is:

$$Idc\_s\_T1 = N7 * Ipk\_p\_T1 * \frac{Tr * Fs}{2}$$

J. *Input Capacitor RMS Current*

The AC component of the primary current waveform, Icin_acrms which is the AC RMS current that flows through the input capacitors, is calculated in Appendix A. There is not a closed form expression given so implementing the equations in an automated calculation program like MathCAD™ is suggested.

K. *Output Capacitor RMS Current*

The AC component of the secondary current waveform, Iacrms_s_T1, which is the RMS current in the output capacitors, is given by:

$$Icout\_acrms = Iacrms\_s\_T1$$

$$Icout\_acrms = N7 * Ipk\_p\_T1 * \sqrt{\frac{2 * Tr * Fs}{3} * \left(1 - \frac{3 * 2 * Tr * Fs}{4}\right)}$$

L. Output Rectifier Peak Current

The peak secondary current is equal to the peak diode current

$$Ipk\_D1 = N7 * Ipk\_p\_T1$$

Summary of Interleaved-Flyback vs. Single-Flyback Converter

Advantages of interleaved flyback converter vs. single flyback:

- Reduced transformer and semiconductor peak currents
- Reduced transformer and semiconductor RMS currents
- Reduced input and output capacitor RMS currents
- Reduction of EMI energy due to lower peak currents
- Distribution of heat generating elements

Disadvantages of interleaved flyback converter vs. single flyback:

- Increased component count
- Possible increase in component area
- Control complexity of interleaved drive signals for Dmax greater than 50%

TABLE 9. INTERLEAVED FLYBACK CONVERTER EQUATIONS

Parameter	Interleaved Flyback
Ipk_s_T1	$N7 * Ipk\_p\_T1$
Ipk_p_T1	$\frac{Vin\_\min * Ton\_\max}{Lp}$
Irms_s_T1	$N7 * Ipk\_p\_T1 * \sqrt{\left(\frac{Tr}{3 * Ts}\right)}$
Irms_p_T1	$Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right)}$
Nx_min	$\frac{Vpk\_Q1 - Vin\_\max}{Vout + Vd}$
Icin_acrms	D<=0.5; $Ipk\_p\_T1 * \sqrt{\left(\frac{D}{3}\right) * \left(1 - \frac{3 * D}{4}\right)}$ D>0.5; See Appendix A
Icout_acrms	$N7 * Ipk\_p\_T1 * \sqrt{\left(\frac{2*Tr}{3*Ts}\right) * \left(1 - \frac{3*2*Tr}{4*Ts}\right)}$
Vpk_Q1	$Vin\_\max + N7 * (Vout + Vd)$
Vpk_D1	$\frac{Vin\_\max}{N7} + Vspike$
Vpk_D2	$\frac{Vin\_\max}{N7} + Vspike$
Ipk_D1	$N7 * Ipk\_p\_T1$

M. Interleaved Flyback Design Example

As an example consider the following design specifications for an interleaved flyback converter designed to operate in DCM:

- Vin_max = 375 Vdc
- Vin_min = 85 Vdc
- Vout = 12 V
- Pout = 200 W
- Fs = 50 kHz
- $\eta = 0.85$
- RL_min = $(Vout)^2$ / Pout = 0.72 Ω

Table 10, DCM single flyback converter vs. interleaved flyback converter, summarizes the values for the equations given in Tables 8 and 9. From these comparisons it is evident that the effect of interleaving power stages is to reduce the peak currents and the RMS currents to manageable levels, even for a 200-W example which would normally be considered outside of the reasonable power levels for a DCM flyback converter.

TABLE 10. DESIGN VALUES FOR 200-W FLYBACK EXAMPLES

200 W	Topology	
Parameter	**Flyback**	**Interleaved Flyback**
Dmax	0.505	0.505
Lp – (μH)	78.3	157
Ipk_s_T1 – (A)	122.3	61.1
Ipk_p_T1 – (A)	10.96	5.5
Irms_s_T1 – (A)	39.9	20.0
Irms_p_T1 – (A)	4.5	2.2
Nx_min	11.15	11.15
Icin_acrms - (A)	3.5	1.6
Icout_acrms – (A)	34.8	20.4
Vpk_Q1 – (V)	520.0	520.0
Vpk_D1 – (V)	33.6	33.6
Vpk_D2 – (V)	N/A	N/A
Ipk_D1 – (A)	122.3	61.1

V. HIGH POWER FACTOR (HIGH-PF) INTERLEAVED FLYBACK TOPOLOGY

A useful modification to the circuit in Fig. 17 is to use the DCM flyback converter as an isolated power factor correction (PFC) stage. The modified circuit is shown in Fig. 19. The main modification between Fig. 17 and 19 is that in Fig. 19 Cin is very small and as a result of the rectifier bridge and AC input, the voltage across Cin is a rectified sine wave at twice the AC line frequency. Also Cout is very large in order to suppress the line frequency ripple voltage on the output and to withstand a holdup time design requirement. In Fig. 19 the converter is operated in discontinuous conduction mode and the bandwidth of the control loop is intentionally much less than the line frequency so as to make the on time constant throughout one half of the line cycle. By operating the converter and control loop in this manner the average input current from the line resembles the wave shape of the line voltage, which by definition results in high power factor correction. With the converter operating in discontinuous conduction mode, this control technique allows unity power factor when used with converter topologies like flyback, Cuk, and SEPIC [3]. The instantaneous and average input current for one line cycle is shown in Fig. 20.

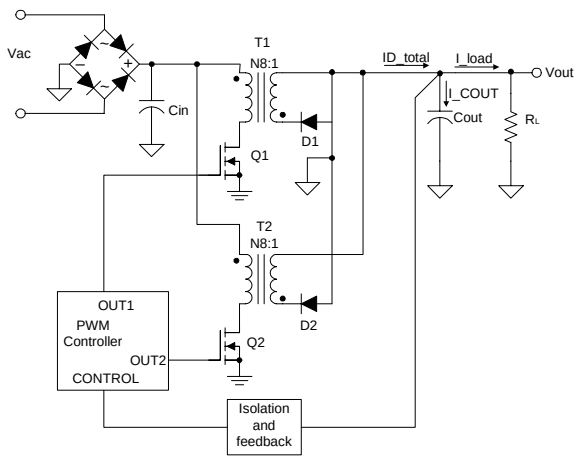

Fig. 19. High power factor (high-PF) interleaved flyback converter.

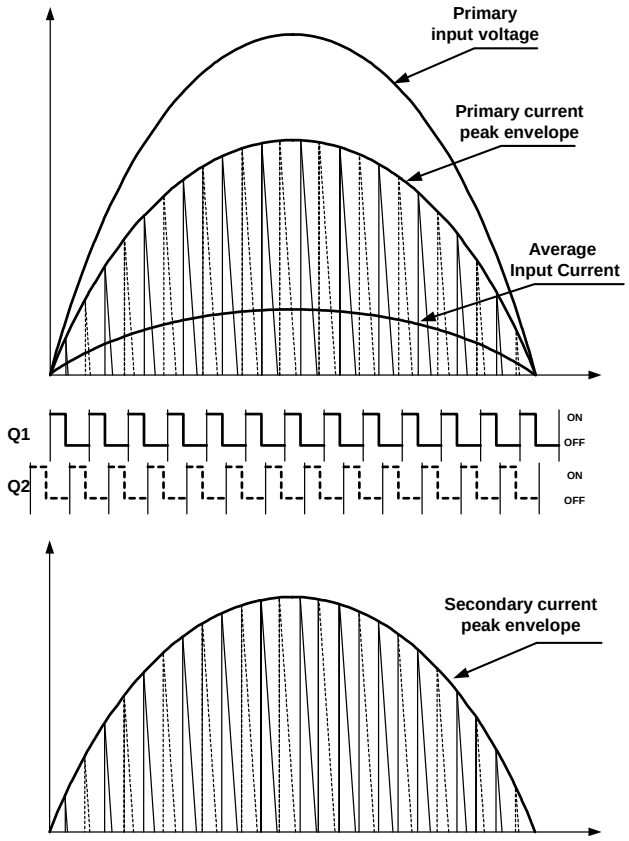

Fig. 20. (A) Input waveforms for high-PF interleaved flyback converter power, (B) Q1 power switch on and off times, (C) Q2 power switch on and off times, (D) secondary current waveform for high-PF interleaved flyback converter power stages.

VI. CONCLUSION

In recent years the usefulness of interleaving power stages has become apparent. The most well known application is in the powering of state-of-the-art microprocessors, commonly referred to as voltage regulator modules (VRMs). In VRM applications the power stages are non-isolated from their input to their output. This paper presented the benefits that interleaved topologies can have for isolated applications and in doing so has shown that the two inductor interleaved forward converter topology or the interleaved flyback converter topology are appropriate choices for many high power applications.

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[6] Raoji Patel, Glenn Fritz, "Switching Power Supply Design Review – 60 Watt Flyback Regulator" *Unitrode Power Supply Design Seminar SEM-100*, 1983

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[8] UCC28220/1 Data Sheet, Texas Instruments, (SLUS544)

[9] Peng Xu, "Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors", Dissertation submitted to the Faculty of the Virginia Polytechnic Institute and State University

[10] Lloyd H. Dixon, "Magnetics Design for Switching Power Supplies", *Unitrode Magnetics Design Handbook,* (MAG100A), 1999

[11] "UCC28220, UCC28221 Data Sheet – Interleaved Dual PWM Controller with Programmable Max Duty Cycle", Texas Instruments (SLUS544), September 2003

[12] Lloyd H. Dixon, "Minimizing Winding Losses in Magnetic Devices", Unitrode Power Supply Seminar, SEM-1400, (SLUP133), 2001

APPENDIX A.
CALCULATION OF THE AC RMS INPUT CURRENT FOR THE INTERLEAVED FLYBACK CONVERTER

This program calculates the ac rms current of two ramp waveforms which have the same duty cycle, but are 180 degrees out of phase from one another.

$Vin := 85$

$Lp := 156 \cdot 10^{-6}$

$Ts := \frac{1}{50000}$

$D := 0.51$

$Ton1 := D \cdot Ts$

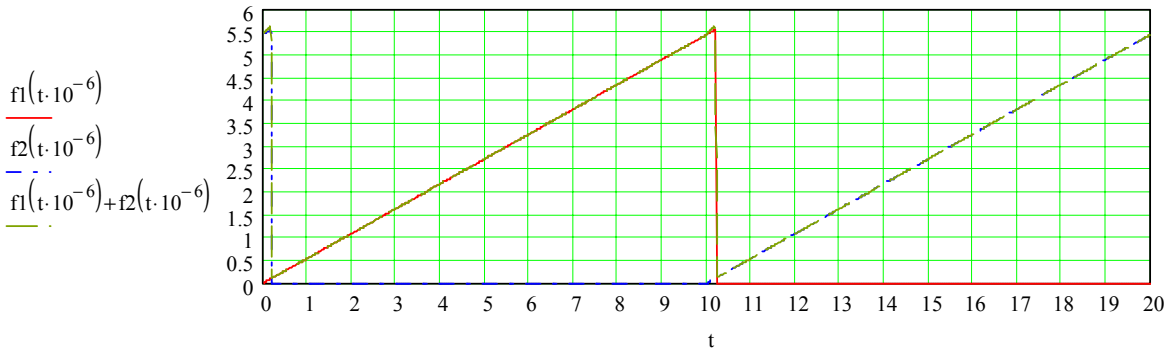
$Ton2 := Ton1$

$Ipk := \frac{Vin}{Lp} \cdot Ton1$

$Ipk = 5.558$ Amps

$$f1(t) := \begin{cases} \frac{Ipk}{Ton1} \cdot t & \text{if } t \le Ton1 \\ 0 & \text{otherwise} \end{cases}$$

$$f2(t) := \begin{cases} \frac{Ipk}{Ton2} \cdot (t + 0.5 \cdot Ts) & \text{if } 0 \le t \le (Ton2 - 0.5 \cdot Ts) \\ \frac{Ipk}{Ton2} \cdot (t - 0.5 \cdot Ts) & \text{if } t > 0.5 \cdot Ts \\ 0 & \text{otherwise} \end{cases}$$



$$Iin\_rms := \sqrt{\frac{1}{0.5 \cdot Ts} \cdot \int_0^{0.5 \cdot Ts} (f1(t) + f2(t))^2 \, dt}$$

$Iin\_rms = 3.266$ Arms

$$Iin\_dc := \frac{1}{0.5 \cdot Ts} \cdot \left[\int_0^{0.5 \cdot Ts} (f1(t) + f2(t)) \, dt \right]$$

$Iin\_dc = 2.861$ Adc

$$Iin\_acrms := \sqrt{Iin\_rms^2 - Iin\_dc^2}$$

$Iin\_acrms = 1.575$ Arms

APPENDIX B.
TWO INDUCTOR INTERLEAVED FORWARD CONVERTER DESIGN EXAMPLE

Specifications:

- V_{IN} = 36 V to 75 V
- $V_{UVLO-ON}$ = 34 V ±4%
- $V_{UVLO-OFF}$ = 32 V ±4%
- $V_{OVLO-OFF}$ = 85 V ±4%
- $V_{OVLO-ON}$ = 83 V ±4%
- V_{OUT} = 12 V ±3%
- Vripple < 1%
- P_{OUT} = 200 W
- $I_{OUT,MAX}$ = 16.7 A
- f_{SW} = 500 kHz (per phase)
- Isolation: 500 V
- PWM controller (UCC28221)
- Form factor: ½ brick

N. Topology: Interleaved Forward with Resonant Reset

The example schematic is shown in Fig. B1. The selection of the power stage is covered below. For information regarding the selection of the components around the PWM control chip refer to the application section in Reference 11.

O. Transformer Design

The transformer area product equation given in Reference 10 on page 4 through 8 provides an estimation of the required core size. In this example the transformer core was smaller than the predicted size from the area product estimate, but its operation and suitability for this application was verified at the extreme operating conditions. The transformer is a custom design from Payton America Inc (part number, 50863). The specifications are:

- Number of primary turns = 7 turns
- Primary magnetizing inductance = 35 μH
- Secondary number of turns = 5 turns
- Primary auxiliary winding = 5 turns

P. Input capacitor Selection

Referring to Table 6, the input capacitor AC RMS ripple current is 1.1 Arms at low line. The maximum AC RMS ripple current in the input capacitors occurs at high line. Evaluating the AC RMS ripple current equation at Vin-max yields a maximum current of 2.98 Arms. The selected film capacitors have an RMS current rating of 12 Amps which easily satisfies this requirement.

Q. Output Inductor Selection

The output inductor is equal to 3.2 μH, which yields a peak-to-peak output ripple current in each phase of 6.39 A at high line and 4.5 A at low line. This amount of ripple current is on the high side, but by factoring in the benefits of ripple current cancellation due to the interleaved power stages, the actual peak-to-peak ripple current seen by the output capacitor is only 4.3 A at high line and 0.343 A at low line.

R. Output Capacitor Selection

Because of the reduced peak-to-peak ripple current seen by the output capacitors, it is possible to use output capacitors with higher ESR than would be allowed for a single forward converter with the same amount of output inductance. In this example, the design specifications dictate that the design have less than 1% total output ripple voltage under worst case conditions, which is at high line. It is customary to allow the resistive portion of the output capacitor to account for half of the output ripple voltage specification. Hence, the maximum allowable equivalent series resistance (ESR) of the output capacitor is 0.014 Ω. The example design used three capacitors with 0.045 Ω of ESR each. Each capacitor has a capacitance of 82 μF.

S. Circuit Schematic

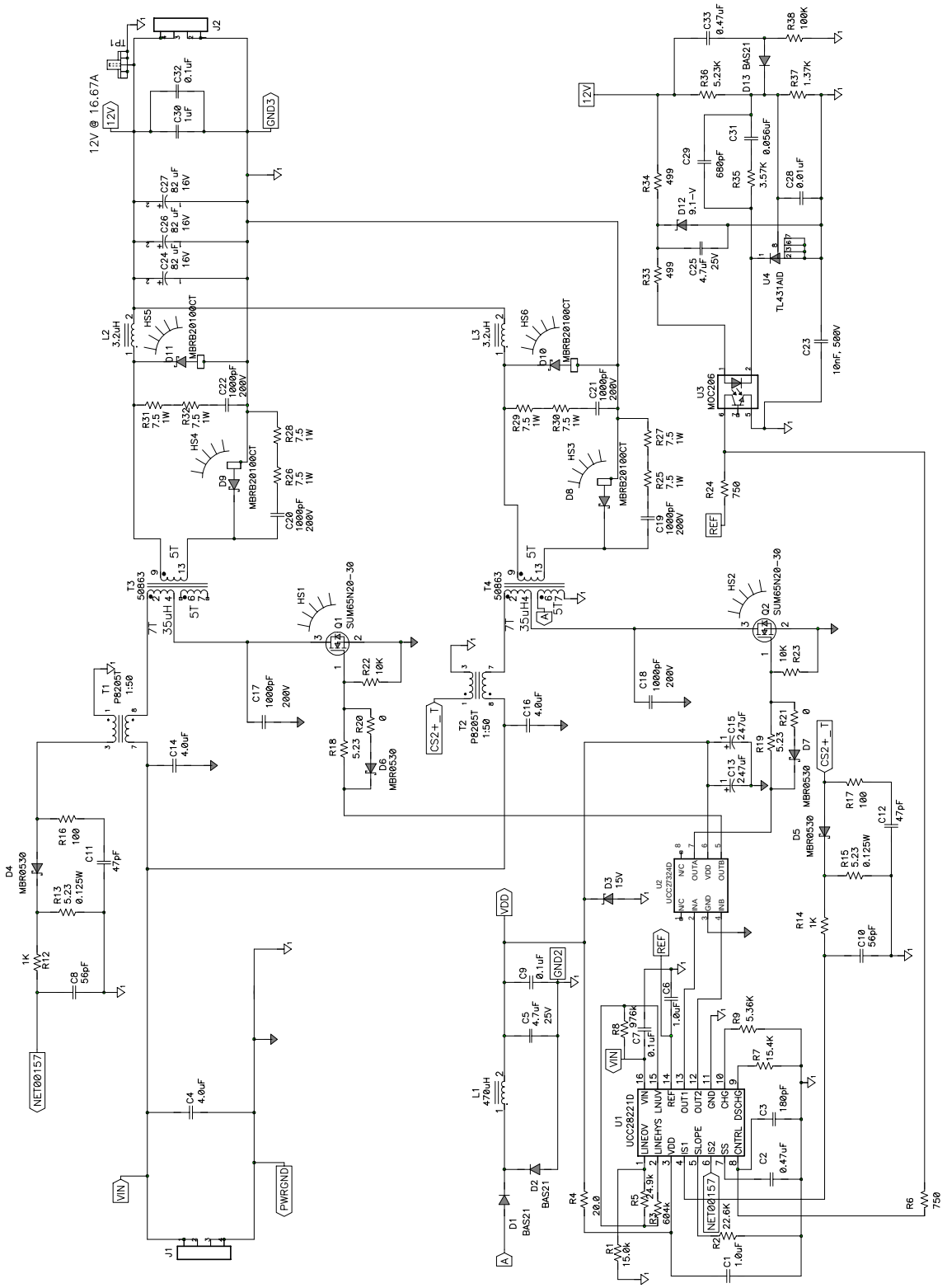


Fig. B1. 2L interleaved forward converter design example.

T. Layout

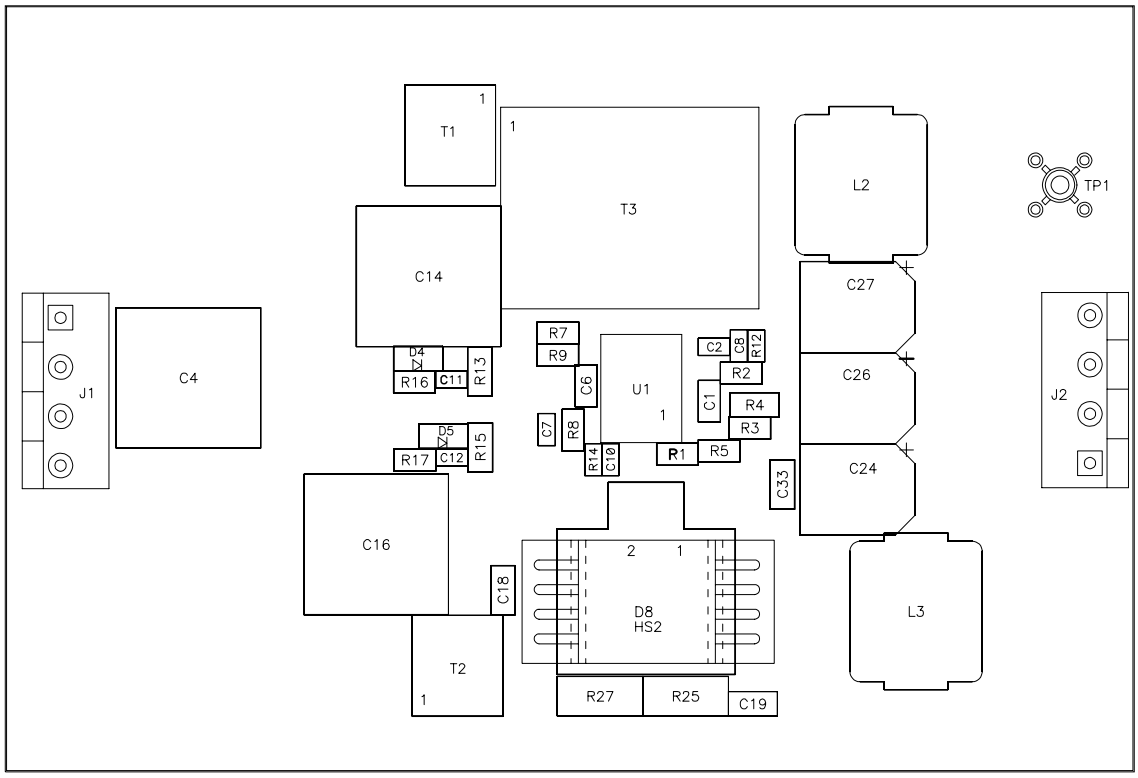


Fig. B2: Top view of PCB layout.

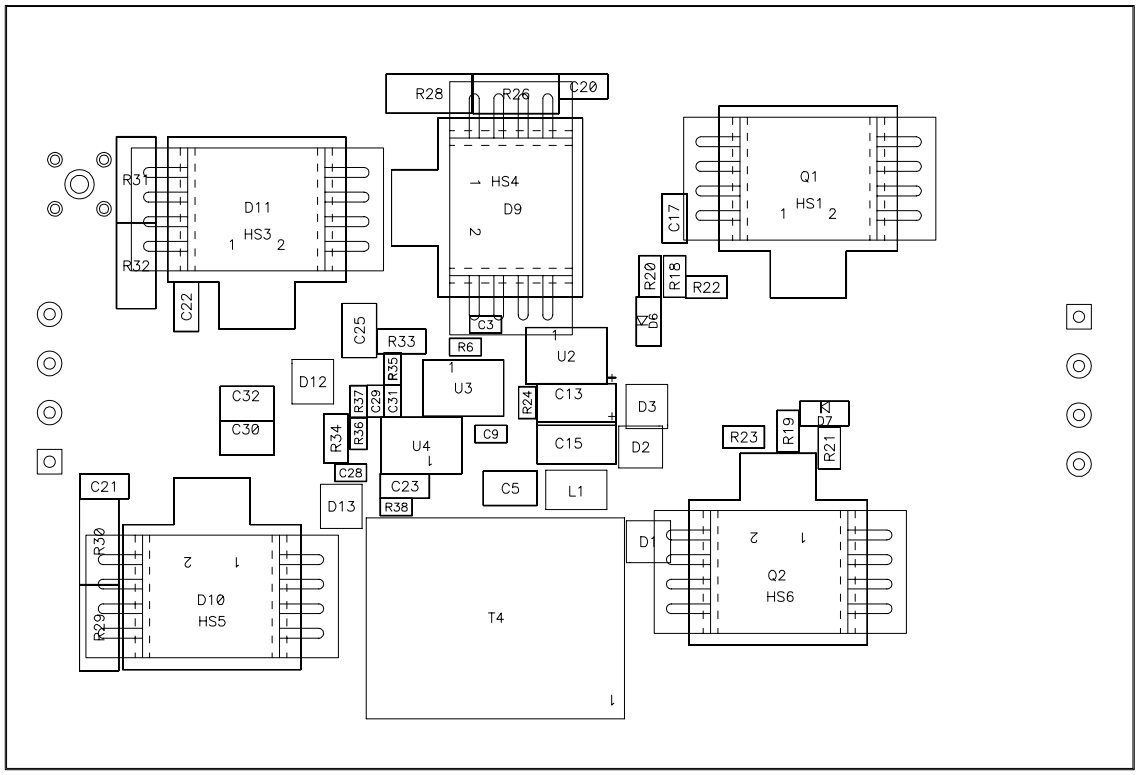


Fig. B3. Bottom view of PCB layout.

U. Drain Voltage Waveforms

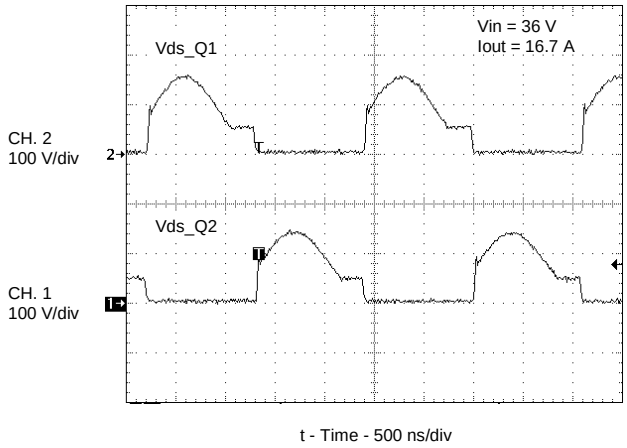


Fig. B4. Q1 and Q2 drain voltages (Vin = 36 V, Iout = 16.7 A).

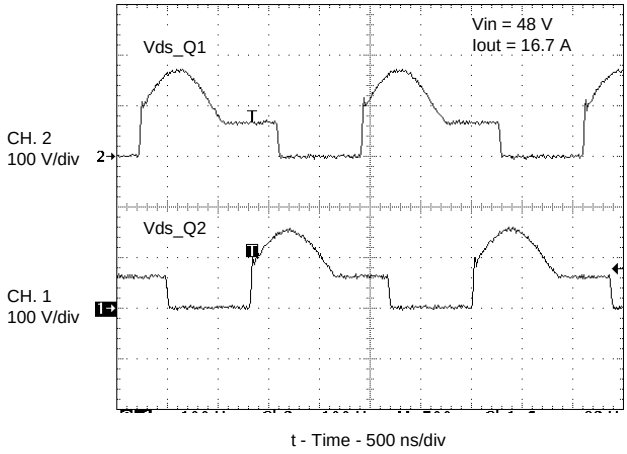


Fig. B5. Q1 and Q2 drain voltages (Vin = 48 V, Iout = 16.7 A).

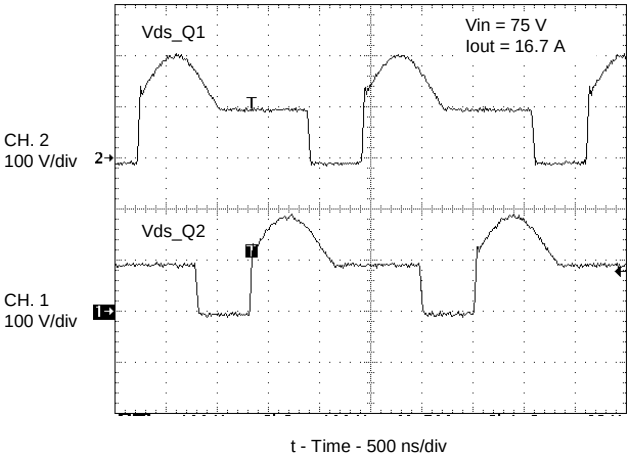


Fig. B6. Q1 and Q2 drain voltages (Vin = 75 V, Iout = 16.7 A).

V. Output Inductor Peak-to-Peak Ripple Current

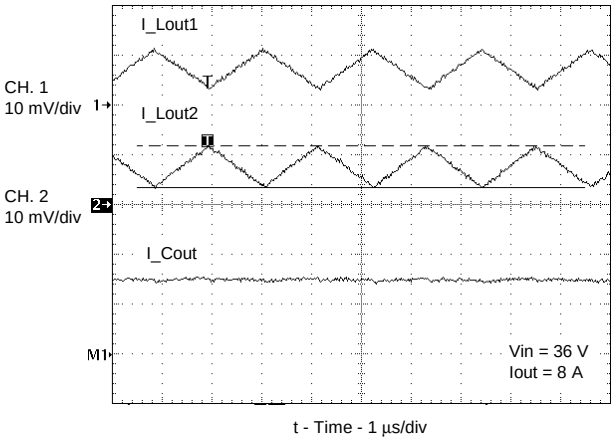


Fig. B7. Output inductor ripple currents and capacitor ripple current (Vin = 36 V, Iout = 8 A).

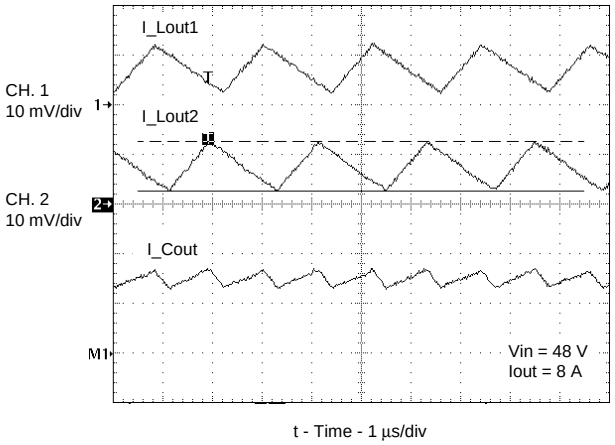


Fig. B8. Output inductor ripple currents and capacitor ripple current (Vin = 48 V, Iout = 8 A).

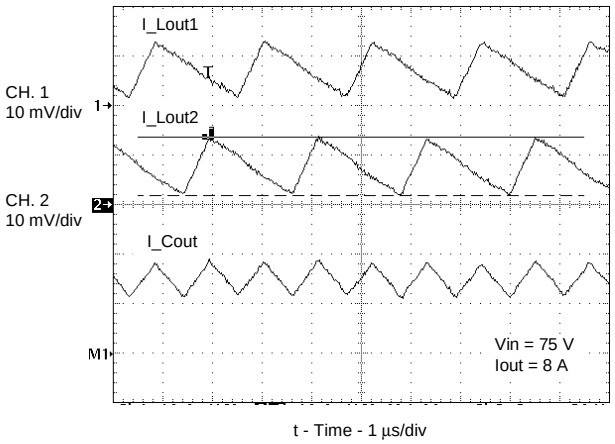


Fig. B9. Output inductor ripple currents and capacitor ripple current (Vin = 75 V, Iout = 8 A).

W. Transient Response 2 Phases and then 1 Phase

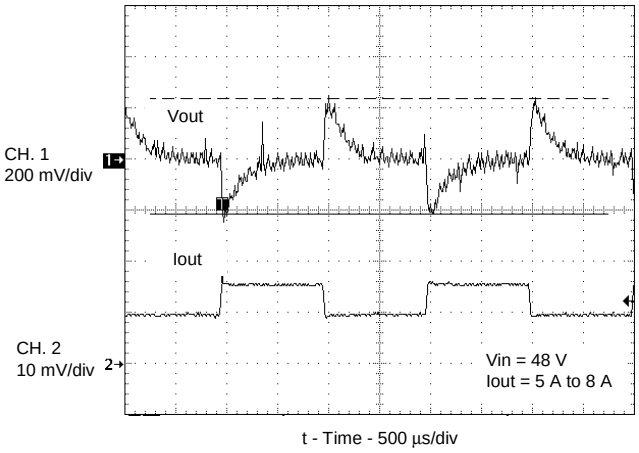


Fig. B10. Output transient response with 2 phases active (Vin = 48 V, Iout = 5 A to 8 A).

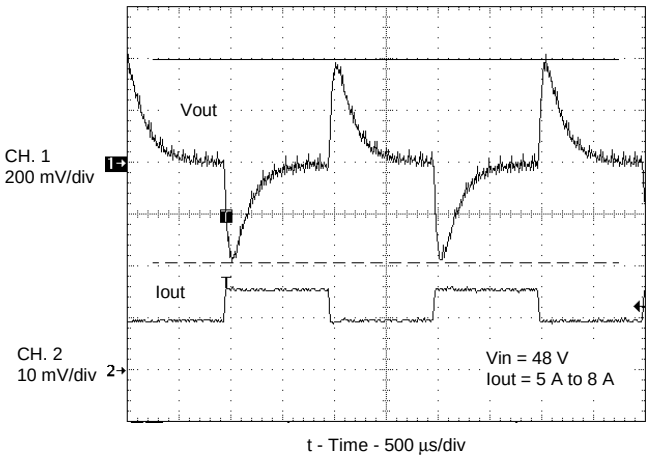


Fig. B11. Output transient response with only one phase active (Vin = 48 V, Iout = 5 A to 8 A).

X. Efficiency Curves

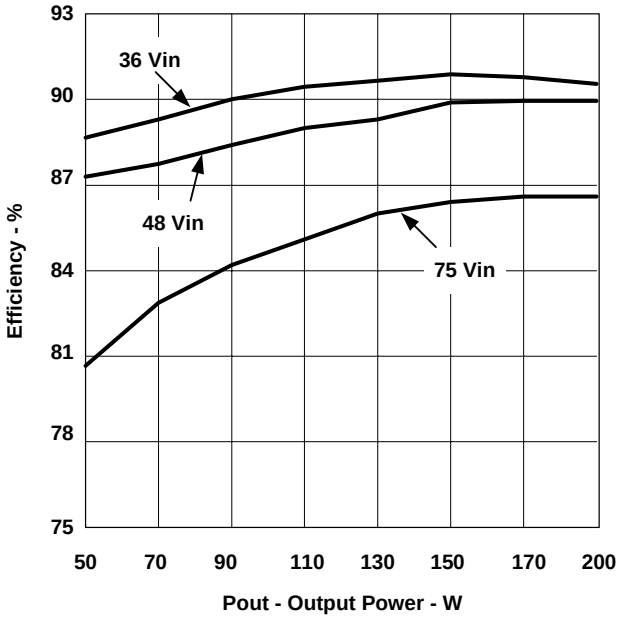


Fig. B12. Efficiency vs. output power.

Topic 6

A Practical Introduction to Digital Power Supply Control

Texas Instruments

A Practical Introduction to Digital Power Supply Control

Laszlo Balogh

ABSTRACT

The quest for increased integration, more features, and added flexibility – all under constant cost pressure – continually motivates the exploration of new avenues in power management. An area gaining significant industry attention today is the application of digital technology to power supply control. This topic attempts to clarify some of the mysteries of digital control for the practicing analog power supply designer. The benefits, limitations, and performance of the digital control concept will be reviewed. Special attention will be focused on the similarities and differences between analog and digital implementations of basic control functions. Finally, several examples will highlight the contributions of digital control to switched-mode power supplies.

I. INTRODUCTION

Power management is one of the most interdisciplinary areas of modern electronics, merging hard core analog circuit design with expertise from mechanical and RF engineering, safety and EMI, knowledge of materials, semiconductors and magnetic components. Understandably, power supply design is regarded as a pure analog field. But from the very early days, by the introduction of relays and later the first rectifiers, power management is slowly incorporating more and more ideas from the digital world. Ones and zeros are translated to "on and off's" but at the end a diode can be viewed as a "digital component". The introduction of switched mode power conversion required even more digital knowledge seeping into the repertoire of the practicing power supply designers. The know-how of the first discrete implementations of the PWM logic using comparators, gates and latches have faded away long time ago. Integrated pulse width modulator ICs have turned those simple digital circuits to history and have introduced even more digital content to power management.

Today's highly integrated power management ICs are packed with digital gates. The digital circuits allow the integration of some highly sophisticated features. Some examples are EEPROM based trimming after packaging to eliminate package stress related initial offsets, digital delay techniques to adjust proper timing of gate drive signals, microcontrollers and state machines for battery charging and management, and the list could go on.

If power conversion already incorporates such a large amount of digital circuitry, it is a legitimate question to ask: what has changed? What is this buzz about "digital power"?

II. GOING DIGITAL

Despite the tremendous amount of digital circuitry used in power management integrated circuits, it remained mainly hidden from the users. Most externally accessible functions are implemented by fundamentally analog circuit blocks today. Thus PWM controllers and other power management integrated circuits have successfully upheld their analog feel to them, making analog measurements and accepting analog controls. Their interfaces to the outside world are the various comparators and amplifiers monitoring the operating conditions and providing a choice of protection options for the designer of the power supply. This elemental principle prevails in existing controllers as demonstrated in Fig. 1.

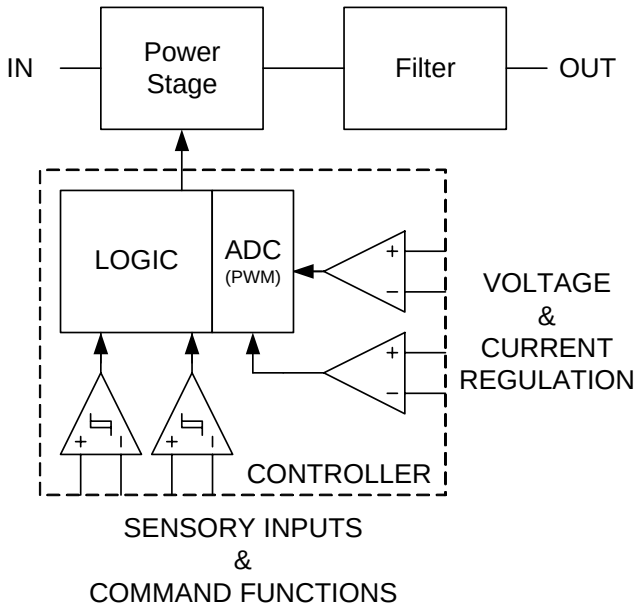


Fig. 1. Top level analog PWM controller architecture.

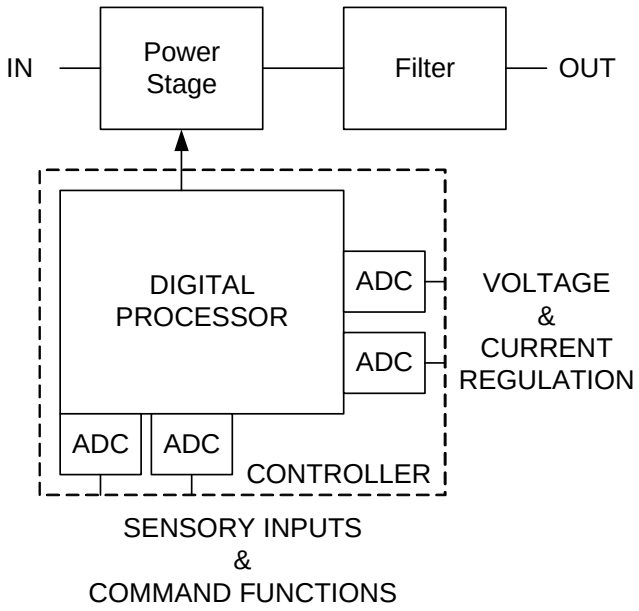


Fig. 2. Top level representation of a "digital" power supply.

Another important aspect to notice in Fig. 1 is the fact that the analog inputs are converted to digital signals as soon as practical. The point where the conversion is taking place in today's controllers varies depending on the signal type. When an under voltage lock out function is considered, the conversion is done by the simplest of all analog-to-digital converters, an UVLO comparator. Its input is strictly analog, while the output is already a digital signal, it is either high ("1") or low ("0"), with no intermediate value. But this digital output is also buried inside the integrated circuit and it is very rarely accessible by the designer. Output voltage and current regulation employs closed loop negative feedback, traditionally done by error amplifiers and the conversion to the digital "domain" is performed by a PWM comparator, again well concealed inside the IC.

A. What Really is "Digital Power"?

"Digital power" is an inaccurate description of a new direction in the *controller design* of the power supply to replace the analog circuits by digital implementations. Accordingly, "digital power" really stands for digital control of the power supply. Digital power supply control attempts to move the barrier between the analog and digital sections of the power supply right to the pins of the control IC.

This fundamental change in the control philosophy is summarized in Fig. 2. When comparing Fig. 1 and 2, it is important to emphasize that the deployment of digital control had no effect on the operating principle and the design of the power stage. The specification of the power supply still determines the choice of topology, the selection of power components and the required control functions. That leaves a fair amount of design tasks still in the analog realm for the power supply expert.

B. What is Changing?

The striking difference between "analog" and "digital" control is the quality and the amount of information available for the controller to make decisions regarding the operation of the power stage. For example, the output of a comparator carries limited information about the monitored parameter, i.e. only whether it is above or below a threshold. When the border between analog and digital is moved from the output of a comparator to the input by converting the actual information to digital form, the controller suddenly knows the concrete value of the parameter. Now, in addition to comparing it to a threshold, changes in the parameter's value can be detected, stored and later reported back to a supervisory system. If necessary, parameter values can be combined

with other information in complex algorithms to perform even more sophisticated functions.

Of course, this large amount of information can not be processed by traditional logic gates. Digital controllers take advantage of large scale integration offered by state of the art semiconductor technology. Typically, a microcontroller (μC) or a digital signal processor (DSP) is at the heart of a suitable digital controller for power supply applications.

Another important controller property which changes significantly is the flexibility to implement various control algorithms. Traditional, "analog" controllers may employ sophisticated decision trees driven by the digital outputs of the various peripheral circuits. But the reactions to the changes in the operating conditions are pre-programmed and rigidly executed by the internal logic. For instance, the usual reaction to exceeding a current limit threshold is to shut down the converter and start over, hard coded into the logic of analog controllers. The power supply designer has no option and in most cases it requires a significant amount of external circuitry to circumvent some of the built-in features of the controllers. By the introduction of a digital engine such as a μC or DSP, the decision, how to react to certain conditions becomes user programmable. In the current limit example the designer might opt to let the power supply operate in current limit for a number of switching cycles before resorting to shutdown. This would allow riding through short overload conditions during transient operation. In other cases where this behavior is not necessary or outright dangerous, the controller could be programmed to shut down immediately.

Another area to address in digital control is to ensure stable operation of the power supply. The output voltage is still regulated by a closed negative feedback loop, but it will be the result of complex calculations performed by the μC or DSP. While stability criterias for a power supply with analog control is well established and understood by the designers, these control laws are not directly applicable to the digital controllers. The digital implementations require new expertise, being familiar with and being able to apply the stability requirements in the Z-domain. The Z-domain transfer function of a sampled data system can be used to predict the small signal behavior of the converter. Additional new problems surface as well, like bandwidth limitations, resolution issues in time and voltage measurements and limit cycle oscillation, just to mention a few which will be discussed later.

One more key aspect of digital implementations is to recognize that microcontrollers and DSPs are powered by very low voltages due to their semiconductor technologies. As a result they are not capable of directly interfacing with the power components, unlike their analog counterparts. Thus, they require their own low voltage supply and a suitable high current gate driver with a compatible input threshold and adequate output voltage range. These requirements establish a clear partitioning between the analog and digital sections of the power supply. A closer look of the fundamental architecture of a digitally controlled converter is shown in Fig. 3.

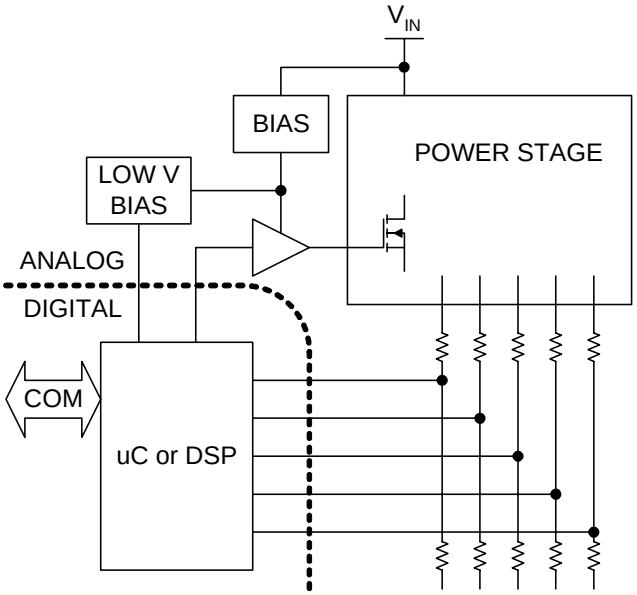


Fig. 3. Analog – digital boundary in a power supply.

The low voltage bias shown in Fig. 3 must be able to power the digital controller independently without operation of the power stage to allow initialization during start-up and to preserve intelligence during standby (disable) and short circuit operation when traditional bootstrap bias might not be available as a viable power source.

Furthermore, the output of the digital controller must be converted to a suitable signal to drive the power switches in the converter and all voltages must be scaled to the input voltage range of the analog inputs, usually determined by the reference voltage of the analog-to-digital converter on-board the digital controller.

C. Advantages of Digital Control

Flexibility is definitely the most noteworthy benefit of digital controllers. It is especially remarkable considering the consolidation of all necessary functions into one *highly integrated*, sophisticated controller. As mentioned before, by the introduction of a digital controller, the hardwired, hardly customizable control flow of analog controllers is exchanged for an open structure, where the designer has the ultimate freedom to decide the right course of action to a given stimuli. This new opportunity can be rather overwhelming for practicing power supply designers, because most of these decisions were made for them by the semiconductor manufacturers of analog controllers. In addition, this freedom comes with another new complication, the digital controller must be told what to do. Software must be written to program the execution of all the functions assigned to the μC or DSP. The software carries the knowledge and intellectual property which was previously realized in the controller hardware.

There are three major areas in the design where flexibility can provide significant benefits. The first one is *adjustability*. Every parameter which is measured or programmed can also be adjusted by the digital controller. These include voltage and current thresholds, operating frequency, thermal shut down, startup time, and so on.

The next level of flexibility is offered by the user defined *what-if decision* making process inside the digital controller. This tool can be exploited for enhanced functionality like green mode or low power stand-by operation, load share or hot swap control, just to mention a few. The foundation of these features is the option to invoke different control algorithms as the operating conditions of the power supply are changing. In addition, fault containment strategies can be refined and adapted as required by diverse applications. For example, once the output current of the converter is measured by the digital controller this information can be used to program fold back, constant power, constant current, delayed shutdown or any other mode of over current protection. Moreover, any combination of these output characteristics can be implemented without ever changing any components in the power supply.

The use of modern digital controllers also adds *communication* as a potential feature to the power supply. When this communication capability is utilized, the flexibility of the digital approach is greatly enhanced through the on-the-fly *programmability*. The adjustability of the converter's output voltage is a great advantage as demonstrated in processor applications using VID code. In a communication enabled power supply, not just the output voltage, but current limit, operating frequency and other vital operating parameters become programmable by a host system during operation. Beyond programming, communication permits *remote data logging* of the operating conditions of the power supply. By examining the data such as efficiency, output ripple, temperature rise, certain shifts in the measured parameters may be the leading indicators of pending failures. These trends can be used for failure prediction, down-time avoidance and intelligent fault management. In a centrally managed power supply, start-up, shut-down and sequencing can also be supervised remotely by a higher level supervisory system.

All these options and the corresponding computing power on-board can open the door for customization of future power supplies and entire power systems through software. This approach promotes platform development and a *faster Time to Market* window. Despite the potential standardization of the hardware, digital control allows unique *product differentiation* through software. The implementation methods of the various power supply features remain well protected due to the software code security feature of modern microcontrollers and DSPs which ensures that the program can not be read by unauthorized users.

In complex systems such as the telecommunication power infrastructure or high end computing environments, digital control also offers *reduced component count* even with the increased functionality. Fewer components mean *lower manufacturing cost* and *higher reliability*.

It is important to note though that all this flexibility and adjustability is restricted by the capabilities of the power stage. For example, widely varying output voltages might require different turn ratios in the transformer and filter inductors must be selected with the maximum output current in mind. Lowering the operating frequency still increases output ripple although it might improve light load efficiency. All these effects of the adjustable parameters must be carefully considered otherwise the performance of the power supply can be significantly penalized. But it is possible to use the same digital controller with several versions of the power stage, taking advantage of its ultimate flexibility.

D. Present Status of Digital Control in Power Management

The "digital revolution" is in its early phase in power supply applications. Its present state resembles the motion control and UPS field just some 20 years ago. The first digital controllers operated at moderate switching frequency and debuted in those applications in the early '80's.

The digital control acceptance rate was relatively slow, despite the fact that the technology was readily available and capable of performing the job. Microcontrollers and DSPs had sufficient computing power to handle speed control, sine wave generation and other similar low speed control function. In addition they offered the possibility of communication between a host supervisor and the equipment. As the performance has improved and the price of the digital controllers has dropped during the years, the technology became standard in most motor control and large UPS systems.

Digital control in power management is gaining considerable attention in recent years in academia and in the industry as well. Numerous publications in major conferences discuss the theoretical and practical aspects of digital control implementations. Significant interest of the subject had been expressed at APEC 2003 where the first Rap Session on digital power took place with participation from end users, power supply manufacturers and IC companies. The first Market Report was published by iSupply on digital power in early 2003.

A closer look at the reported results confirms that in power supplies, digital technology might not yet be ready for prime time. Some of the problem stems from the ever present price pressure the industry is operating under. Like any new technology, digital controllers cost more until reasonable sales volume is reached. Reaching a sufficient level of production is delayed by the required time to learn and introduce new design disciplines and to address manufacturing needs associated with digital controllers. Also hindering the effort is the lack of appropriate analog support components to go along with the microcontroller or DSP.

On the theoretical front, the majority of present implementations "translate" S-domain transfer functions to Z-domain. This approach permits utilization of the well understood linearized small signal model of the power supply. Once the poles and zeros are calculated to ensure the stability of the system, the Z-coefficients of the digital transfer function can be found easily. The weakness of this method is that by starting from a linearized model, the benefits of a higher performance non-linear control theory can not be fully utilized. As a result, the performance of power supplies using either digital or analog controllers are very similar today.

To set realistic expectations of today's digital implementations in power supplies, Table 2 attempts to highlight the pros and cons of the analog and digital approaches.

TABLE 1. COMPARISON OF ANALOG AND DIGITAL CONTROLLER PERFORMANCE (+ BETTER; - WORSE)

Control Properties	Analog	Digital
Switching frequency (CPU limitations)	+	-
Precision (tolerances, aging, temperature effects, drift, offset, etc.)	-	+
Resolution (numerical problems, quantization, rounding, etc.)	+	-
Bandwidth (sampling loop, ADC – DAC speed)	+	-
Instantaneous over current protection	+	-
Compatibility with power components	+	-
Power requirements	+	-
Communication, data management	-	+
Understanding theory	+	-
Advanced control algorithm (non-linear control, improved transient)	-	+
Multiple loops	-	+
Cost of controller	+	-
Cost of a platform (flexibility, time to market)	-	+
Component count (comparable functionality, integration)	-	+
Reliability	+	?

Achieving high switching frequency is definitely easier using analog controllers. Obtaining high enough clock frequency to implement direct digital pulse width modulation with reasonable resolution is the fundamental problem. Today's digital controllers with suitable clock speed for high switching frequency operation are not cost effective and consume a significant amount of bias power. Another area where speed is critical is the performance of the digital controller's analog-to-digital converter. The ADC's conversion time and the number of instructions needed to acknowledge the result have an effect on the digital controller's performance. Where sensing and reacting to certain conditions should happen simultaneously – peak current limiting for example – analog circuits still has a significant advantage over pure digital implementations. Furthermore, the repetition rate of converting important parameters like output voltage, impacts the bandwidth of the control algorithm. An additional important characteristic of the analog-to-digital converter is its resolution which can introduce rounding or quantization errors. These numerical issues are inherent in digital control and represent a new challenge for the power supply designer. On a positive note, digital components can offer better accuracy, great resilience against temperature drift and aging effects. Digital controllers are a better fit to implement advanced control algorithms and to manage multiple control loops if necessary.

In the most important comparison – cost – digital power supply control can be competitive. If all the functions provided by a digital implementation are necessary to meet specification, digital controllers will come out on top. In this case, component count and cost will be significantly lower than the cost of analog control circuits and the required additional support ICs to accomplish comparable features. When the only task is to regulate an output voltage, digital controllers might have a hard time competing on price. In this instance, a bigger picture should be considered to evaluate the real advantages of a digital implementation. If the design is expected to be re-used in several power supplies, the flexibility and possibility of quick modifications in software is a very valuable attribute of the digital implementation although it could be difficult to identify its cost benefit.

Finally, reliability is a key question. Analog controllers have a proven track record in power supply applications. They work reliably in harsh, noisy environment. Digital controllers have

proven to be very reliable as well, but not necessarily inside a power supply. It is unclear whether microcontrollers and DSPs will operate reliably under the same circumstances.

III. Digital Basics

To fully understand the potential benefits of digital control, some basic operating principles and terminology must be clarified. The two fundamental building blocks to understand are the time base and how the analog signals are converted to digital form. These two circuits interface with the surrounding analog world and are critical to the digital controller's performance.

A. Generating the Time Base

One of the first steps in the design procedure is to establish the operating frequency of the controller. It is usually defined by an on-board oscillator, often programmed by R-C timing components. A frequently used implementation of a simple analog oscillator is shown in Fig. 4.

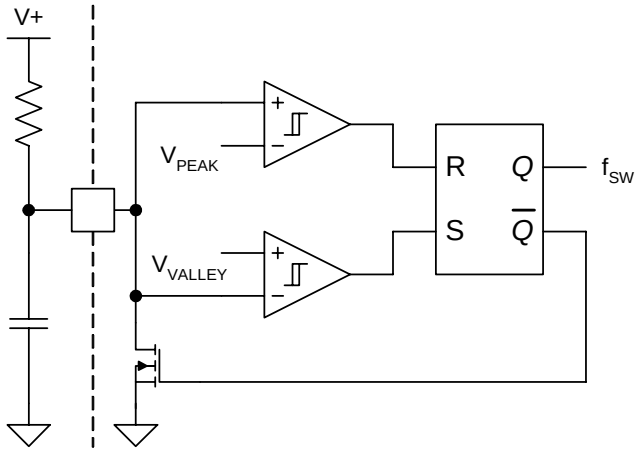


Fig. 4. Analog oscillator.

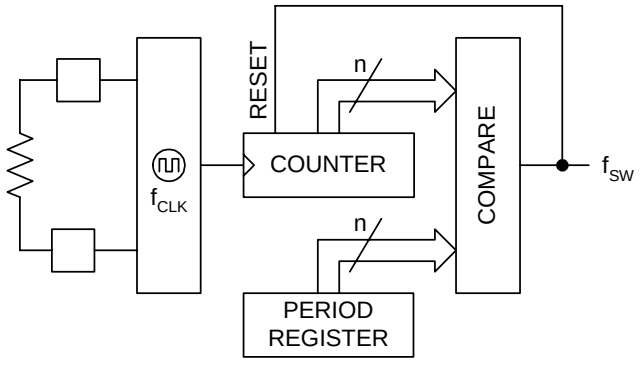


Fig. 5. Simplified digital oscillator ($f_{CLK} >> f_{SW}$).

Since the R and C values can be set to any desired value, this oscillator can run at any frequency within its wide operating range. In an analog implementation the controller's clock frequency and the converter's operating frequency (f_{SW}) are the same.

On the other hand, the clock frequency (f_{CLK}) of a microcontroller or a DSP is much higher than the actual operating frequency of the converter. The digital controller uses f_{CLK} as the time base for the central processor unit and its peripherals only. All other timing functions, including the switching period, must be generated using the internal resources of the digital controller.

Fig. 5 demonstrates the principle of deriving the switching frequency. Once the clock frequency of the digital controller and the switching frequency of the converter are fixed, the switching period can be established. The number of clock cycles in the switching period can be calculated by dividing the switching period by the clock period. This number is stored in the "period register". Every clock signal increments the counter by one and eventually the counter value will be equal to the period. At that time the digital comparator produces an output pulse which will reset the counter to zero. The frequency of the comparator output pulse is also the desired operating frequency of the converter.

As f_{CLK} increases with respect to f_{SW}, more clock cycles become available within a switching period to perform the complex arithmetic calculations, data conversions and housekeeping functions. This indicates that the higher clock frequency has a desirable effect on the performance of the digital controller.

Another important reason to push the clock frequency higher becomes clear when the relationship between the number of clock cycles in a switching period and the PWM resolution of the digital controller is investigated. An analog controller can command any pulse width as the decision is made using analog signals providing infinite resolution. In a digital controller the PWM pulse width is represented by an integer number of clock cycles calculated by the arithmetic unit, therefore the pulse width has a finite number of discrete values.

TABLE 2. EFFECTIVE NUMBER OF BITS, NUMBER OF CLOCK CYCLES PER PERIOD AND DUTY CYCLE RESOLUTION IN %, USING TYPICAL COMBINATIONS OF SWITCHING AND CLOCK FREQUENCIES

f_{SW} (kHz)	f_{CLK} - Clock Frequency (MHz)								
	1	2	4	8	20	40	100	150	
25	5.3	6.3	7.3	8.3	9.6	10.6	12.0	12.6	Bit resolution (eff.)
	40	80	160	320	800	1600	4000	6000	Clock cycles/period
	2.50	1.25	0.625	0.313	0.125	0.063	0.025	0.017	D resolution (%)
50	4.3	5.3	6.3	7.3	8.6	9.6	11.0	11.6	Bit resolution (eff.)
	20	40	80	160	400	800	2000	3000	Clock cycles/period
	5	2.50	1.25	0.625	0.250	0.125	0.050	0.033	D resolution (%)
100	3.3	4.3	5.3	6.3	7.6	8.6	10.0	10.6	Bit resolution (eff.)
	10	20	40	80	200	400	1000	1500	Clock cycles/period
	10	5	2.50	1.25	0.50	0.25	0.10	0.067	D resolution (%)
250	2.0	3.0	4.0	5.0	6.3	7.3	8.6	9.2	Bit resolution (eff.)
	4	8	16	32	80	160	400	600	Clock cycles/period
	25	12.5	6.25	3.125	1.250	0.625	0.250	0.167	D resolution (%)
500	1.0	2.0	3.0	4.0	5.3	6.3	7.6	8.2	Bit resolution (eff.)
	2	4	8	16	40	80	200	300	Clock cycles/period
	50	25	12	6.25	2.50	1.25	0.50	0.333	D resolution (%)
1000	0.0	1.0	2.0	3.0	4.3	5.3	6.6	7.2	Bit resolution (eff.)
	1	2	4	8	20	40	100	150	Clock cycles/period
	100	50	25	12.5	5.0	2.5	1.0	0.667	D resolution (%)

The pulse width of the digital controller can only be multiples of the clock period. The important characteristics of the digital PWM engine can be defined as a function of the switching frequency and the clock frequency as shown in Table 2.

For every combination there are three numbers in the table. The first number is called the effective number of bits and it signifies how many bits are required in the counter to be able to set up the desired switching frequency with a given clock frequency. The second number indicates how many clock cycles are available in a switching period. And the third number, which can be defined as:

$$D_{RES}(\%) = \frac{f_{CLK}}{f_{SW}} \cdot 100$$

gives the duty cycle resolution in percentage which is the most important parameter determining the performance of the digital controller. Due to the distinct values of the duty ratio of the digital controller, the output voltage of the converter can not be adjusted continuously. Depending on the difference between two neighboring duty cycle values, the output voltage resolution is also affected. A further variable to define how coarse the output voltage adjustment will be is the steady state operating duty ratio at nominal input, output conditions (D_{NOM}).

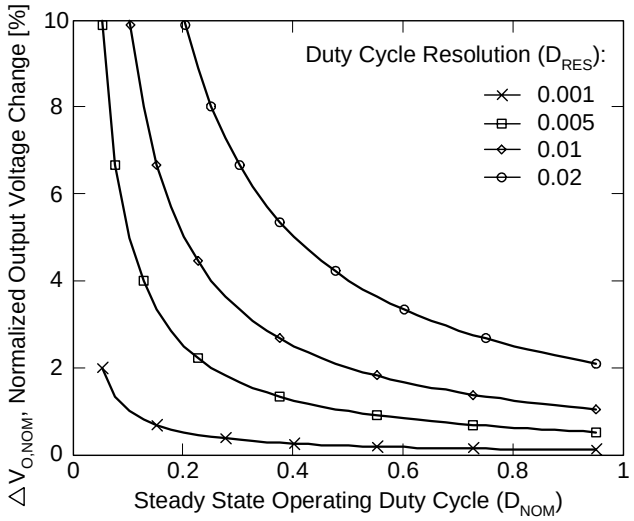


Fig. 6. The effect of duty cycle resolution on the output voltage resolution as a function of nominal operating duty ratio.

In Fig. 6, the curves represent the percentage of output voltage change in response to changing the converter's duty ratio between two neighboring discrete values. It is important to remember that the time difference between two neighboring duty ratio values is constant and it equals $1/f_{CLK}$. As Fig. 6 emphasizes, the same duty cycle step will result different output voltage changes depending on the nominal operating duty cycle of the converter. In other words, increasing the conduction time of the power supply's main switch by one clock period ($1/f_{CLK}$) at narrow operating duty ratio will raise the converter's output voltage more than the same change applied at wider nominal duty cycles. Therefore, in converters typically operating with narrow duty cycles – for example a 12V to 3.3V non-isolated buck converter – it is desirable to have a higher speed (f_{CLK}) digital controller even at moderate switching frequencies.

To further underline the impact of the duty cycle resolution, consider the above mentioned buck converter as an application example. The converter operates at 250kHz switching frequency using an 8 MHz digital PWM engine. The input is 12V and the output voltage is 3.3V. The required operating duty ratio would be:

$$D_{REQ} = \frac{V_{OUT}}{V_{IN}} = \frac{3.3}{12} = 0.275$$

The corresponding PWM pulse width is:

$$t_{ON} = \frac{D_{REQ}}{f_{SW}} = \frac{0.275}{250kHz} = 1.1\mu s$$

This requires;

$$n_{ON} = t_{ON} \cdot f_{CLK} = 1.1\mu s \cdot 8MHz = 8.8$$

number of clock cycles. Since the digital controller can not put out fractional number of clock cycles, the on-time will be the closest integer number of cycles, nine. This duty cycle will yield an output voltage of:

$$V_{O(n=9)} = V_{IN} \cdot n \cdot \frac{f_{SW}}{f_{CLK}} = 12V \cdot 9 \cdot \frac{250kHz}{8MHz} = 3.375V$$

While this value might satisfy the requirements of the design (+2.2%), it is important to determine what the output voltage would be at neighboring duty ratios:

$$V_{O(n=8)} = V_{IN} \cdot n \cdot \frac{f_{SW}}{f_{CLK}} = 12V \cdot 8 \cdot \frac{250kHz}{8MHz} = 3.00V$$

$$V_{O(n=10)} = V_{IN} \cdot n \cdot \frac{f_{SW}}{f_{CLK}} = 12V \cdot 10 \cdot \frac{250kHz}{8MHz} = 3.75V$$

The calculations show a 0.375V or 11.1% output voltage step in response to a duty cycle change of one clock period which is clearly not acceptable. A visual representation of the output voltage and discrete duty cycle values around the nominal output voltage is shown in Fig. 7.

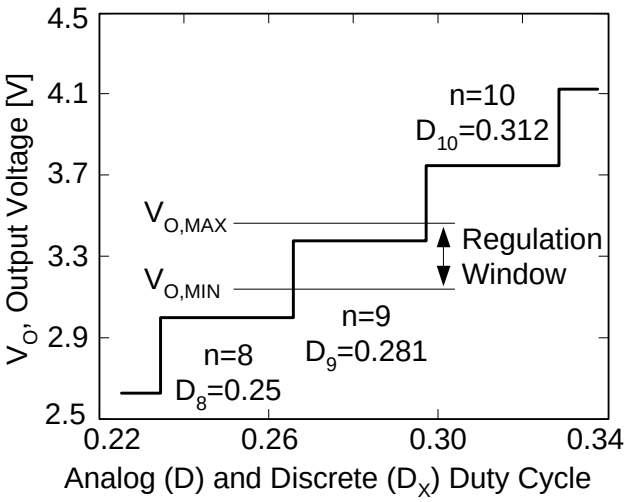


Fig. 7. Output voltage vs. duty ratio in digitally controlled power supply.

Another instance where discrete duty cycle values can be observed is the effect of input voltage change on the output voltage of the converter. Utilizing the infinite resolution of analog controllers, the output voltage is regulated practically at a constant level, independently from the input voltage. With only a finite number of duty ratios being available in digital control the output voltage can not be held at a constant value. Fig. 8 shows the example converter's output voltage as a function of V_{IN} around the nominal 12V value.

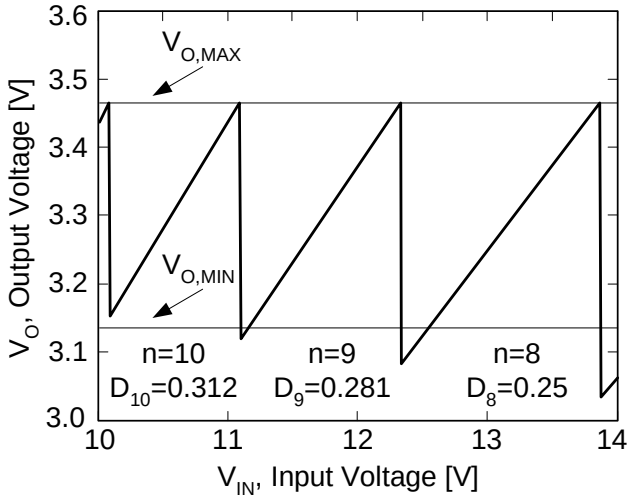


Fig. 8. Output voltage vs. input voltage in digitally controlled power supply.

Due to the finite number of possible duty ratios the converter's output voltage will be proportional to the input voltage until the operating conditions will demand the next smaller duty cycle. At that moment the output voltage suddenly drops to the new value corresponding to the new duty ratio as demonstrated in Fig. 8.

B. Digitizing Variables – Voltage Sense

In addition to the effects of discrete time steps the various control variables are also digitized in the digital controller. This introduces another level of complexity in the design. First of all it is important to note that the digital controller measures everything as a voltage input connected to an on-board analog-to-digital converter, usually through a multiplexer. All voltages monitored by the ADC must be scaled to the input voltage range of the ADC, generally between ground and the reference of the ADC. Typical reference levels are either 1.25V or 2.5V and these references can be internal or external to the analog-to-digital converter. After the conversion, the measured voltage level will be represented by a digital value as shown in Fig. 9.

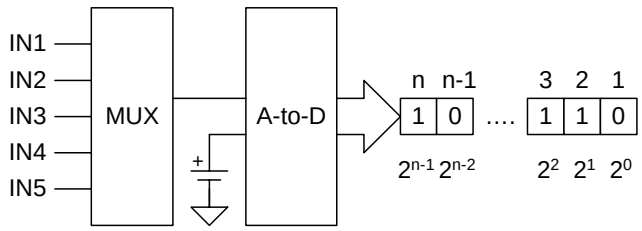


Fig. 9. Voltage measurement using ADC.

The analog-to-digital converter can be characterized by the number of bits of its output and by the time required to produce the result. The ADC's number of bits is directly related to the accuracy of the measurement because it defines the resolution. When the input signal to the ADC is equal to (or larger than) its reference voltage all output bits will be 1. From this relationship the resolution of the ADC can be calculated according to:

$$res_{ADC} = \frac{V_{REF}}{2^n}$$

where *n* is the number of bits of the analog-to-digital converter. That means that the input voltage range is divide into 2^n number of equal bands and the ADC "identifies" the band containing the amplitude of the input signal. In order to establish the resolution of the actual measurement the gain and accuracy of the external resistive divider needs to be taken into account as well. For instance, measuring the 3.3V output of the earlier introduced example using an 8-bit ADC with a 1.25V reference will require a 3:1 divider in front of the input of the analog-to-digital converter. Notice that the 1.25V should not be used as an equivalent of the 3.3V because potential over voltage conditions could not be sensed. The 3:1 divider will allow measurement of the output voltage in the 0V to 3.75V range. Now the resolution of the output voltage measurement can be established as:

$$res_{Vo} = \frac{V_{FS}}{2^n}$$

where V_{FS} is the full scale amplitude and *n* is the number of output bits of the ADC. In our example the output voltage resolution is:

$$res_{Vo} = \frac{3.75V}{2^8} = 14.6mV$$

This means that the converter's output voltage can change as much as 14.6mV before it will become evident at the output of the analog-to-digital converter and the duty cycle could be modified. The ambiguity introduced by the measurement resolution ultimately impacts the regulation accuracy in power supply applications. The worst case error can be calculated by the following expression:

$$E_{RES}(in\%) = \frac{V_{FS}}{2^n \cdot V_O} \cdot 100$$

Substituting the already familiar values from our example yields:

$$E_{RES}(in\%) = \frac{3.75V}{2^8 \cdot 3.3V} \cdot 100 = \pm 0.44\%$$

This inaccuracy is additional to the error introduced by the tolerance of the reference and the resistive divider which scales the output voltage level to the input range of the ADC.

Theoretically, using more bits in the analog-to-digital converter increases the resolution and consequently the measurement accuracy as shown in Table 3.

TABLE 3. ADC ACCURACY AS A FUNCTION OF BITS

ADC Number of bits	8	10	12	14	16
E_{RES} (in %)	0.444	0.111	0.028	0.007	0.002

Another property of the analog-to-digital converter which deserves attention is the time needed between the command initiating the measurement and when the result is available in the output register of the ADC. This period consists of two intervals, the actual time needed to convert the analog signal to a digital word plus the number of instructions used to process, store and read the result. Since most modern microcontrollers and DSPs can access the result in a single instruction cycle, the most important parameter is the conversion time. Usually the conversion time is given indirectly by specifying the number of conversions in a second. For example, 200ksps (kilo-samples-per-second) performance translates to 200,000 conversions in a second, i.e. 200kHz. That means that the conversion time is around 5µs. Since the ADC is an autonomous peripheral, the microcontroller or DSP can perform other tasks during the conversion.

The conversion time is important for two main reasons in power supply applications. The first problem is that the conversion time can be considered as a time delay. Its effect is similar to having a very slow comparator in an analog controller. There are plenty of functions in a power supply where this is acceptable like under voltage lockout, but it is certainly not adequate where quick response to a fast changing parameter is critical, such as for current protection or even for peak current mode control. In general, it can be said that digital controllers can not replicate the instantaneous reaction of the analog controllers due to the time lag of the ADC's conversion time.

The other aspect of the conversion time is related to the bandwidth of the control loop. The sample frequency, how often the output voltage can be measured, will be seriously impacted by the conversion time of the analog-to-digital converter. In an analog implementation the output voltage is sampled in every switching cycle. If similar performance is expected from the digital controller, the switching frequency must be equal or less than the maximum frequency which can be supported by the ADC. Even then it should be assumed that the output voltage is the only parameter the ADC is measuring which is clearly not the case in most power supply applications.

C. Digital Pulse Width Modulation

Now that some of the basic blocks and characteristics of a digital controller have been introduced, the operation of the analog and digital pulse width modulator can be compared. Fig. 10 illustrates the fundamental process to obtain the operating duty ratio of a power supply using an analog (top drawing) and a digital (bottom drawing) approach.

The analog control circuit requires a reference, an error amplifier and a comparator to determine the required duty cycle. As shown in Fig. 10, the output voltage is compared to a reference using a resistive divider at the inverting

input of the error amplifier. The control law is also implemented by the error amplifier by selecting the appropriate R and C values to set the poles and zeros of the differential equations governing the behavior of the negative feedback loop. The actual duty cycle is produced by a simple comparator by comparing the error voltage to an artificial ramp which also carries the information of the operating frequency of the circuit. The duty cycle generated this way can be any value allowing the analog controller to regulate the output voltage of the power supply exactly at the desired amplitude.

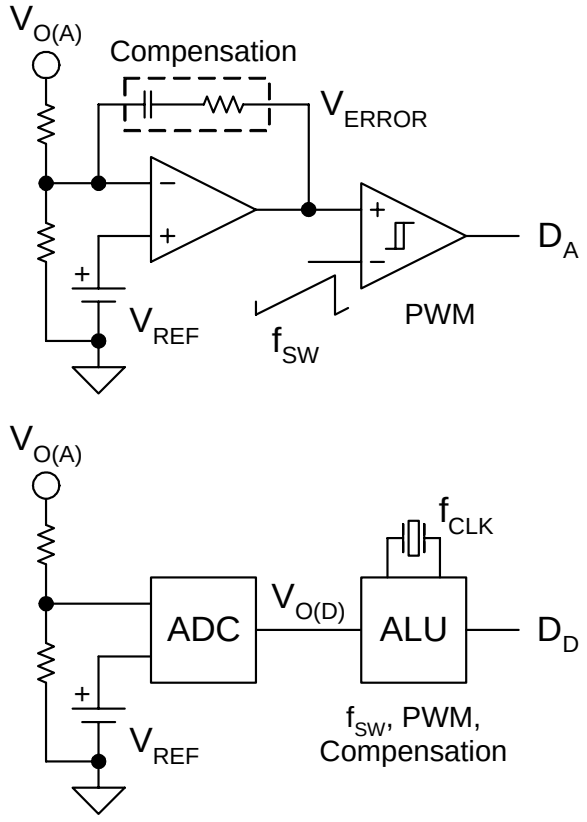


Fig. 10. Comparison of analog and digital PWM implementation.

The digital implementation of the pulse width modulator starts with a similar resistive divider which scales the output voltage to the input voltage range of the analog-to-digital converter.

As mentioned before, the input voltage of the ADC at nominal output voltage must be less than V_{REF} to accommodate output voltages above the nominal value during transient operation. The ADC then converts the output voltage to a representative digital word labeled as $V_{O(D)}$ in Fig. 10. The Arithmetic and Logic Unit (ALU), the digital core of the microcontroller or DSP takes care of the rest of the functions. It can establish the switching frequency from the clock frequency of the processor (f_{CLK}) and it will calculate a value for the power supply duty cycle (D_D). The digital representation of the nominal output voltage and some of the previously measured $V_{O(D)}$ values are stored in memory and available for a comparison to the most recent output voltage level produced by the ADC. The control law is also executed by the digital engine as programmed by the software.

Without going into digital control theory, the Z-domain control function of our example buck converter which implements the equivalent of two poles and two zeros for a typical type 3 compensation can be written in the following form:

$$G(Z) = \frac{K1 \cdot z^2 - K2 \cdot z + K3}{z^2 - K4 \cdot z + K5}$$

This equation closely resembles the usual S-domain transfer function of the power supply. The computations to execute this control law in the digital domain can be summarized by the next two equations where *n* refers to the present cycle, *n-1* and *n-2* are the values from the previous two calculations respectively. The first step is to calculate the error between the desired and measured output voltage:

$$E(n) = V_{O,NOM} - V_O(n)$$

Using the just calculated value of *E(n)* and its earlier values from the previous two cycles along with the respective duty cycle values (from the memory of the digital controller) the new duty cycle *D(n)* can be computed:

$$D(n) = a2 \cdot D(n-2) + a1 \cdot D(n-1) + b2 \cdot E(n-2) + b1 \cdot E(n-1) + b0 \cdot E(n)$$

The coefficients of the equation can be obtained by simple mathematical manipulations from the S-domain transfer function or synthesized directly from the component values of the power supply. These constants are stored in the memory of the digital controller and as such can be easily modified during debug or even while the power supply is running according to a specific mode of operation.

D. Limit Cycle Oscillation

To ensure stability with a digital controller, there are two fundamental requirements which must be satisfied. The first one is the traditional small signal stability criteria which is addressed by the appropriate selection of the various constants in the control law equations.

The second constraint involves the time domain resolution of the digital PWM engine and the voltage resolution of the analog-to-digital converter. This unique problem is demonstrated in Fig. 11.

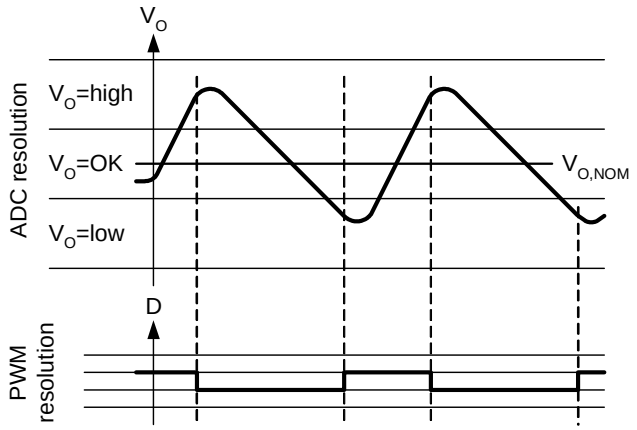


Fig. 11. Demonstration of limit cycle oscillation with digital control.

Assume that the power supply is running in steady state operation with a constant duty ratio producing an output voltage which is in the zero error bin (V_O=OK). When the operating conditions change – the input voltage increases or some of the load is removed – the output voltage starts to climb. Slight output voltage variation is allowed and will not change the duty cycle as long as V_O stays within the V_O=OK band because the analog-to-digital converter will produce the same result. As soon as the output goes higher than the upper threshold of the zero error bin, the ADC output will change which indicates that the output is too high. The digital controller mimics the reaction of any analog controller under the same circumstances and will try to compensate by decreasing the duty ratio. The minimum change in the duty ratio is a function of the clock period of the digital PWM engine. In Fig. 11 a situation is depicted where shortening the on-time of the main power switch by one clock period ($1/f_{CLK}$) results a new output voltage in the V_O=low band. This will initiate a correction asking for the next larger duty cycle value which will bring the output voltage back to the V_O=high band. And the cycle starts again, the output voltage will oscillate. The smoothing of the output voltage waveform in Fig. 11 is accomplished by the averaging L-C output filter of the power supply.

The obvious problem in this example is that the time domain resolution is too course with respect to the resolution of the analog-to-digital converter. This phenomenon is called limit cycle oscillation and it can happen regardless of whether the design meets all conventional stability criteria. The solution to this dilemma is to follow a design procedure where the ADC resolution is selected first, based on the required accuracy of the output voltage regulation. The duty cycle resolution is then adjusted to the ADC resolution by selecting an appropriate clock and switching frequency combination.

IV. Programmable Functions and Variables

The development of a suitable power supply controller is primarily driven by the answers for three fundamental questions:

- What functions to provide? (in addition to f_{SW}, and PWM)
- How to implement them?
- When to execute them?

With an analog approach, the first two questions are answered by selecting the PWM controller and some auxiliary components to match the intended features. Once the components are chosen and interconnected, the functions and the control algorithm are fixed and the circuit becomes dedicated to the particular application. Any change in functionality would require adding more components or redesigning

the interaction among the different sections of the controller. Finally, the voltage levels and limits are set according to the predefined or user adjustable thresholds and by fixed external components. This will define permanently when the functions will be carried out.

On the other hand, the hardware of the digital controller is designed almost independently of its functionality. Only the selection of the input parameters might impact the available functions and their implementation. Practically, all three questions are answered by the programming of the microcontroller or DSP. The software can integrate selected subroutines to address the necessary control functions. The control algorithm can be based on complex decisions evaluated by the digital controller and it can be easily modified by changing a few lines of code in the programming. The different thresholds and limits are also defined in the software as variables and their value can be modified easily. Through this mechanism, many operating parameters of the power supply can be customized without ever changing any component value in the circuit.

Accordingly, programmability and flexibility are the most significant differentiators in favor of the digital power supply controllers.

A. Miscellaneous Control Functions

With a powerful processor, the digital controller is capable of performing many more functions beyond the basic voltage regulation task. By measuring just a few more working parameters of the power supply, a host of intelligent control and protection functions can be implemented. Some of the data and variables which can be easily made available for the digital controller through its analog-to-digital converter or by values stored as variables in memory are:

- Input voltage
- Average input current
- Average output current
- Operating temperature
- Other output voltages in the system
- Host supervisor with serial bus communication capability
- DC Transfer function of the converter
- Variable examples:
  - V_{OUT}
  - V_{OVP}
  - $I_{OUT,MAX}$
  - $P_{OUT,MAX}$
  - $V_{IN,MIN}$
  - $V_{IN,MAX}$
  - $I_{IN,MAX}$
  - $I_{PK,MAX}$
  - f_{SW}
  - D_{MAX}
  - $V{\cdot}s_{\,MAX}$
  - D_{MIN}
  - t_{SS} (soft-start time)

A partial inventory of the possible functions using these additional measurements and variables is summarized in the following list:

- Switching frequency modulation
- Input voltage monitoring (UVLO, line OVP)
- Shutdown, Enable
- Soft-start profile
- Sequencing – sync. rectifier control
- D_{MAX} limit
- Volt-second clamp
- Green mode operation (burst mode, D_{MIN} limit)
- Transient overload response
- Current limit profile
- Output characteristic (droop, constant power)
- Temperature protection (derating, shutdown)
- Communication

Since these functions would be implemented in software, the behavior of the system could be tailored to specific applications rather easily. That's where the flexibility of the digital controller would be the most valuable in contrast to the hard wired responses of analog controllers.

Switching Frequency Modulation

Because the operating frequency is defined by the digital controller, it can be managed through software. There are several applications where variable frequency operation can be beneficial. Off-line power supplies can take advantage of *spreading EMI noise spectrum* by slowly modulating the switching frequency of the converter in a relatively narrow band around the nominal operating frequency. This could reduce input EMI filter requirements, offer smaller size and lower cost. Another application where this

opportunity might be welcomed is to meet *green mode* power consumption limit in standby. In most green mode implementations high efficiency, low power standby mode is facilitated by reduced switching frequency or by burst mode operation, both achievable by controlling the switching frequency using the digital controller's software routines.

Input Voltage Monitoring

Knowing the input voltage of the converter allows the digital controller to accomplish some additional control functions. The most basic ones are line *under voltage lock out* (UVLO) and line *over voltage protection* (OVP). To realize these functions, the valid input voltage range of the converter is stored in the digital controller's memory and the measurement is compared to those limits. When the input voltage is outside of the operating range, the power stage is disabled and all other operations of the controller can be suspended. This technique allows low power operation of the microcontroller or DSP because its clock frequency can be significantly reduced. It is also possible for the microcontroller to enter standby mode between measurements since all other tasks are put on hold until the input voltage returns to the nominal range.

Some of the more sophisticated functions based on the actual input voltage level could be *brown out protection* when the converter's input power is limited during brown out conditions.

Another option is to implement an advanced *volt-second clamp* to protect the transformer from saturation in isolated topologies. When volt-second clamping is employed in analog controllers, designers often face the trade off between fast transient response and effective protection due to the duty cycle limiting effect of the volt-second clamp. The ultimate flexibility of the digital control algorithm could help to overcome this trade-off according to the flow chart shown in Fig. 12.

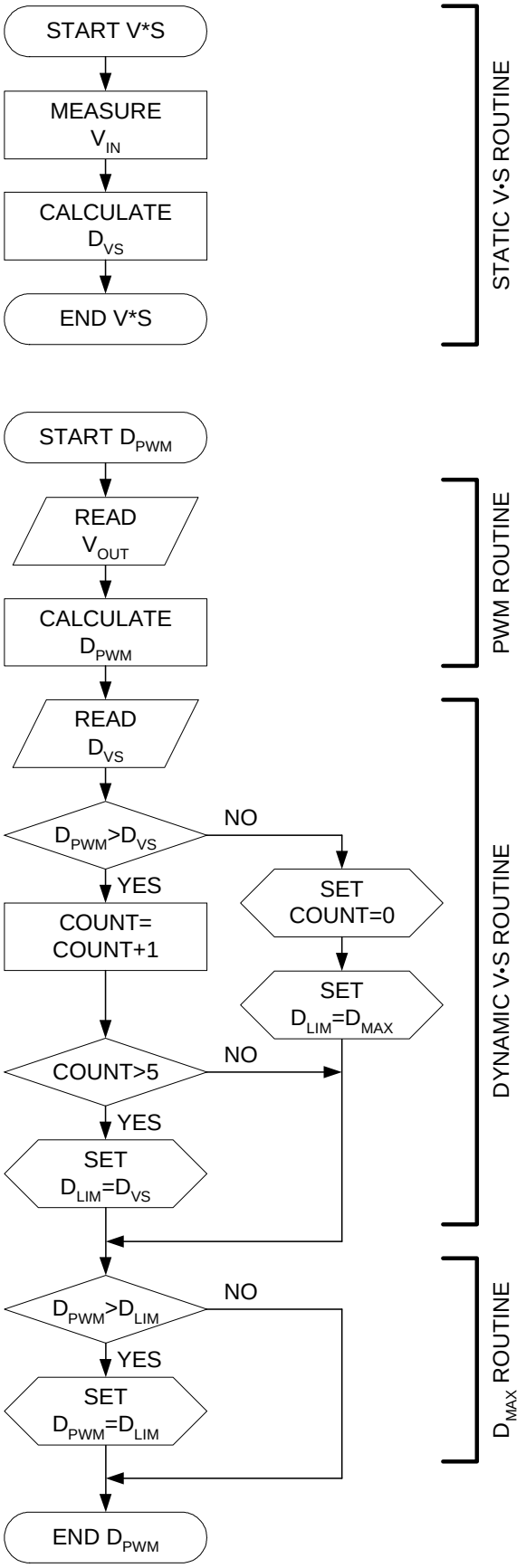


Fig. 12. Advanced volt-second clamp routine.

Isolated converters frequently adhere to a maximum duty cycle limit (D_{MAX}) especially if they employ a single ended topology. D_{MAX} is usually set during the power stage design and corresponds to operation at minimum input voltage. At that point $D_{MAX}=D_{VS}$, the volt-second duty ratio limit, calculated as a function of the input voltage. At higher input voltages the volt-second limit reduces the maximum operating duty cycle according to:

$$D_{VS} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{N_P}{N_S} \cdot 1.2$$

In this equation the volt-second clamp is set 20% above the nominal duty ratio of the converter as indicated by the 1.2 multiplier. The lower of D_{MAX} or D_{VS} limits the actual duty ratio calculated by the controller based on the output voltage error (D_{PWM}). In normal, steady state operation none of these limits impact the operation of the power supply.

The software routine illustrated in Fig. 12 would allow the converter to operate beyond the volt-second limit for 5 cycles to accommodate fast transient response before cutting back the allowable maximum duty ratio to protect the converter. During the five transient cycles this example uses D_{MAX} to limit the maximum operating duty ratio but the software could be easily modified to provide more protection if needed.

Since the input voltage change is relatively slow, it will not be sampled in every switching period to save computing resources. Therefore, the static volt-second routine is independent from the PWM calculation as shown in Fig. 12 and once it is executed, its result can be used until the next calculation is completed.

Current Sense

The digital controller can also measure the input, output or both currents of the power supply. The collected current information can be utilized to implement various types of current limiting methods or can be combined with other parameters to customize the power supply's output characteristic under overload conditions.

The most frequently used current limit techniques include:

- Constant output current
- Foldback
- Transient ride through (delayed shutdown)
- Hiccup (shut down & retry)
- Shutdown (permanent lock out)

When foldback current limit is required, the output current must be measured and controlled as a function of the output voltage. The digital controller could implement the following relationship:

$$I_O(V_O) = I_{MIN} + R_{LOAD(MIN)} \cdot V_O$$

In addition, the maximum output current can be limited as well by comparing the result of the above equation to an absolute limit stored in the parameter table in memory.

Transient current limit of the converter could be established in software by a simple routine similar to the one used for the dynamic override of the volt-second clamp (Fig. 12). Hiccup and shutdown type current limit actions are even simpler and lend themselves for easy execution in digital control. What will differentiate the digital implementation from traditional analog circuits is the possibility to effortlessly adjust the current limit threshold either through the programming interface (communication) or as a function of operating parameters like temperature. Furthermore, it is conceivable that the controller could switch between the different over current protection methods based on a pre-programmed algorithm during operation. One example for changing between different current limit methods is the incorporation of *constant output power characteristic*. Frequently done even with analog controllers in telecom rectifiers, in the nominal range (for instance, between 43V and 58V output) the current limit is a function of the output voltage to utilize the maximum power throughput of the converter. At low output voltages, power limiting would cause excessive current stress, thus the control changes to limit the current at a safe maximum value (constant output current characteristic).

Soft-Start Operation

The two most common soft-start methods used in integrated analog PWM controllers are shown in Fig. 13. These techniques are called open loop soft-start because the voltage regulation loop is open during the soft-start time interval. That also means that control must be asserted by some other means instead of the voltage error amplifier. In both examples the controlling variable is the voltage across the soft-start capacitor, C_{SS}.

The top drawing depicts a voltage mode implementation since the control quantity is compared to a sawtooth waveform derived from the oscillator. As the voltage across C_{SS} slowly ramps up, the operating duty cycle of the converter increases until the nominal value is reached. At that time the voltage regulation loop becomes operational and takes over the duty cycle control. According to the voltage mode operation just described, during soft-start the converter's duty ratio is a simple function of the capacitor voltage which linearly increases with time. In other words the task at hand is to increase the duty ratio from zero to D_{NOM} during the time defined by the value of the soft-start capacitor.

This could not be easier to implement in a digital controller. The soft-start time can be given and the software can impose a gradually increasing maximum duty cycle limit on the PWM output to emulate the operation of the analog circuit.

In the current mode implementation, as shown in the lower part of Fig. 13, the soft-start capacitor voltage controls the maximum current of the main power switch. The PWM comparator matches up the current sense voltage to the linearly increasing C_{SS} voltage. Similar to the voltage mode operation, during soft-start the voltage loop is open. This algorithm implements soft-start by increasing the peak current limit from zero to full current capability during the time interval defined by the value of C_{SS}.

Again, this behavior can be replicated simply by ramping up the current limit threshold according to the required soft-start time stored in the program of the digital controller.

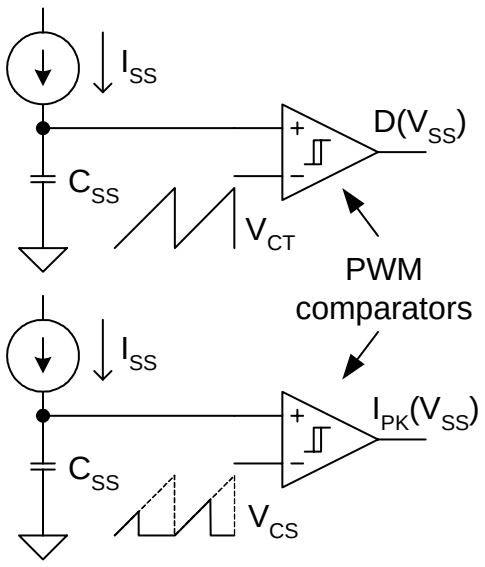


Fig. 13. Typical soft-start circuits in analog PWM controllers.

Temperature Monitoring

Several microcontrollers and DSPs are equipped with on-board temperature sense elements or can measure temperature using an external sensor. As implied in the current sense section, the temperature information can be combined with an adjustable current limit threshold to provide protection against temperature related damage of the power supply. In addition to *derating* the output power of the converter, *over-temperature shutdown* with programmable threshold is also possible.

Presence of a Higher Intelligence

The controller of a power supply is just as good as the algorithm it implements, regardless of whether it is analog or digital. In an analog controller the algorithm gets embedded in the hardware during the circuit development. Digital power supply control replaces a lot of hard wired responses with intelligent software based decisions which supervises the operation of the power supply. One of the cornerstones of establishing intelligence is *communication* which is natural to digital controllers.

The first instance of communication is in the programming, when the knowledge of the power supply designer gets "downloaded" into the microcontroller or DSP. But communication can be maintained and utilized during the entire lifetime of the power supply. The digital controller can provide the interface between the converter and the external world. Established, industry standard protocols make it easy to connect to other equipments. Most microcontrollers and DSPs offer one or more serial communication bus protocols implemented either in hardware or through software programming. Some of the potential suitable standard buses and their basic characteristics for power supply applications are:

- I^2C – Inter-Integrated Circuit
  - 2 wire, bi-directional bus
  - 100kb/s, 400kb/s, 3.4Mb/s selectable speed
  - device addressable bus
- SMBus – System Management Bus
  - I2C like bus (2 wire, bi-directional)
  - speed is between 10kb/s and 100kb/s
  - limited device addressing
- SPI – Serial Peripheral Interface
  - 3 wire bus plus chip select (Enable)
  - 1Mb/s, 10Mb/s speed
  - Master – slave arrangement
- Microwire
  - version of SPI
  - variable length bit stream
- CAN – Controller Area Network
  - 2 wire, differential bus
  - up to 1Mb/s speed

Once the communication is established the power supply can talk and listen to the host computer of the larger system or it can accept commands from a human operator through a small touch pad. This new opportunity makes remote control and adjustments of the operating parameters and limits feasible. Furthermore the digital controller can store and provide data about the operation of the unit for diagnostic purposes. Monitoring long term trends in the operating parameters can be a very useful tool to predict pending failures of the power supply and to avoid down time of the system.

V. HARDWARE EXAMPLE

The most computation intensive tasks for the digital controller are clearly the output voltage regulation and implementation of digital pulse width modulation. Also, these are the most difficult, new theoretical areas of digital control for the practicing power supply designer. But before facing the first endeavors with Z-transformations, resolution issues and speed, digital control can provide tremendous benefits for power supplies as shown in the next circuit example.

A. Digitally Assisted Power Supply

This circuit demonstrates an approach which can provide a bridge between pure analog and fully digital power supply control. The converter's specification is detailed next.

V_{IN} = 36 V to 75 V
$V_{IN,TURN-ON}$ = 33 V
$V_{IN,TURN-OFF}$ = 30 V
V_{OUT} = 12 V
P_{OUT} = 100 W
$I_{OUT,MAX}$ = 8.3 A
$T_{AMB,MAX}$ = 55°C
f_{SW} = 500 kHz
Isolation: 500 V
Communication:

- JTAG – for programming
- RS-232 (UART) – monitoring, adjustments

Microcontroller: MSP430F1232
PWM controller: UCD8509
Form Factor: ¼ Brick
Topology: Resonant Reset Forward

B. Circuit Descriptions

The forward converter is an isolated topology and utilizes a simple two-winding transformer to transfer power across the isolation boundary. Like in all forward based converters, the transformer operates in the first quadrant of the core's magnetization curve. Accordingly, the transformer core must be reset to its initial demagnetized state before the next clock period starts. In this converter the reset action is provided by the resonance between the magnetizing inductance of the transformer and the node capacitance where the primary winding connects to the drain of the switching power

transistor. Since the focus of this paper is to gain familiarity with digital control, the detailed power stage design is omitted. For completeness the schematic is provided in Fig. 14.

The typical building blocks of the power stage are easily recognizable in the schematic. In line with industry standard design practices the converter has minimum on-board input capacitance, only 4uF for high frequency bypassing. The quarter brick requires additional energy storage capacitors on the system board located close to the input terminals of the module.

The power transformer is a planar magnetic structure, manufactured by Payton Inc. The primary number of turns is 7 and the secondary is 5 turns. There is a third auxiliary transformer winding which also has 5 turns and it is referenced to the primary side of the power supply. It is used for the bootstrap bias supply.

When the converter is switching, the power consumption of the controller and gate drive circuit exceeds the current capability of the high voltage bias circuitry which draws power directly from the input terminal during start up. The bootstrap bias supply provides an efficient way to power the primary side control circuit while the converter is running. Since the input voltage can vary over a two to one range, the bootstrap supply uses an averaging L-C filter to generate a quasi regulated 12V rail.

The forward converter utilizes the SUM65N20-30, 200V, 30mΩ MOSFET from Vishay as the main switching transistor. Its current is measured by a 50:1 current sense transformer which is terminated by a 3Ω current sense resistor and fed to the controller through a low pass filter.

Due to the 12V output and its simplicity, rectification is implemented by two Schottky diodes on the secondary side of the transformer. Both diodes are equipped with a small R-C snubber to reduce the ringing on the switching waveforms.

The averaging output filter is designed for approximately 12A as opposed to the specified 8.3A maximum to allow experimenting with different current limit strategies. The output inductor value is 10µH. There are three output capacitors in parallel, an 83µF polarized energy storage capacitor and two high frequency filter components, 1µF and 0.1µF.

The schematic in Fig. 14 also indicates the different signal connections to the control circuit which is shown in Fig. 15.

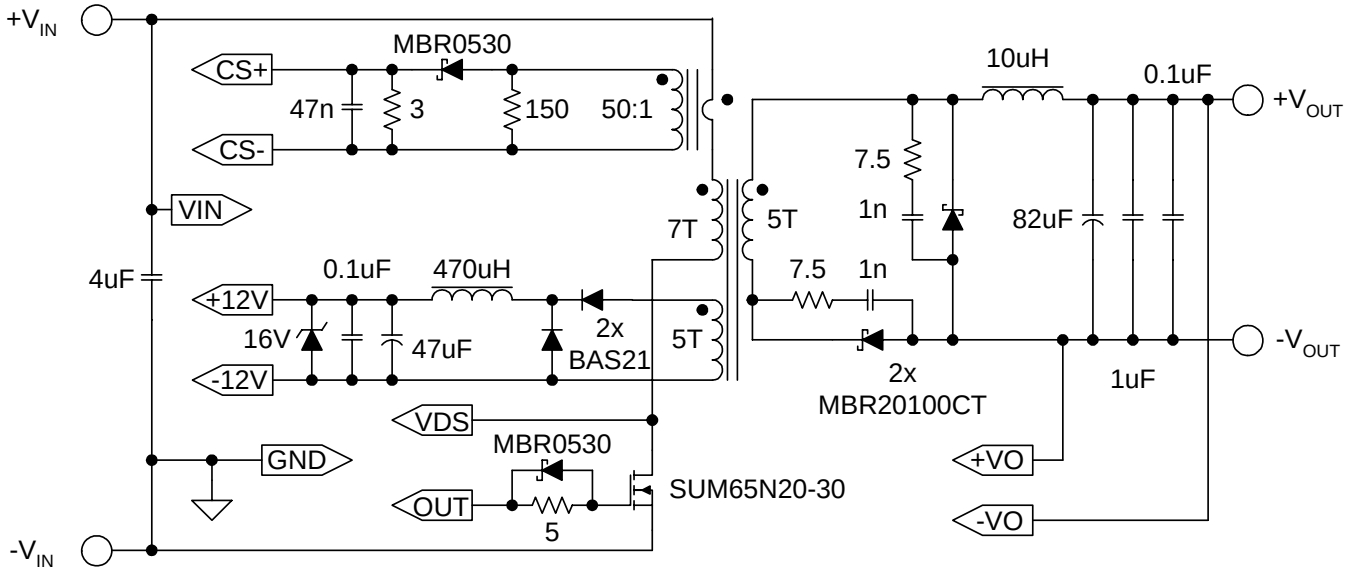


Fig. 14. 100-W resonant reset forward power stage.

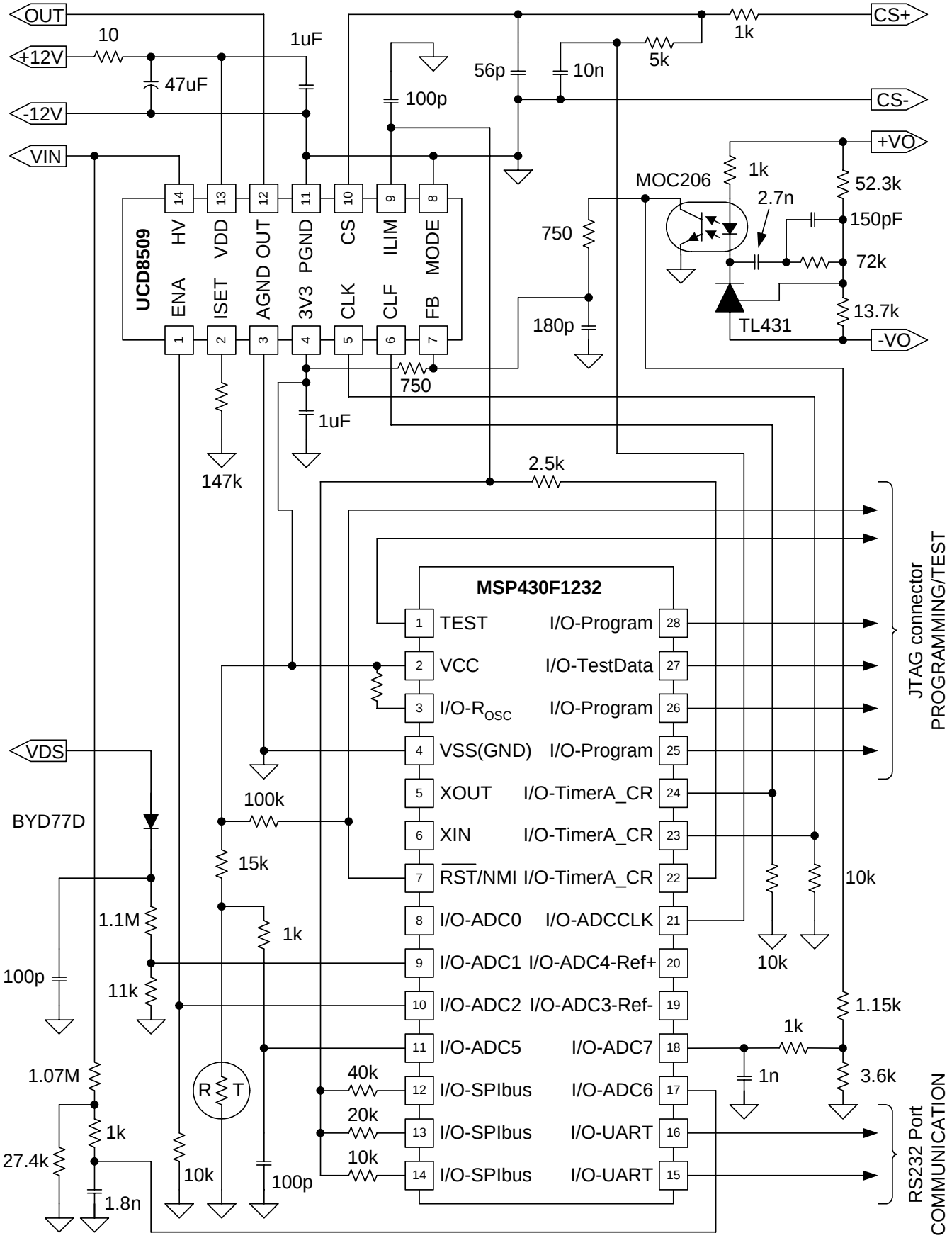


Fig. 15. Digitally assisted power supply controller of the forward converter.

The controller operates with a fixed, 500kHz switching frequency and implements current mode control using the primary switch current information. The primary side control circuit is comprised of two ICs representing the demarcation between analog and digital control functions. The digital portion of the control algorithm is implemented in the MSP430F1232. The microcontroller is connected to the power stage and powered through the UCD8509 type analog controller which was specifically developed for digital power supply control applications in single ended converters. The regulation of the power supply's isolated output is performed by the opto isolated error amplifier section based on the popular TL431 integrated circuit.

C. Functional Description

The division between analog and digital control functions is based on the capabilities of the selected processor and the amount of computational resources needed to perform the control functions. In general, the more high speed control functions are moved to the digital domain, a higher performance, more expensive microcontroller or DSP is needed to execute the control algorithm. The most difficult functions for the digital controller are the voltage regulation loop, the digital pulse width modulation, the implementation of peak current mode control with slope compensation or input voltage feed forward in voltage mode control and over current protection. These functions correspond to fast changing signals which have to be measured and recalculated on the switching frequency basis or require immediate action to protect the power supply. The utilization of a dedicated analog building block can remove the burden of these computation intensive tasks from the processor and allow using a cost effective microcontroller. In addition, using analog circuits for the basic high speed power supply functions also permits the use of familiar analog control principles to ensure the stability of the power supply. The development of an analog controller also presents the opportunity to optimize the partitioning and the signal interface between the digital and analog portions of the controller.

Analog Functions – UCD8509

The UCD8509 is a highly integrated analog companion chip to a microcontroller to implement digitally assisted power supply control. Its primary purpose is to provide high speed, analog pulse width modulation and secure over current protection. It also includes all auxiliary housekeeping function to service the microcontroller and a specialized interface to effectively communicate using only a few digital signals. The simplified block diagram is illustrated in Fig. 16.

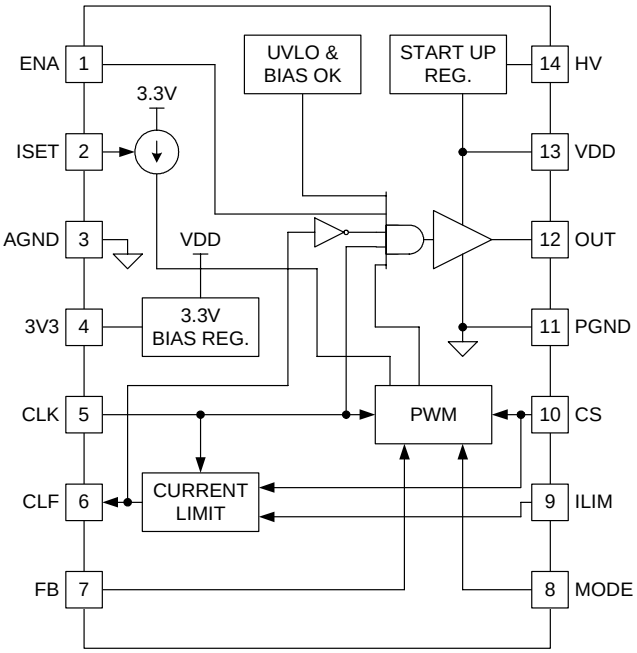


Fig. 16. UCD8509 simplified block diagram.

In telecom or similar input voltage applications, an on-board start up regulator provides initial bias to the chip which can be connected directly to the input power source. The start up regulator's maximum input voltage is 110V. Once the power supply is up and running, the start up regulator turns off and the auxiliary power must be provided by a bootstrap power supply as shown in the schematic diagram in Fig. 14. The bootstrap voltage must be between 8V and 15V which is the recommended operating voltage range of the UCD8509.

The on-board 3.3V regulator draws power from the VDD rail and provides bias to the IC's internal circuits and to the microcontroller. The maximum external current consumption must be kept below 10mA, thus using a low power microcontroller is desirable.

The UCD8509 includes a high current output to drive the gate of an external power MOSFET. The gate driver switches between ground and the actual VDD voltage and has approximately 4A sink and 2.5A source current capability.

The controller also accommodates a high speed analog PWM section which can be set up for voltage or peak current mode operation according to the MODE input. The operating mode can be selected by shorting the pin to ground or to 3.3V, or by the microcontroller driving the MODE pin directly. While the UCD8509 has no oscillator, an internal local ramp generator is employed for the pulse width modulation in voltage mode. The same ramp generator is used to provide slope compensation in current mode. The slope of the ramp is adjusted by an external resistor connected to the ISET pin. The converter's operating duty cycle is controlled by the error voltage which has to be connected to the FB pin.

One of the most important features of the UCD8509 is to provide instantaneous and autonomous over current protection for the power stage without any help from the microcontroller. This function is implemented in the current limit block. For autonomous operation the UCD8509 has a default, internally set 0.5V current limit threshold which can be overridden by the microcontroller or by an external resistor network through the ILIM terminal. For added protection, the current limit adjustment range is internally limited between ground and twice the default value, i.e. between 0V and 1V. In case the cycle by cycle current limit circuit is activated, the UCD8509 will set the current limit flag (CLF) output high which can be read by the digital controller. The flag is automatically cleared before the beginning of the next switching period making it easy for the microcontroller to count the number of switching periods terminated by the current limit circuit.

The operating principle of the UCD8509 and the interaction between the microcontroller and the analog PWM block can be explained using the timing diagram in Fig. 17.

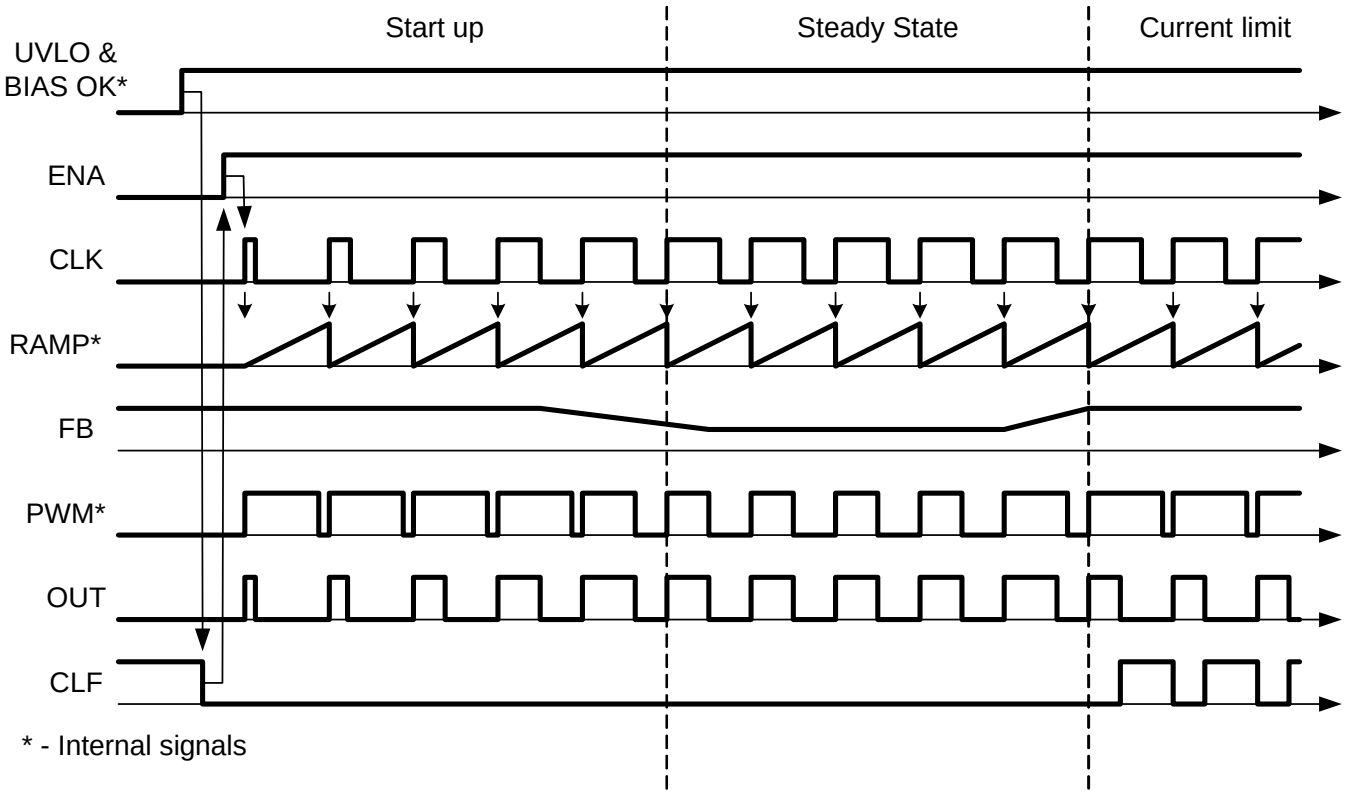


Fig. 17. UCD8509 timing diagram (voltage mode operation).

During initial start up the UCD8509 establishes its own bias voltage (VDD) and the 3.3V bias for the microcontroller. During this time the CLF output is high, indicating for the digital circuit that the analog functions are not yet available. When all internal voltages are at their nominal level the CLF signal is cleared and the operation can commence. At that time the microcontroller is expected to enable the operation by setting the enable signal high and start sending the CLK pulse train.

The CLK signal carries two important pieces of information to supervise the operation of the UCD8509. As shown in Fig. 17, coinciding with the rising edge of CLK signal the pulse width modulator is reset and the gate drive output turns on indicating the beginning of the next switching period. Thus the switching frequency is determined by the rising edge of the waveform. The width of the CLK pulse limits the maximum on-time of the gate drive output. In fact, the duty ratio of the CLK signal is used as a variable maximum duty cycle clamp. According to the functions programmed in the microcontroller, the width of the CLK pulse is continuously recalculated by the digital controller and can be used to implement several control functions. Fig. 17 exemplifies how to use the CLK pulse width to implement soft-start.

During normal operation the converter's duty ratio is less than the limit imposed by the digital controller, hence it is determined strictly by the analog PWM circuit of the UCD8509. Therefore the time domain resolution of the microcontroller is not a concern anymore. Assuming that the voltage regulation loop is also analog, as it is the case in the example power supply in Fig. 14 and 15, the small signal stability of the power supply can be ensured by obeying the familiar analog rules.

In current limit, the UCD8509's cycle-by-cycle current limit comparator overrides both duty cycle values – the pulse width of the CLK input and the duty cycle of the analog pulse width modulator. The gate drive pulse terminates when the switch current reaches the current limit threshold. The threshold can be the default value or the adjusted voltage present at the ILIM pin. When the current limit circuit is activated the CLF signal goes high for the remainder of the switching period and the information can be managed by the microcontroller according to its software.

An important feature of the current limit block is its complete independence from the signals of the digital controller. The current limit event is latched and kept in the memory of the UCD8509 until the next switching period is initiated by the microcontroller. This technique can protect the power stage in case the digital controller stalls. The CLK input can freeze in either state, the current limit circuit will protect the power stage and keep the power switch off until the pulse train is restored and the next rising edge of the CLK signal resets the current limit circuit.

Software Functionality

Since the UCD8509's control functionality is limited to pulse width modulation, peak current limiting and start up bias generation, all other control functions on the primary side of the power supply must be executed by the digital controller. Accordingly, the MSP430F1232 controls the following functions in the demonstration power supply:

- Operating frequency
- Input line UVLO
- Input line OVP
- Absolute duty cycle limit – D_{MAX}
- Volt-second clamp – $D_{LIM}(V_{IN})$
- Soft-start – $D_{LIM}(t_{SS})$
- Current limit threshold adjustment
- Current limit profile (delayed shutdown based on the number of allowable events)
- Temperature shutdown
- MOSFET over voltage protection

In order to perform these functions the microcontroller needs to know the following variables:

- f_{CLK} – its own clock frequency
- f_{SW} – switching frequency
- $V_{IN,ON}$ – turn-on input voltage thresholds
- $V_{IN,OFF}$ – turn-off input voltage thresholds
- D_{MAX} – maximum allowable duty ratio based on the reset requirements of the transformer
- DC transfer function – to calculate appropriate volt-second limit

- t_{SS} – duration of the soft-start interval
- T_{MAX} – maximum board temperature
- $V_{DS,MAX}$ – highest acceptable drain-source voltage

These numbers can be entered through the graphical user interface of the demonstration software and will be incorporated in the executable code of the microcontroller. The screen shot of the demonstration software's user interface is pictured in Fig. 18.

In addition to the values entered by the user, the digital controller must measure and handle four more inputs:

- V_{IN} – input line voltage
- V_{DS} – drain to source voltage
- T_{BOARD} – board temperature
- CLF – current limit flag

The demonstration hardware measures two additional parameters for future expansion of the software functionality. These are V_{FB} and $I_{IN,AVE}$, the feedback voltage and the average input current, respectively.

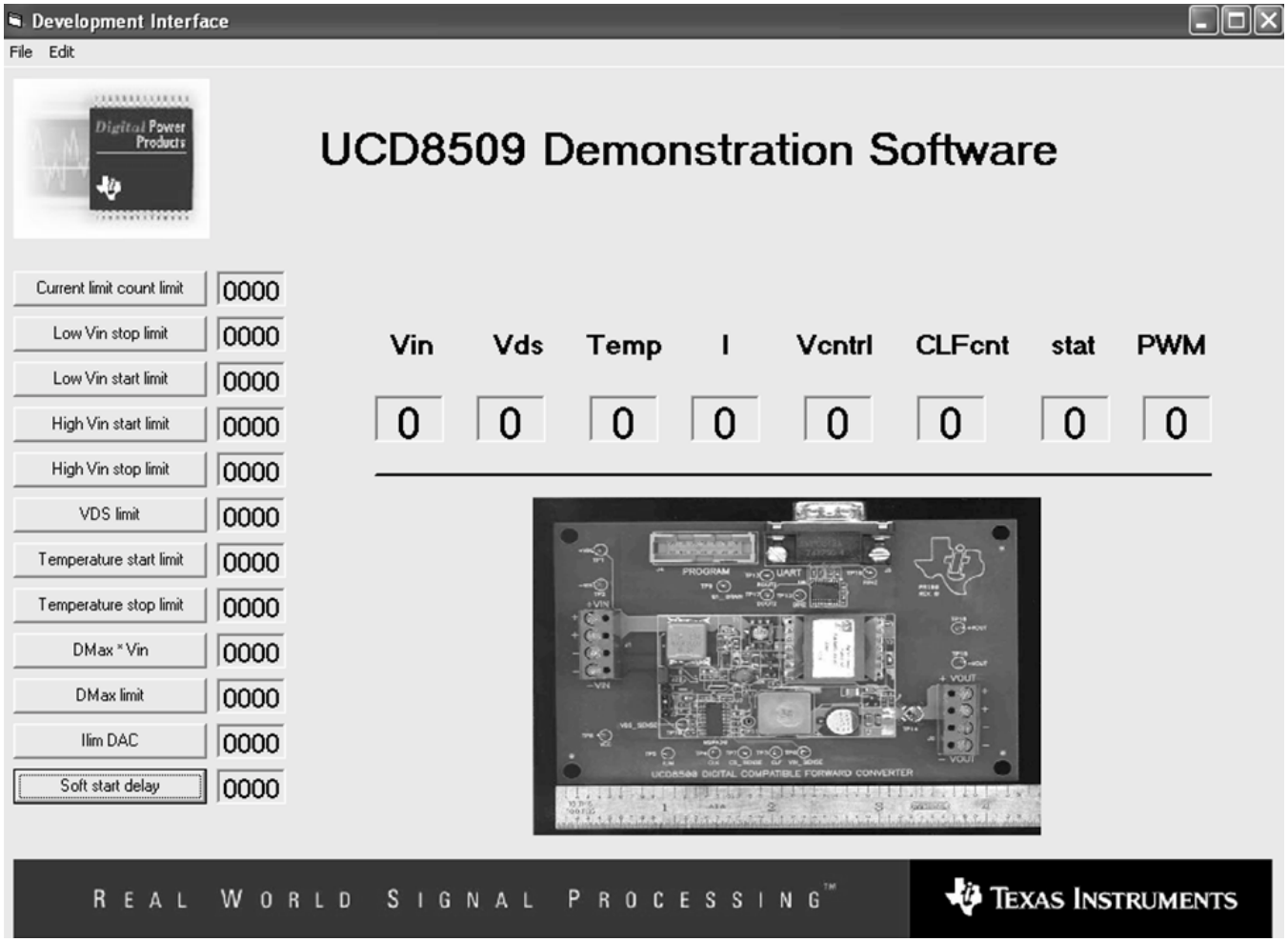


Fig. 18. Graphical user interface of the demonstration software.

Setting the Operating frequency

The MSP430F1232 is set up with a core clock frequency of 8MHz which frequency corresponds to the execution of the program instructions. The microcontroller can be tricked to operate its PWM timer at twice the clock frequency, which opportunity was utilized in this design. Based on f_{CLK}=16MHz and f_{SW}=500kHz, the switching period consists of:

$$n = \frac{16 \cdot 10^6\,Hz}{500 \cdot 10^3\,Hz} = 32$$

clock cycle of the PWM timer. Accordingly, the minimum duty cycle adjustment can be calculated as:

$$\Delta t = \frac{1}{16 \cdot 10^6\,Hz} = 62.5ns$$

or the duty cycle resolution is given as:

$$\Delta D = 500 \cdot 10^3\,Hz \cdot 62.5ns = 0.03125$$

Because the pulse width modulation is still done in analog by the UCD8509, the microcontroller's resolution impacts only the accuracy of the maximum duty ratio and the volt-second limit. For these functions the achieved resolution is sufficient.

Since the core of the microcontroller runs only with an 8 MHz clock frequency, every switching period contains 16 instruction cycles for program execution.

Maximum Duty Cycle

The power stage design allows a maximum operating duty ratio of approximately 80% to accommodate the reset time of the transformer. To provide some margin the controller is set up to limit the duty ratio at 75% or 24 clock cycles of the PWM timer (32·0.75=24).

Input Voltage Measurement

Knowing the actual input voltage value allows the digital controller to perform several housekeeping and protection functions. In this design the input voltage is measured by the on-board analog-to-digital converter. Since the ADC input is limited to the 0V – 2.5V range by the reference of the analog-to-digital converter, the anticipated input voltage range must be scaled down to meet this constraint. Assuming 100V maximum input voltage transient, the gain of the resistive divider can be calculated as:

$$G_{INPUT} = \frac{2.5V}{100V} = 0.025$$

This factor is implemented by the 1.07MΩ and 27.4kΩ resistors which are connected to the ADC6 input of the MSP430F1232 through an additional noise filter as shown in Fig. 15, the schematic diagram of the controller.

The ADC of the MSP430F1232 is a 10-bit analog-to-digital converter, therefore the 100V full scale input voltage range is represented by 2^{10}=1,024 individual values and the measurement resolution is:

$$res_{INPUT} = \frac{100V}{2^{10}} \cong 98mV$$

As this number indicates it is really easy to accurately adjust the turn-on or turn-off input voltage levels of the power supply. The demonstration circuit uses the result of the input voltage measurement to provide software programmable line under and over voltage protection with user adjustable hysteresis and to implement an input voltage dependent duty ratio limit, also known as volt-second clamp. The V·s clamp is based on the DC transfer function of the power stage and can be calculated as:

$$D_{LIM}(V_{IN}) = \frac{V_{OUT}}{V_{IN}} \cdot \frac{N_P}{N_S} \cdot 1.2 \cong 18.5 \cdot \frac{1}{V_{IN}}$$

where N_P and N_S are the primary and secondary number of turns of the transformer and the 1.1 multiplier indicates that the volt-second clamp is set 10% higher than the operating duty ratio of the converter. The working of the volt-second routine is demonstrated in Fig. 19 through 21.

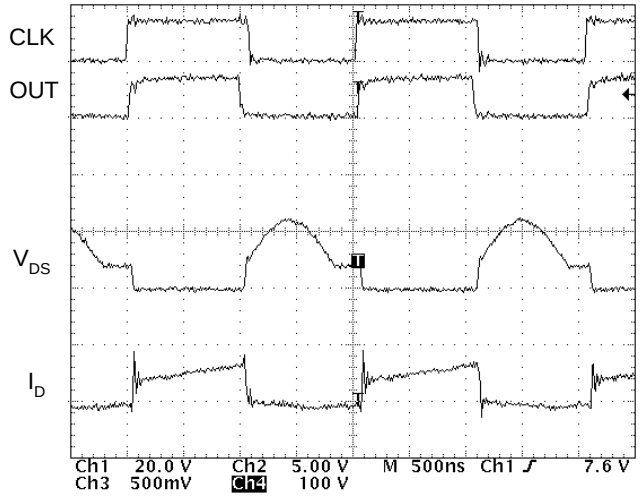


Fig. 19. Operating waveforms at V_{IN} = 36 V.

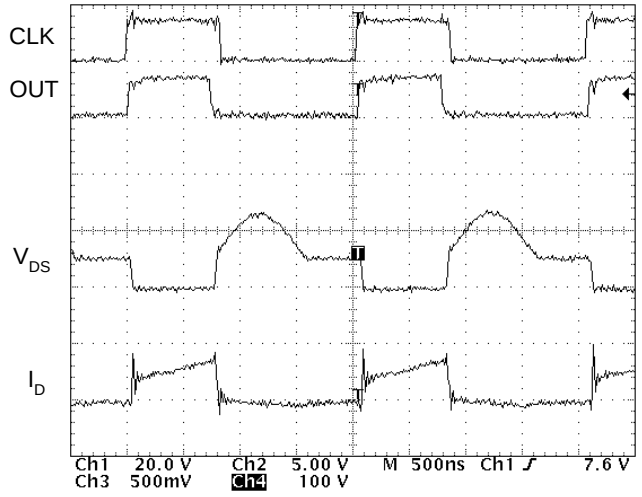


Fig. 20. Operating waveforms at V_{IN} = 48 V.

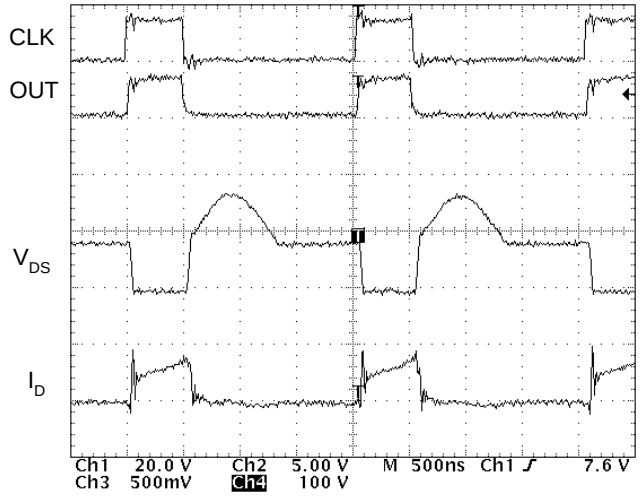


Fig. 21. Operating waveforms at V_{IN} = 76 V.

The converter's steady state operating duty ratio can be deciphered from the V_{DS} waveform of the switching transistor. The maximum allowable duty ratio ($D_{LIM}(V_{IN})$) is calculated by the microcontroller and it is based on the actual input voltage level. Its value is represented by the duty ratio of the CLK waveform. As the three figures demonstrate, the duty ratio of the CLK signal is approximately 10% higher than the operating duty cycle of the converter at all three input voltages.

Soft-Start

The soft-start time of the converter can be programmed through the software and will be implemented by the digital controller by gradually increasing the duty ratio of the converter. It is the same method outlined earlier in the Soft-Start Operation section under *Miscellaneous Control Functions*. The practical implementation starts by calculating the number of duty cycle values between zero duty cycle and D_{MAX}.

$$SS_{STEPS} = \frac{f_{CLK}}{f_{SW}} \cdot D_{MAX} = \frac{16 \cdot 10^6\, Hz}{500 \cdot 10^3\, Hz} \cdot 0.75 = 24$$

If the duty cycle limit would be increased by one step in every switching period the converter would reach maximum duty cycle in 24 switching period or in 60us. This is an unusually fast start up and it is also questionable whether the output capacitor can be charged to the nominal level within this time interval. To achieve a reasonable soft-start time in the milliseconds range, each of the 24 duty cycle values between zero and D_{MAX} has to be maintained for several switching periods. For instance, if the soft-start time is given as t_{SS}=5ms, each duty ratio must be valid for n_{SS} number of switching cycles which can be obtained as:

$$n_{SS} = \frac{f_{SW}}{SS_{STEPS}} \cdot t_{SS} = \frac{500 \cdot 10^3\, Hz}{24} \cdot 0.005 \cong 104$$

The effect of the gradually increasing discrete duty cycle values is demonstrated in Fig. 22. In order to show the step function in the output voltage waveform the soft-start time had to be extended to approximately 8 seconds.

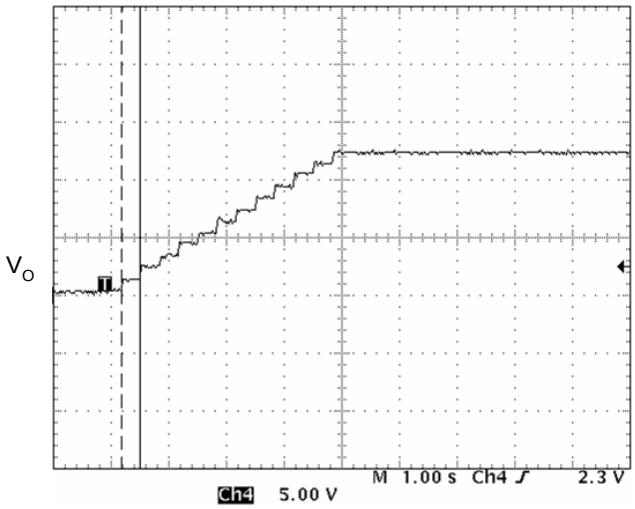


Fig. 22. Output voltage waveform with artificially long soft-start time.

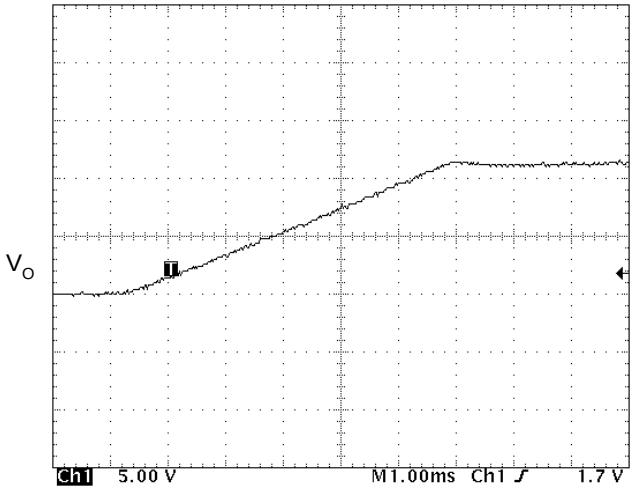


Fig. 23. Output voltage ramp up with 5ms soft-start time.

The normal 5ms long soft-start waveform of the converter is shown in Fig. 23 and it demonstrates the usual monotonic ramp up of the converter's output voltage.

Current Limit Operation

Using the capabilities of the UCD 8509, the digital controller is able to adjust the current limit threshold and also the overload behavior of the power supply.

To override the default 0.5V current limit threshold of the analog current limit circuit, its ILIM pin voltage needs to be overridden. For current limit adjustment the UCD8509 expects an analog voltage at the ILIM terminal which can be generated by the microcontroller. Since the MSP430F1232 has no digital-to-analog converter on-board, the function is implemented by four of its digital I/O ports and an external resistor network as shown in Fig. 24.

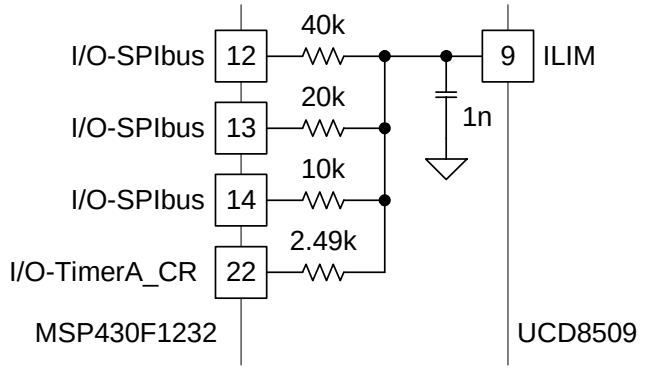


Fig. 24. Current limit adjustment using "poor man's DAC".

The digital output ports are three state outputs, they can be high impedance or connected either to GND or to the VCC voltage of the microcontroller. When all four outputs are high impedance, the default 0.5V threshold of the UCD8509 prevails. Assuming that pin 22 of the MSP430F1232 is connected to ground, to limit the maximum ILIM voltage below the 1V maximum threshold of the UCD8509, the microcontroller can select from 27 individual current limit thresholds between 0V and 1V using the other three ports.

During overload, the conduction time of the power MOSFET is limited by the cycle-by-cycle current limit circuit. When the current sense signal amplitude reaches the current limit threshold the gate drive output is immediately terminated to protect the power stage. This event is indicated by the CLF pin of the UCD8509 going high and can be read by the microcontroller. The typical waveforms of the converter in current limit mode are shown in Fig. 25.

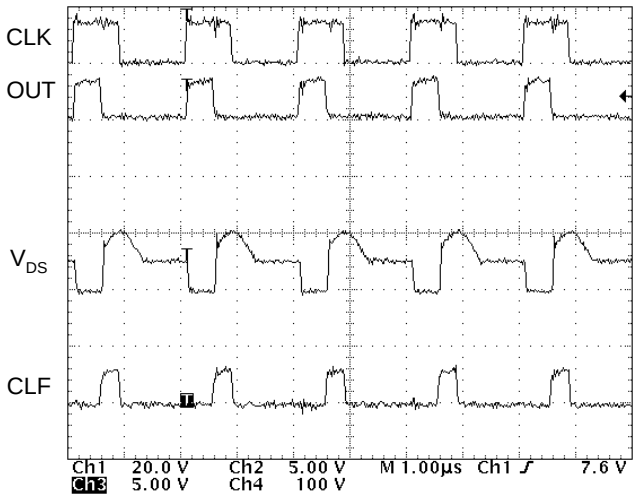


Fig. 25. Current limit operation.

In this design the power supply is allowed to operate in current limit mode for a fixed number of switching cycles before it shuts down. The number of cycles in current limit mode before shut down can be entered by the user through the GUI of the demonstrations software. This operating mode allows short periods of overload conditions – occurring typically during load transients – without the need to increase the steady state current limit of the power supply.

Temperature Protection

The demonstration power supply is equipped with a temperature shut down feature based on the board temperature of the module. In order to get a better reading of the critical temperature of the power components, an external sensor is favored over the built-in temperature sensor of the microcontroller. The thermistor is placed in close proximity to the power MOSFET.

In order to eliminate any potential noise coupling, its signal is filtered near the input pin (pin 11 – I/O-ADC5) of the MSP430F1232. The shut down threshold as well as the hysteresis of the temperature protection is user adjustable using the parameter entry screen of the demonstration software.

MOSFET Over Voltage Protection

The last protection function of the converter is based on the peak voltage stress of the primary MOSFET. The maximum voltage across the drain source terminal of the device is scaled and peak rectified. Once the measured stress voltage reaches the user entered shutdown threshold the converter stops operating. The shut down is followed by an automatic restart, initiating the full soft-start routine.

Software Algorithm

Without going too deep into the fine details of the software, one important characteristic of the controlling algorithm must be highlighted. In most applications the available computational resources and data conversion speed necessitates that the execution of the software functions are distributed over several switching periods. Accordingly, the functions are divided to two categories; basic functions which must be executed in every switching period and auxiliary routines which are scheduled over a longer period. This scheduling technique is demonstrated in Fig. 26.

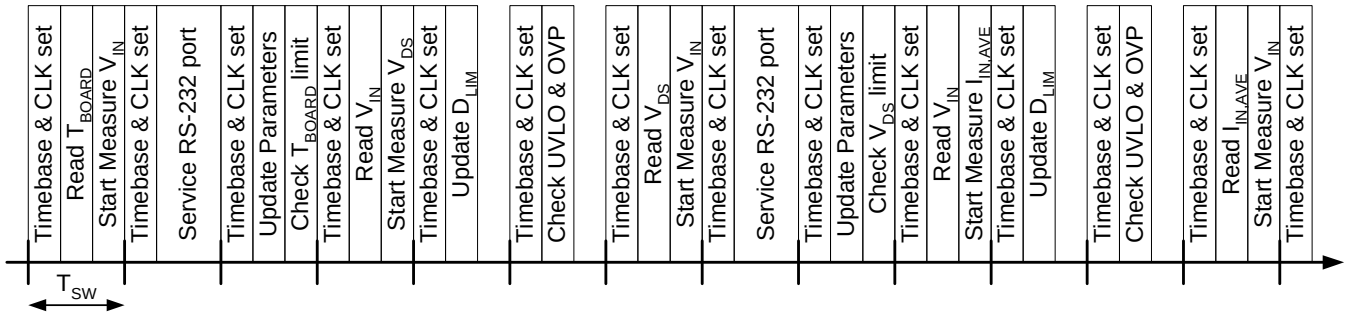


Fig. 26. Software scheduling example.

The diagram shows the program flow in steady state operation. The basic time base and CLK signal generation functions are performed in every switching cycle since they are essential to the proper operation of the analog companion circuit. In every third cycle the microcontroller initiates a signal measurement. The frequency of the ADC conversions is limited by the maximum speed of the analog-to-digital converter of the microcontroller. Since the most important input parameter is the input voltage, every second measurement cycle is dedicated to the input voltage measurement. In between the input voltage measurements the other analog parameters are measured in a rotating fashion. Once a measurement result is available, the microcontroller recalculates its internal variables and compares the measurement result against the limit values of the particular variable. In addition, a significant amount of the microcontroller's resources are reserved for communication in the demonstration software because of the frequent update of the displayed results.

Some of the software functions are assisted by specialized hardware resources in the MSP430F1232. For instance, no significant resources are allocated to handle the CLF signal. The number of current limit cycles is counted by the microcontroller's capture & compare register which generates an interrupt when the allowed number of consecutive current limit cycles is reached.

This short description of the software does not attempt to cover all aspects of the software development, but rather to show the level of expertise required to write the program. When power supply engineers make the first steps towards digital control, it might be wise to supplement their vast amount of power supply know-how with the proficiency of a skilled software engineer as it was the case in this project.

VI. SUMMARY

This paper aimed to introduce digital power supply control to the practicing power supply design community. Like most new technology, digital control in power supplies is expected to start its proliferation slowly. But this is definitely a trend not to overlook in the years to come.

At the same time, it is important to remember that the power supply is still a fundamentally analog circuit. The knowledge of various power supply topologies and related analog design expertise can not be substituted even by the most advanced software algorithm. On the other hand, digital implementation of the converter's control offers new opportunities to develop advanced features and make the power supply a more visible, more integrated part of the system.

While transitioning to full digital control might require a completely different approach and skill set in the controller design, the circuit example of this paper presents a practical, intermediate step towards that final goal. As demonstrated by this converter, advanced features and protection functions, and communication capability can be integrated cost effectively and reliably in a quarter brick form factor.

Topic 7

Compensating DC/DC Converters with Ceramic Output Capacitors

Texas Instruments

Compensating DC/DC Converters with Ceramic Output Capacitors

Rais Miftakhutdinov

ABSTRACT

The latest technology uses ceramic capacitors as the main part of filtering in DC/DC converters. This low-ripple solution is small and inexpensive. However, ceramic capacitors in the output filter require an advanced feedback and compensation circuit design than that used for traditional electrolytic capacitor. Transient performance of a DC/DC converter with a low-output capacitance filter depends significantly on the gain and bandwidth of the feedback loop. Ceramic capacitors cause higher resonant frequency of the output filter and a sharp phase lag, affecting stable operation of a DC/DC converter. Worst-case analysis for different conditions takes into account components and parameters tolerances. The suggested compensation-circuit design procedure ensures highest gain and bandwidth of frequency response, with comfortable phase and gain margin for stability.

I. INTRODUCTION

Size, cost, and accuracy remain important for any DC/DC converter design. However, these, often contradictory, criteria require proper output-filter components and optimized loop-compensation circuit design. Recently, the cost and stability have improved for ceramic capacitors with tens of microfarads of capacity. Therefore, these capacitors are now attractive as output filters of DC/DC converters, since their low equivalent series resistance (ESR) and equivalent series inductance (ESL) offer substantial benefits of lower output ripple voltage and reduced size. However, compared to traditional electrolytic types with larger ESR and ESL, ceramic capacitors also give an output filter a higher resonant frequency, lower damping, and a more nearly ideal second-order characteristic, with a sharp and almost full 180° phase lag at resonance.

Best load-current transient response requires optimizing both the output filter and the feedback loop. Traditional filter designs with electrolytic capacitors successfully use larger capacitance values to provide low output ripple. These higher values have also relaxed the need to maximize the control bandwidth for fast transient response. However, ceramic output capacitors with less total capacitance require increased gain and bandwidth of the control loop for equivalent transient response. These requirements, while insuring unconditional stability with an ideal second-order filter, significantly challenge the circuit engineer.

This paper addresses that challenge, discussing worst-case conditions for voltage-mode control loop design, the effect of component tolerances and variations, and the effect of limited bandwidth of the error amplifier. It provides practical recommendations implemented in Mathcad™-based design software.

II. CERAMICS OUTPUT CAPACITORS VS ELECTROLYTIC

A. Main Parameters

The dramatic increase in capacitance-to-size ratio of ceramic capacitors with X5R, X7R dielectric within the last few years makes the switching DC/DC converters with ceramic output capacitors a very popular solution. This popularity is due to low cost, better filtering capability, high-frequency operation, and thermal stability of X5R, X7R ceramic capacitors. Table 1 compares typical characteristics of ceramic capacitors to those of other popular types, including electrolytic, OS-CON, and specialty polymer.

TABLE 1. TYPICAL CHARACTERISTICS OF VARIOUS OUTPUT FILTERING CAPACITORS

Type	Vendor	Part Number	V_{DC} (V)	C (µF)	ESR (mΩ)	ESL (nH)	Size (mm)	Relative Cost
Aluminum Electrolytic	Rubycon	6.3ZA1000	6.3	1000	24	4.8	10 (diam) x 16	1
OS-CON	Sanyo	4SP820M	4	820	8	4.8	10 (diam) x 10.5	6
POSCAP	Sanyo	4TPC150M	4	150	40	3.2	7.3 x 4.3 x 1.9	3
Ceramic	TDK	C3225X5R1A156M	6.3	15	2	0.5	3.2 x 2.5 x 1.35	0.7

Ceramic capacitors with X5R or X7R dielectric have much lower parameter variations and tolerances in comparison to the electrolytic capacitors. The latest ceramic capacitors have capacitance in the 10-µF to 100-µF range, with extremely low ESR, near 2 mΩ to 5 mΩ. Their capacitance has ± 20% tolerance or lower.

B. Output Voltage Ripple

Low ESR and ESL of ceramic capacitors significantly decrease the output voltage ripple of DC/DC converters. The ripple in this case depends primarily on capacitance value. The ripple of other types of capacitors with relatively large ESR is defined mainly by the ESR value. Thus the output voltage ripple reflects the current ripple waveforms of the output inductor. The waveforms in Fig. 1 show the switching waveforms and output voltage ripple of a DC/DC converter using 2 x 150-µF specialty-polymer capacitors. The waveforms in Fig. 2 relate to the regulator with 3 x 22-µF ceramic capacitors. Both regulators have the same 0.65-µH output inductor and run at the same switching frequency of 700 kHz. The input voltage is 3.3 V and the output voltage is 1.8 V for these measurements. The peak-to-peak ripple using totally 66-µF ceramic capacitors is only 6.4 mV, while the totally 300-µF SP capacitors have peak-to-peak ripple of 23.2 mV.

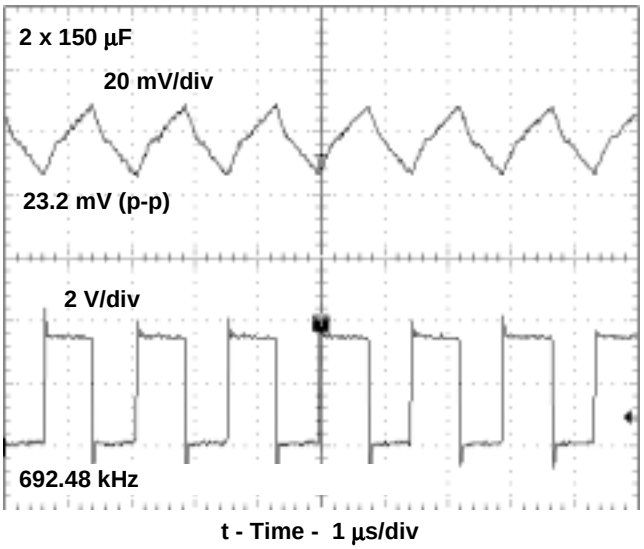


Fig. 1. Output ripple and switching waveforms of converters with specialty-polymer capacitors.

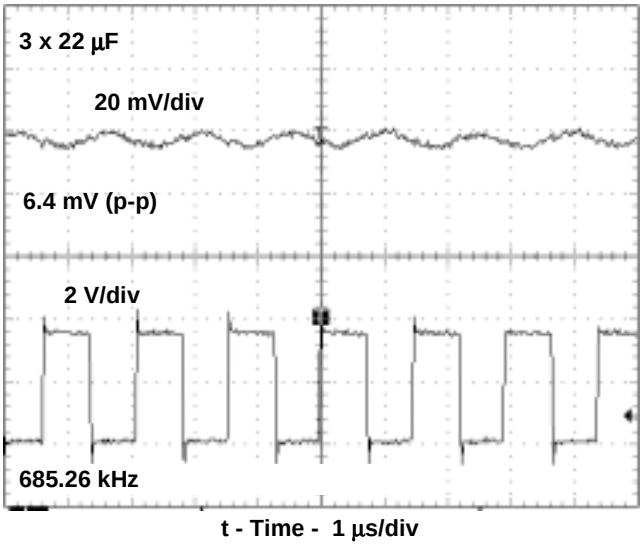


Fig. 2. Output ripple and switching waveforms of converters with ceramic capacitors.

C. Output Filter Frequency Response

Output capacitor parameters and their tolerances significantly affect the frequency response of the regulator. The differences of typical output-filter frequency responses for electrolytic and ceramic capacitors are illustrated in Figs. 3 and 4. When using electrolytic capacitors, selecting a larger inductance value generates approximately equal output ripple at the same switching frequency as the ceramics.

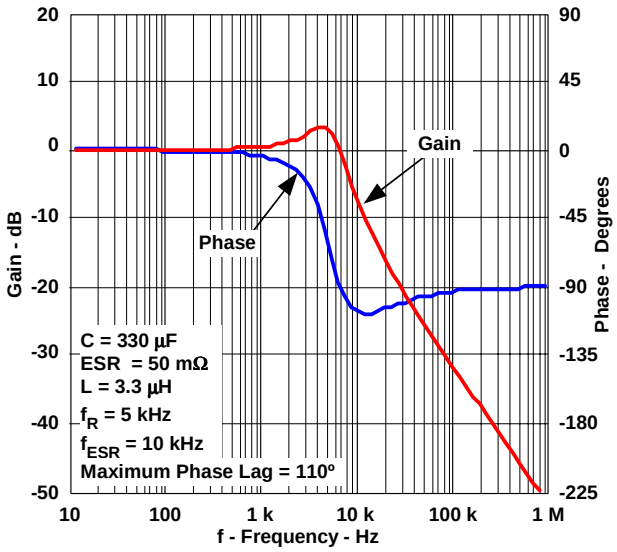


Fig 3. Frequency response of output filter with electrolytic capacitors.

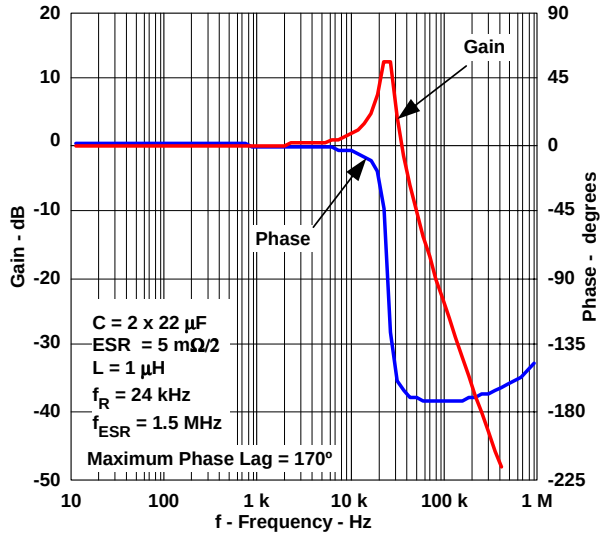


Fig 4. Frequency response of output filter with ceramic capacitors.

Most electrolytic capacitors have relatively large capacitance and ESR values that vary by 2 to 3 times or more, depending on the type and lot of capacitor, temperature and frequency. ESR of the output capacitor and its variation affect the feedback-loop design, because one of the poles of the compensation circuit is usually selected equal to the frequency of the ESR-zero. Variation of output capacitance leads to the variation of corner frequency of the output L-C filter. This fact also influences compensation circuit design. Because of wide tolerances and variations, electrolytic capacitors require at least 60° phase margin at nominal operating condition when the compensation circuit of the feedback loop is selected.

The frequency of the ESR-zero for ceramic capacitors is located in the MHz range. It is far above the typical crossover frequency, which is usually less than 1/5 of the switching frequency. That means that the ESR-zero has negligible effect on compensation-circuit design. For example, the crossover frequency of a 700-kHz switching frequency regulator does not exceed 140 kHz, which is much lower than the frequency of the ESR-zero.

Fig. 4 shows that the output filter of a DC/DC converter using ceramic capacitors has about 5-times higher resonant frequency (F_R), 15-times higher ESR-related zero frequency (F_{ESR}), and a phase lag of 170° versus 110° for the electrolytic output capacitor. For example, an ideal second-order filter provides 180° phase lag, and thus the output filter with ceramic capacitors is close to ideal.

D. Transient and Frequency Response of Converter Using Electrolytic Capacitors

Ceramic and electrolytic capacitors behave differently during the load-current transients of the DC/DC converter.

A typical example of the load current transient response using electrolytic output capacitors is shown in Fig. 5. Two transient peaks, V_{m1} and V_{m2}, must be considered closely. Peak V_{m1} occurs at the beginning-of-load current step. It is defined by ESR and ESL of the output capacitor. This spike is too fast for the feedback loop of the converter. The ESL-related part of V_{m1} can be decreased by adding high-frequency decoupling capacitors. The ESR-related portion requires more capacitors in parallel or more expensive, lower ESR electrolytic capacitors.

The second peak V_{m2} is caused by the removal of charge from the output capacitor during the load current step-up. A similar but positive peak occurs during the load current step-down. In that case it is caused by the excessive charge delivered from the output inductor. The amplitude of second peak V_{m2} depends on optimal output filter selection and on how quickly the feedback loop of the converter responds on transient [1],[2]. However, relatively large capacitance helps maintain the output voltage dynamic deviation within the required window, even with the relatively slow feedback loop. The loop frequency response for this converter is shown in Fig. 6. The crossover frequency is 33 kHz, and the phase margin is 88°. Because of low bandwidth and gain feedback loop, the output voltage returns to the nominal value slowly, after more than 100 µs in this case. However, for this particular output filter, increase of loop bandwidth does not affect peak-to-peak output voltage deviation, because V_{m2} is already less than V_{m1}. It is important to remember that the output ripple of converters with electrolytic capacitors can occupy a significant part of the voltage window allowed for the transient response. Standard evaluation module with electrolytic capacitors TPS54310EVM-201 from TI [8] has been used for the measurements.

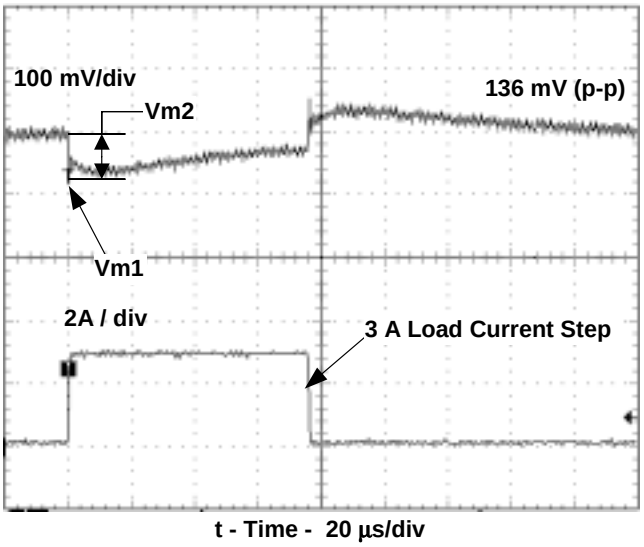


Fig. 5. Load current transient response of converter using electrolytic capacitors.

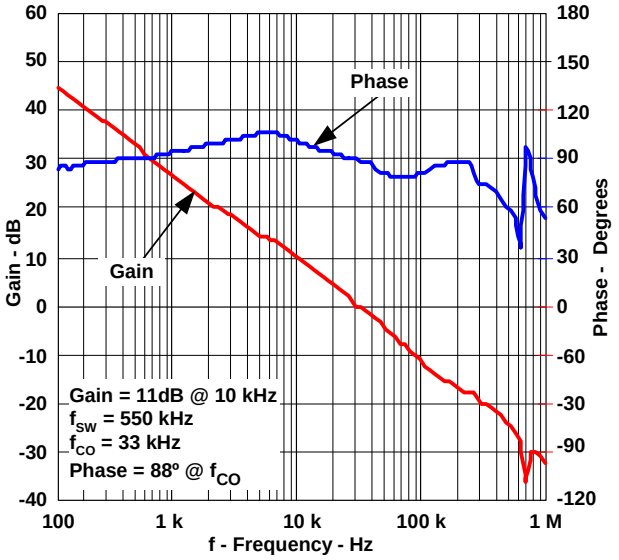


Fig. 6. Frequency response of converter using electrolytic capacitors.

E. Transient and Frequency Response of Converter Using Ceramic Capacitors

The load current transient response of a converter using ceramic output capacitors is shown in Fig. 7. TI's Evaluation module TPS54610EVM-213 using ceramic capacitors is selected for the comparison [5].

In case of ceramic capacitors, the first peak V_{m1} is negligible because of low ESR and ESL. The output ripple is also very low and practically does not affect peak-to-peak voltage deviation during the transient. However, the second peak V_{m2} is larger in comparison to the electrolytic capacitors. This difference occurs because ceramic capacitors experience the same excessive charge and discharge during the transients as electrolytic capacitors in previous section, but their capacitance is much lower. Selection of lower output inductance helps to reduce the charge applied to the capacitor during the transients because of the shorter time needed to change the inductor current to the new load level. However, it does not solve the problem if the feedback loop does not respond quickly on transient. The loop frequency response for this converter is shown in Fig. 8. The compensation circuit for this version is referred to as Circuit A for the comparison. It has a crossover frequency of 60 kHz and a gain of 12 dB at 10 kHz while for the converter with electrolytic capacitor the crossover frequency 33 kHz and the gain 10 dB at 10 kHz were sufficient (Fig. 6). Thus, an output filter with ceramic capacitors requires higher feedback loop bandwidth to provide similar transient performance as the electrolytic capacitors.

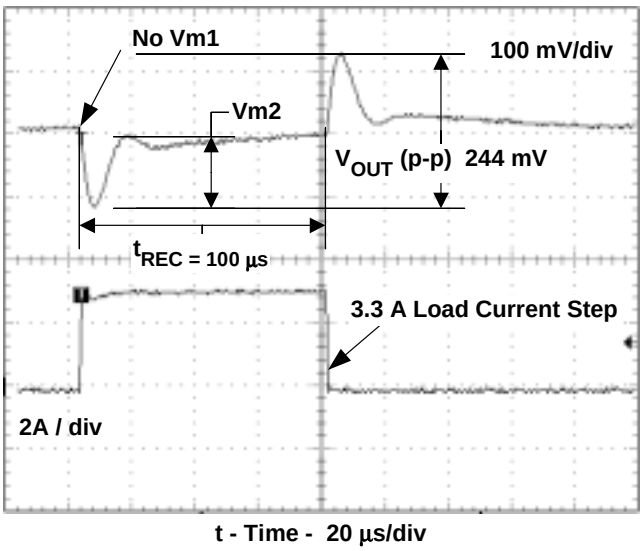


Fig. 7. Load currrent transient response of converter using ceramic capacitors.

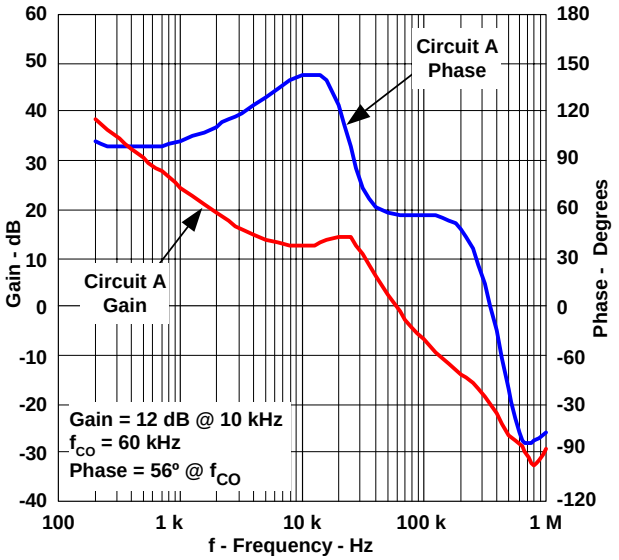


Fig. 8. Frequency response of converter using Compensation Circuit A.

Figs. 9 and 10 illustrate the effect of the increased bandwidth and gain feedback loop using Compensation circuit B. The feedback loop of the example shown in Fig. 8 has been modified to increase the crossover frequency up to 80 kHz and the gain up to 22 dB at 10 kHz. At the same transient conditions, 3.3-V input voltage, 1.8-V output and 3.3-A current step, the converter with higher gain and bandwidth has peak-to-peak transient response of 184 mV and recovery time of 20 µs (Fig. 9), while the converter with the original loop has 244 mV and 100 µs (Fig. 7). This is a 33% improvement of the peak-to-peak output voltage transient. To provide the same peak-to-peak transient response, the converter with low bandwidth requires more output ceramic capacitors, thus increasing the cost of converter.

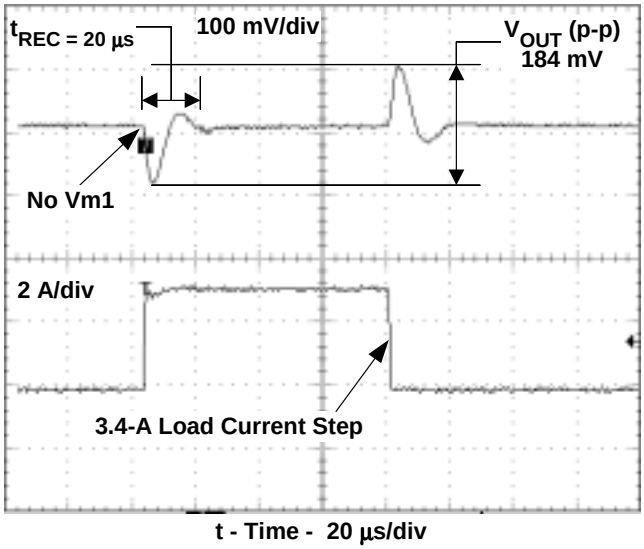


Fig. 9. Transient response improvement for the converter.

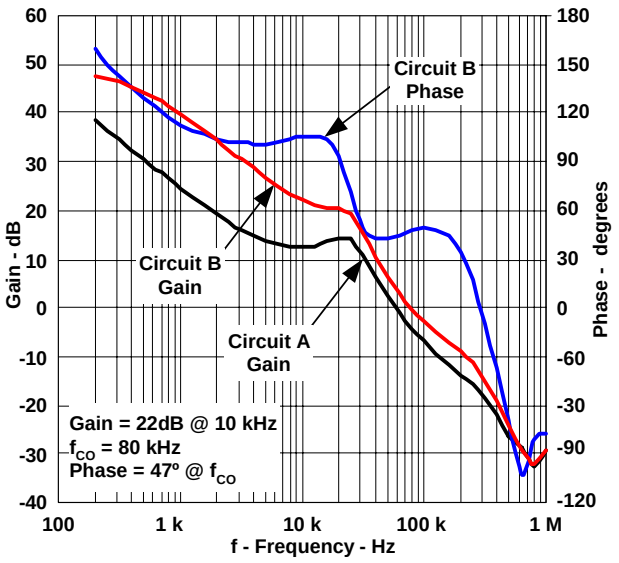


Fig. 10. Frequency response using Compensation Circuit B.

III. Accuracy of Small Signal Analytical Model for DC/DC Converter with Voltage Mode Control

Stable operation of switching DC/DC converters requires an adequate frequency response phase and gain margin. The previous section of this paper discussed the importance of high gain and bandwidth in the feedback loop for better transient response of DC/DC converters with ceramic output capacitors. Increased loop bandwidth requires careful consideration of converter switching delays, sampling, and error amplifier limitations that may affect accuracy of existing small-signal frequency response models. A simplified schematic of a synchronous buck converter with voltage-mode control is shown in Fig. 11. The overall frequency response loop has two main parts. The first part includes the power-stage, driver, and PWM comparator. The second part is the compensation circuit, which includes an error amplifier and additional impedances Z1 and Z2, which shape the required feedback-loop frequency response.

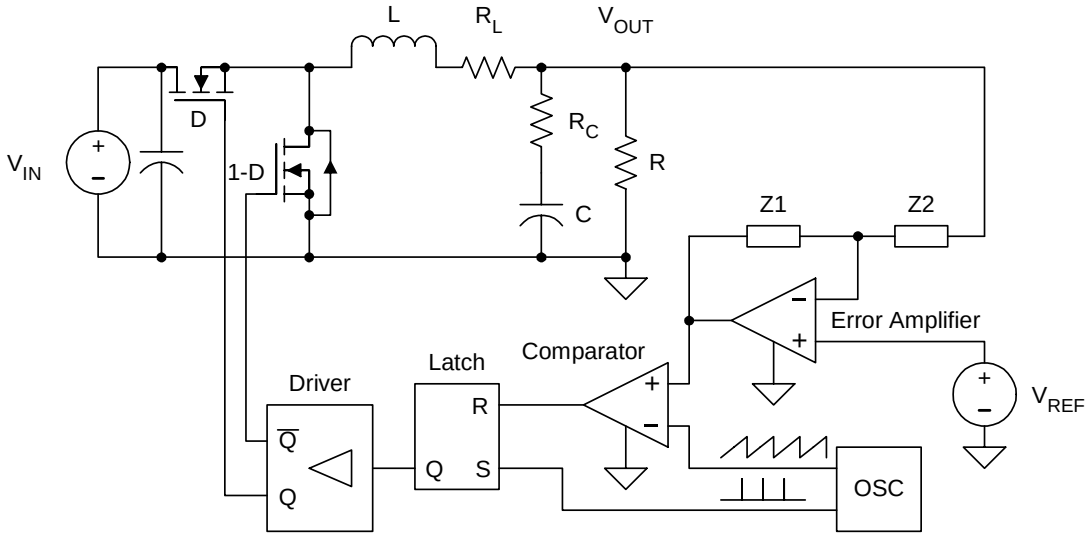


Fig. 11. Simplified schematic of voltage-mode control synchronous buck converter.

F. Power Stage and Modulator Transfer Function

The widely-used small-signal transfer function of the power stage and modulator for synchronous buck converter is defined by equation (1), where:

- V_S is the input voltage
- R is the load resistance
- L is the output inductance
- C is the output capacitance
- R_L is the sum of output inductor DC resistance and $R_{DS(ON)}$ of FETs
- R_C is the equivalent series resistance (ESR) of the output capacitor
- K_{PWM} (=1/V_{PWM}) PWM gain where V_{PWM} is an amplitude of the ramp modulation signal

It does not take into account any potential phase lag caused by modulator and driver delays and by sampling. To verify the validity of the equation, the frequency response is measured on a standard evaluation module with ceramic capacitors TPS54610EVM-213 from TI [5], at the following conditions:

- V_S = 3.3 V
- V_{OUT} = 1.8 V
- R = 1800 Ω
- C = 3 × 22 µF
- R_C = 1 mΩ
- R_L = 58 mΩ
- L= 0.65 µH
- V_{PWM} = 1 V
- F_{SW} = 700 kHz

All further analysis and measurements are based on the same module TPS54610EVM-213. The schematic, list of materials, and other technical details related to this module are in [5].

Comparison of measured frequency response and plots calculated from equation (1) (Figs. 12 and 13) does not reveal any phase lag associated with the delay and sampling effect. The measured Bode plots closely replicate behavior of a second-order filter at frequencies up to 350 kHz (half the switching frequency, 700 kHz). Half of the switching frequency is the theoretical limit that determines whether small-signal analysis applies to the switching system.

$$Wpt(s) = Vs\left(\frac{R}{R+R_L}\right)K_{PWM}\frac{1+s\times R_C\,C}{1+s\left(R_C\,C+\frac{R\,R_L}{R+R_L}\times C+\frac{L_O}{R+R_L}\right)+s^2\times L_O\,C\times\left(\frac{R+R_C}{R+R_L}\right)} \quad (1)$$

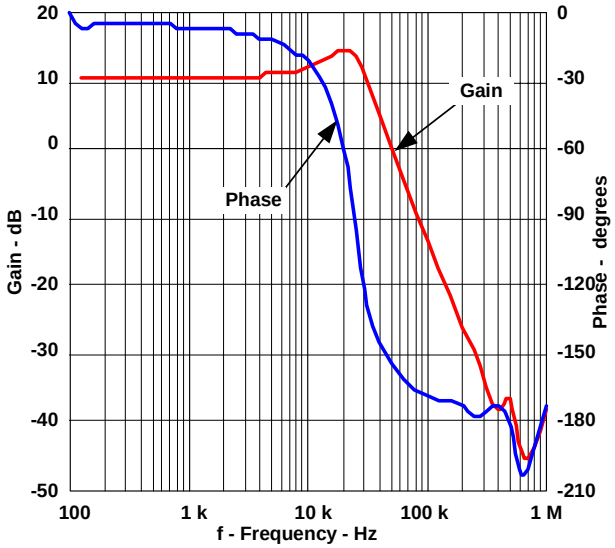


Fig. 12. Experimental results based on measurements.

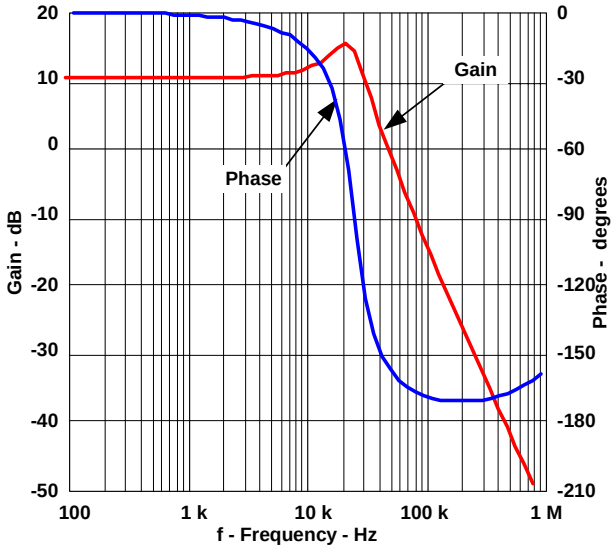


Fig. 13. Model in accordance with equation (1).

G. Transfer Function of Type 3 Compensation Circuit and its Limitation

The type 3 compensation circuit in Fig.14 is widely used for voltage-mode control because of design flexibility.

The generic transfer function of an ideal error amplifier with type 3 compensation is defined by equation (2):

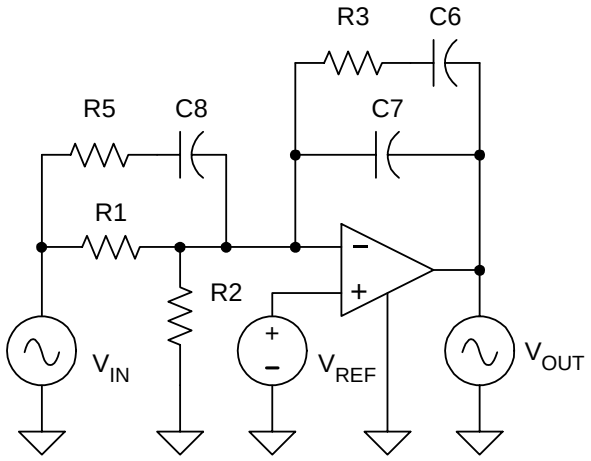


Fig. 14. Type 3 compensation circuit.

The type 3 compensation has a pole at the origin (integrator) that ensures high dc gain and resulting low output-voltage error of the converter. Additionally, a pair of available zeros provides required phase boost near resonant frequency thus allowing increased bandwidth of feedback loop. Another pair of additional poles sets required gain margin in high-frequency region. However, the actual frequency response measurements of converters with ceramic capacitors, designed for the high-bandwidth feedback loop, revealed an unexpected and sharp phase-lag at frequencies above 200 kHz.

$$W1(s) = \frac{\left[1 + s\ C8\ (R1 + R5)\right]\left(1 + s\ C6\ R3\right)}{s\ (C6 + C7)\ R1\ (1 + s\ C8\ R5) \times \left[1 + s\ R3 \times \left(\frac{C6\ C7}{C6 + C7}\right)\right]} \tag{2}$$

The theoretical frequency response and experimental measurements are shown in Figs. 15, 16, and 17 for the comparison. The measured gain (Fig. 15) and gain based on equation (2) (Fig. 16, solid line) coincide well up to 200 kHz. At frequencies above 200 kHz, the measured gain declines at 20 dB/decade, while the theoretical gain still increases until it reaches a frequency of about 1 MHz. The internal gain of error amplifier, built into the same plot (Fig. 16, straight line), explains this effect. If the frequency response of the compensation circuit goes beyond the boundary of the error-amplifier internal bandwidth then the 20-dB/decade slope of the error-amplifier internal gain defines the phase of the compensation circuit

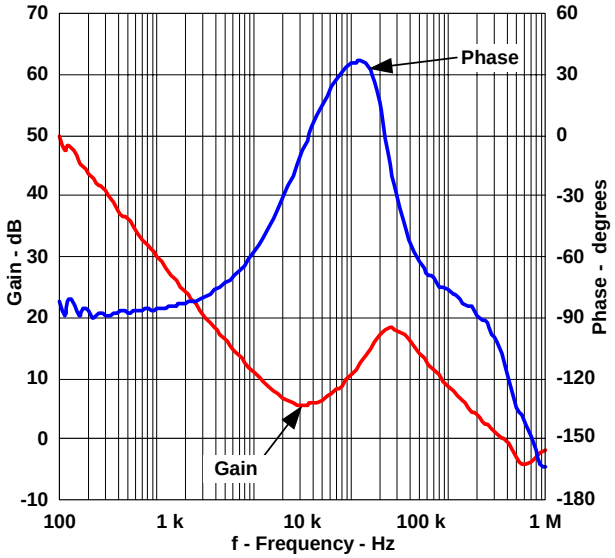


Fig. 15. Measured gain and phase.

The only way to avoid this issue with compensation circuit is to stay below the bandwidth limit of the error amplifier[9]. (The gain and phase based on this assumption are shown in Figs. 16 and 17 by dashed lines.) That means that higher bandwidth of the error amplifier is required to take full advantage of ceramic as opposed to electrolytic capacitors.

The transient of existing design may need to be improved even if the compensation circuit has reached the error-amplifier limit. Room remains for the transient response improvement but equation (2) is not valid above the error-amplifier limit.

However, an accurate equation can be derived that predicts gain and phase of frequency response when the compensation circuit exceeds the boundary of the error amplifier. The new equation helps to improve transient performance of a DC/DC converter using the existing error amplifier.

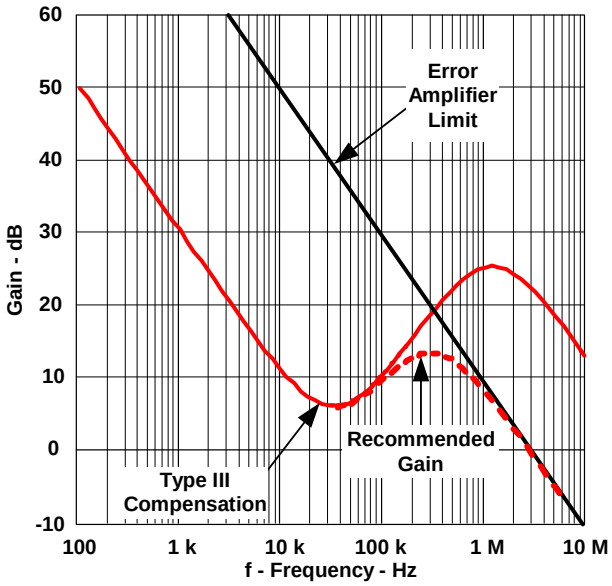


Fig. 16. Gain based on equation (2).

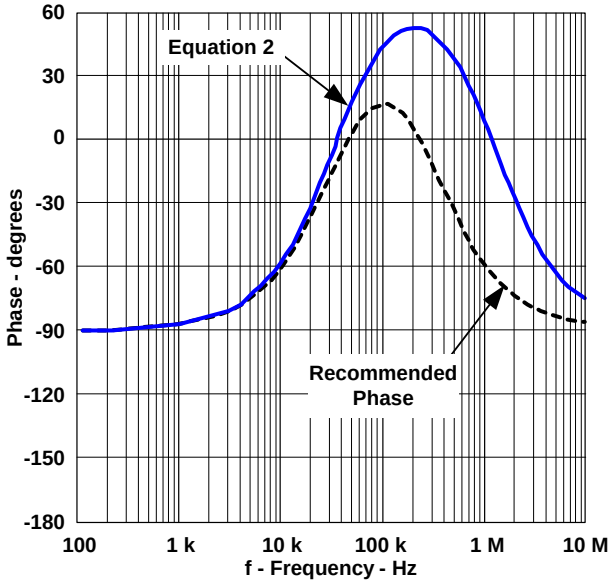


Fig. 17. Phase based on equation (2).

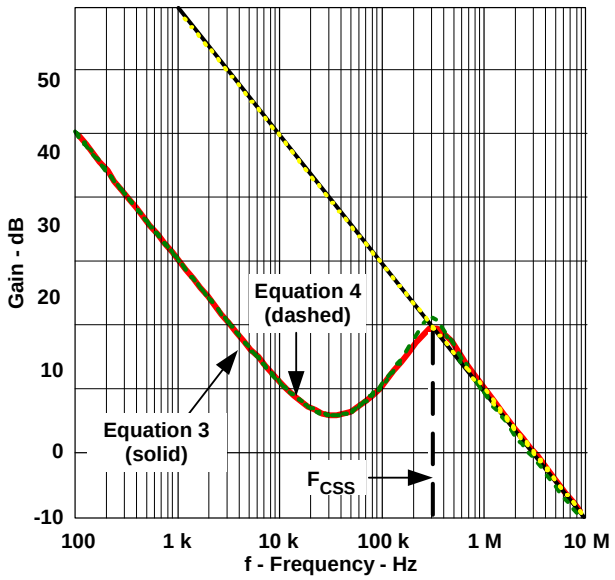


Fig. 18. Gain based on equations (3) and (4).

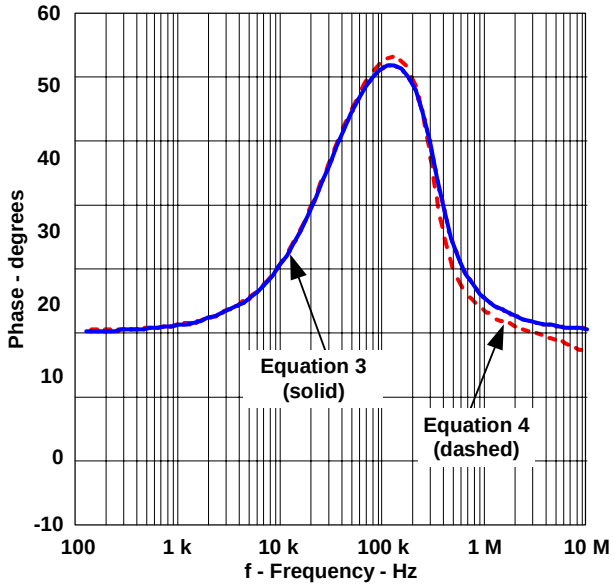


Fig. 19. Phase based on equations (3) and (4).

Assume that the compensation circuit frequency response curve, originally selected using equation (2), crosses the error amplifier boundary at the frequency F_{CSS} (Fig. 18).

The curve has positive 20-dB/decade slope below F_{css} and then changes its slope to negative 20 dB/decade above F_{css}. So, the total slope change is 40 dB/decade. This behavior is similar to the straight line approximation of a second-order filter with the resonant frequency equal to F_{css} and the quality factor Q = 1. The effect of the two poles in equation (2) is negligible, because they are located well above F_{css} (Fig. 16). With these assumptions, equation (3) below applies. A more general equation (4) describes a non-ideal inverting operational amplifier and is provided in equation (4) in [7].

$$W1(s) = \frac{\left(-a(s)\times Z1\right)}{\left(Z1 + Z2 + a(s)\times Z2\right)} \qquad (4)$$

The variable a(s) in this equation is the frequency response of non-ideal amplifier itself and Z1 and Z2 are the compensation circuit impedances shown in Fig. 11. This general equation becomes complicated after the substitution of all variables. However, it is preferable for the final design validation with the help of computer software tools.

The gain and phase of the compensation circuit in accordance with equations (3) and (4) are shown in Figs. 18 and 19 respectively. Fig. 18 also includes the boundary of the error amplifier, shown as the straight line to the right. The gain and phase based on the new equations (3) and (4) closely match the measured frequency response shown in Fig. 15. Note that equation (3) is most accurate if the high frequency poles in accordance with equation (2) are at least 4 times higher than F_{CSS}.

The frequency above 3 MHz must be excluded from the comparison, because the test setup is not highly accurate in the MHz region. That range is outside the practical design scope for this application.

$$W1(s) = \frac{\left[1 + s\ C8\ \left(R1 + R5\right)\right]\times\left(1 + s\ C6\ R3\right)}{s\ \left(C6 + C7\right)\ R1} \times \left[\frac{1}{1 + \left(\frac{s}{2\pi\times F_{CSS}}\right) + \left(\frac{s}{2\pi\times F_{CSS}}\right)^2}\right] \qquad (3)$$

IV. Worst-Case Stability Analysis at Two Critical Conditions

The following parameters affect the worst-case analysis based on equations (1) and (3):

- Operating conditions, including input voltage and load-resistance range.
- Power stage parameters, including output inductor and capacitor tolerances, resistance of power FETs, and DCR of the output inductor. Variations of these parameters are important, because the corner frequency and damping factor of the L-C output filter depend on these parameters.
- Internal error-amplifier and PWM-modulator tolerances, including gain and bandwidth of the error amplifier, ramp-signal variation, and additional phase lag when the compensation circuit frequency response exceeds the boundary of the error amplifier gain.
- External components, including three resistors and three capacitors and their tolerances when using type 3 compensation.

Two worst-case situations become obvious from the Bode plots in Fig. 8. The first one, based on the abrupt phase lag at frequencies above 200 kHz, is due to the limited bandwidth of the error amplifier. The extreme condition in this case occurs when the error amplifier has minimum bandwidth while the rest of the feedback loop has maximum gain and bandwidth. This condition occurs when the input voltage is high and the output inductor and capacitor are at their lowest values. In this situation, the compensation circuit may not provide the required phase-boost at frequencies above 200 kHz, because it is limited by the error amplifier bandwidth.

Another worst-case condition is at the minimum gain and bandwidth, where the resonant frequency of the output filter stays close to the crossover frequency. In Fig. 8 this is the area near 50-kHz frequency. Additional phase lag in this area because of feedback-loop tolerances may cause conditional instability at transients, or even unconditional oscillation if the gain is low enough at steady-state condition.

Table 2 shows the worst-case tolerances of all variables for these two conditions. The possibility of 14 different variables having worst-case condition is relatively low, but the statistical analysis of tolerances is outside the scope of this paper. Maximum load resistance is selected as the worst case for both conditions because lower damping means larger phase-lag for the second-order output filter.

Table 2. Worst Case Tolerances for the Two Extreme Conditions

Component/Parameter	Condition 1: Maximum Gain	Condition 2: Minimum Gain
Input voltage	$V_{S(max)}$	$V_{S(min)}$
Load resistance	Maximum	Maximum
Error amplifier bandwidth	3 MHz (minimum)	3 MHz (minimum)
Ramp signal	- 10%	+ 10%
Output inductor L	- 20%	+ 20%
Output capacitor C	- 20%	+ 20%
Compensation C6, C7, C8 (Fig. 14)	± 20%	± 20%
Compensation R1, R3, R5 (Fig. 14)	± 1% (± 3% over temperature)	± 1% (± 3% over temperature)

Worst-case Bode plots, calculated for Conditions 1 and 2 in accordance to Table II, are shown in Figs. 20 through 23. All data for the analysis are taken from [5], except that C1 is 270 pF instead of 470 pF, and C4 is 3300 pF instead of the original 470 pF (p. 4-2, Fig. 4-1 in [5]). The solid line shows frequency response when all feedback loop parameters have nominal values. The dashed and dotted lines show Bode plots at Conditions 1 and 2 at worst-case tolerances of components R1, R3, R5, C6, C7, and C8 (Fig.14). For Condition 1, minimum phase margin is about 43°, and for Condition 2 it is about 38°. The input voltage for Condition 1 is 6 V and for Condition 2 is 3 V. The phase margin varies from 38° to 55° and gain margin from -10 dB to -26 dB after taking into account all worst-case conditions and tolerances. The crossover frequency varies in the range from 45 kHz to 130 kHz. At minimum load resistance, the damping is higher, phase shift is lower and the phase margin is even higher. This analysis shows that 45° phase margin, -10 dB gain margin, and 100 kHz crossover frequency can be taken as the design goal at nominal conditions for the voltage-mode control, synchronous buck-converters using ceramic capacitors in the output filter. This combination allows stable operation at worst-case conditions and good dynamic response of DC/DC converter at large load-current transients

V. Feedback Loop Design Recommendations

Most recommendations and design rules for selecting feedback-loop bandwidth and stability margins are based on industry's long-time experience with electrolytic capacitors [3], [4]. Usually, a phase margin ranging between 45° and 60° is recommended to avoid instability caused by feedback-loop variation because of components and parameters tolerances. The crossover frequency or feedback-loop band-width does not exceed 30 kHz in most designs using electrolytic capacitors. However, as mentioned in the previous section, the much lower tolerances of ceramic capacitors with X5R and X7R dielectrics as compared to tolerances of electrolytic capacitors allows selection of a comfortable 45° margin in most cases.

The outline below summarizes the lessons learned during an analysis, design, and performance measurements of DC/DC converters with ceramic-output capacitors using voltage-mode control. It specifies the design goals, outlines potential limits, and provides recommendations helpful for optimizing feedback-loop design for the best transient response while maintaining a comfortable margin for stability.

A. Design Goals

- Design for highest gain and bandwidth feedback loop, while allowing for worst-case conditions at any practically reasonable combination of feedback-loop tolerances.
- Provide phase margin of 45° for ceramic capacitors and 65° for electrolytic
- Allow at least 10 dB gain margin for less jitter and noise sensitivity.

B. Feedback Loop Limitations

- The error amplifier may limit compensation-circuit bandwidth.
- Crossing the frequency-response boundary of the error amplifier by the compensation circuit initiates a sharp phase lag at frequency about half a decade below crossing.
- Switching frequency may also limit crossover frequency: $F_{CO} < F_S/2$ (theory), $F_{CO} < F_S/5$ (practice).
- Abrupt phase lag at frequency above resonant might cause the conditional instability.
- Two conditions at worst-case tolerance combinations require verification for stability.

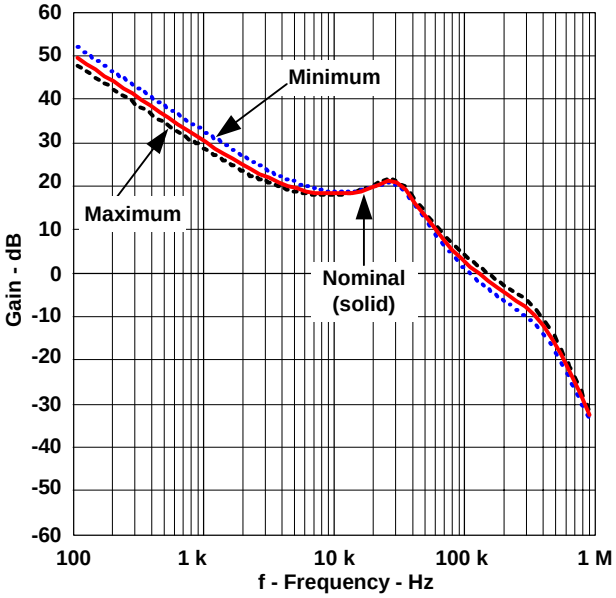


Fig. 20. Gain at worst case Condition 1.

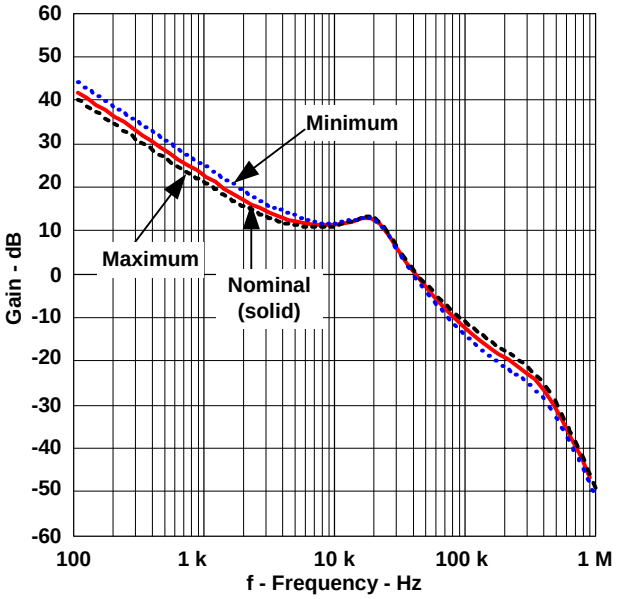


Fig. 22. Gain at worst case Condition 2.

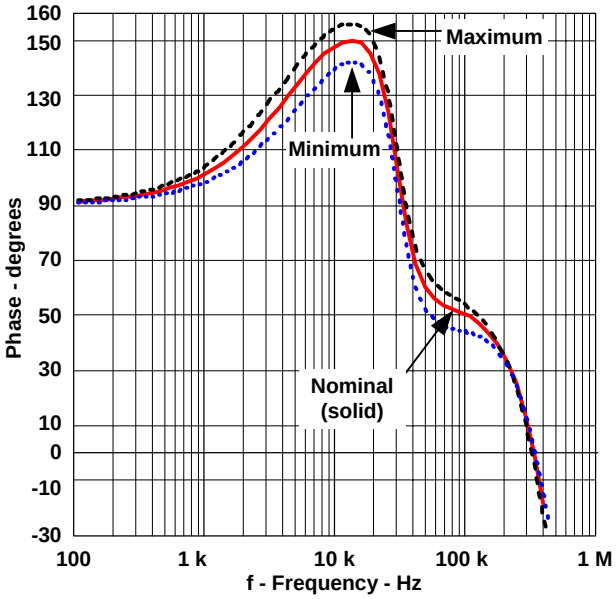


Fig. 21. Phase at worst case Condition 1.

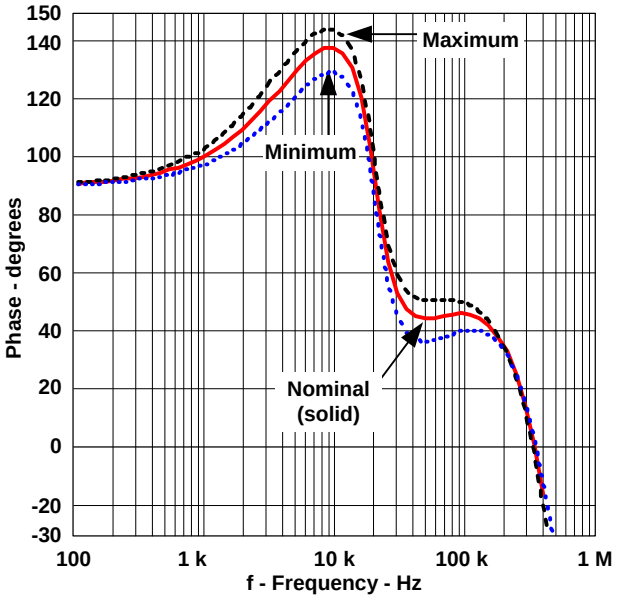


Fig. 23. Phase at worst case Condition 2.

C. *Recommendations*

- Keep gain and bandwidth as high as possible for good transient response.
- Use type-3 compensation circuit to provide proper phase boost.
- Accept compensation-circuit gain to between 10 dB and 20 dB at switching frequency. The low output-ripple of ceramic capacitors does not cause significant jitter of switching waveforms with this gain.
- Recognize that the frequency of ESR-zero does not affect compensation circuit design, because it is in MHz range. This is well above of the considered frequency range.
- Increase the bandwidth by putting two equal poles as high as possible, but not above the error-amplifier limits. Use of equation (3) for the compensation circuit allows design for higher bandwidth and improved transient response.
- Ensure that the crossover frequency does not exceed one-fifth (1/5) of switching frequency.
- After frequency of equal poles is located on the basis of maximum achievable crossover frequency, locate the fist zero in accordance with the equation

$$Fz1 = \frac{\left(Fr^2 \times 10^{\frac{1}{Q}} \right)}{Fp1} \qquad (5)$$

  where:
  - F_r is resonant frequency
  - Q is the quality factor

- Locate the second zero to ensure 45° phase margin at crossover frequency. If necessary, move this zero into lower frequency region to guarantee 30° phase margin at the frequency

$$Fr \times 10^{\frac{1}{2Q}} \qquad (6)$$

These design goals and recommendations have been implemented in the Mathcad™ file. The file includes not only worst-case feedback loop design for voltage mode control, but also steady state design including RMS currents, ripple, power losses, efficiency, etc. The file also generates main waveforms of power stage. This file is available for free distribution upon request [6].

VI. CONCLUSION

The main characteristics of ceramic capacitors versus electrolytic, OS-CON, and specialty polymer capacitors are compared. The pros and cons of use of ceramic capacitors in the output filter of DC/DC converters are analyzed and illustrated by measurements. Currently available ceramic capacitors, with thermally stable X5R and X7R dielectrics, provide a low cost, small size, low ripple solution but require optimal feedback loop design. The effect of feedback loop bandwidth and gain on the load-current transient-response is confirmed by experiments. Based on experiments, modification of the small-signal transfer function of synchronous buck converter for voltage mode control is described that takes into account error amplifier limitations. This analytical model is used for the worst-case stability analysis of DC/DC converters with ceramic output capacitors. Two worst-case conditions are investigated covering 14 different variations of feedback loop parameters and components. General recommendations for the optimal feedback loop design of synchronous buck converter with ceramic output capacitors are provided. This algorithm is implemented in a Mathcad-based program that includes complete steady-state and small-signal design of a buck converter.

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