1A, Single-Input, Single Cell Li-Ion Battery Charger with 50-mA LDO, and External Power Path Control

Check for Samples: bq25060

FEATURES

- **30V input Rating, With 10.5V Over-Voltage Protection (OVP)**
- **FET Controller for External Battery FET for External Power Path Control (BGATE)**
- **Input Voltage Dynamic Power Management**
- **50mA integrated Low Dropout Linear Regulator (LDO)**
- **Programmable Charge Current Through ISET and EN Pin**
- **0.5% Battery Voltage Regulation Accuracy**
- **7% Charge Current Regulation Accuracy**
- **Thermal Regulation and Protection**
- **Battery NTC Monitoring During Charge**
- **Status Indication – Charging/Done**
- **Available in small 2mm × 3mm 10 Pin SON Package**

APPLICATIONS

- **Smart Phones**
- **Mobile Phones**
- **Portable Media Players**
- **Low Power Handheld Devices**

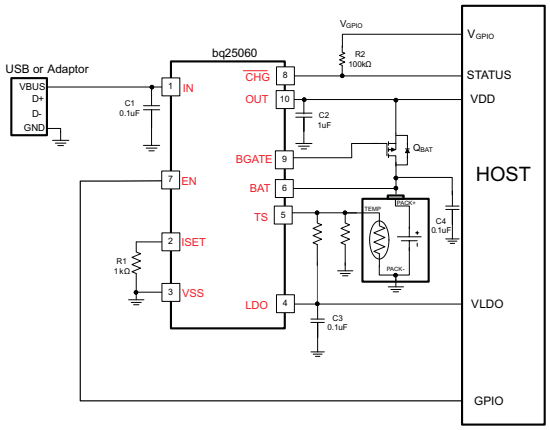
DESCRIPTION

The bq25060 is a highly integrated Li-Ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell Li-Ion battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The bq25060 has a single power output that charges the battery. The system load is connected to OUT. The low-battery system startup circuitry maintains OUT greater than 3.4V whenever an input source is connected. This allows the system to start-up and run whenever an input source is connected regardless of the battery voltage. The charge current is programmable up to 1A using the ISET input. Additionally, a 4.9V 50mA LDO is integrated into the IC for supplying low power external circuitry.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PART NO.	MARKING	MEDIUM	QUANTITY
bq25060DQCR	DAN	Tape and Reel	3000
bq25060DQCT	DAN	Tape and Reel	250

PACKAGE DISSIPATION RATINGS TABLE

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
10 Pin 2mm × 3mm SON(1)	58.7°C/W(2)	3.9°C/W	1.70W	0.017W/°C

(1) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is PD = $[T_{J(max)} - T_A]/R_{\theta JA}$.
(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2×3 via matrix.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE / UNIT
Input Voltage	IN (with respect to VSS)	–0.3 to 30 V
	EN, TS, $\overline{CHG}$, BGATE, ISET (with respect to VSS)	–0.3 to 7 V
Output Voltage	BAT, OUT, LDO, $\overline{CHG}$, BGATE (with respect to VSS)	–0.3 to 7 V
Input Current (Continuous)	IN	1.2 A
Output Current (Continuous)	BAT	1.2 A
Output Current (Continuous)	LDO	100 mA
Output Sink Current	$\overline{CHG}$	5 mA
Junction temperature, T_J		–40°C to 150°C
Storage temperature, T_{STG}		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	3.55	28	V
	IN operating voltage range	4.4	10.2	
I_{IN}	Input current, IN		1	A
I_{OUT}	Ouput Current in charge mode, OUT		1	A
R_{ISET}	Input current limit programming resistor range	1	10	kΩ
T_J	Junction Temperature	0	125	°C

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT						
V_{UVLO}	Under-voltage lock-out	V_{IN}: 0V → 4V	3.25	3.40	3.55	V

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{HYS-UVLO}$	Hysteresis on UVLO	V_{IN}: 4V → 0V		250		mV
$V_{BATUVLO}$	Battery UVLO	V_{BAT} rising	1.95	2.05	2.15	V
$V_{HYS-BUVLO}$	Hysteresis on BAT UVLO	V_{BAT} falling		125		mV
V_{IN-SLP}	Valid input source threshold V_{IN-SLP} above V_{BAT}	Input power good if $V_{IN} > V_{BAT} + V_{IN-SLP}$ V_{BAT} = 3.6V, V_{IN}: 3.5V → 4V	30	75	150	mV
$V_{HYS-INSLP}$	Hysteresis on V_{IN-SLP}	V_{BAT} = 3.6V, V_{IN}: 4V → 3.5V		32		mV
$t_{DGL(NO-IN)}$	Deglitch time, input power loss to charger turn-off	Time measured from V_{IN}: 5V → 2.5V 1µs fall-time		32		ms
V_{OVP}	Input over-voltage protection threshold	V_{IN}: 5 V → 11 V	10.2	10.5	10.8	V
$V_{HYS-OVP}$	Hysteresis on OVP	V_{IN}: 11 V → 5 V		100		mV
$t_{DGL(OVP)}$	Input over-voltage deglitch time			100		µs
$t_{REC(OVP)}$	Input over-voltage recovery time	Time measured from V_{IN}: 11V → 5V 1µs fall-time to LDO = HI, V_{BAT} = 3.5V		100		µs
V_{IN_DPM}	Input DPM threshold	V_{IN} Falling, V_{IN}-DPM enabled with EN	4.2	4.30	4.4	V
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Battery current into BAT, No input connected	V_{IN} = 0V, T_J = 85°C			6	µA
$I_{BAT(DONE)}$	BAT current, charging terminated	V_{IN} = 6V, $V_{BAT} > V_{BAT(REG)}$			10	µA
$I_{IN(STDBY)}$	Standby current into IN pin	EN = HI, V_{IN} < VOVP			0.6	mA
		EN = HI, V_{IN} ≥ VOVP			2	
I_{CC}	Active supply current, IN pin	V_{IN} = 6V, no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, IC enabled			3	mA
BATTERY CHARGER FAST-CHARGE						
$V_{BAT(REG)}$	Battery charge regulation voltage	T_A = 0°C to 125°C, I_{OUT} = 50 mA	4.16	4.20	4.23	V
		T_A = 25°C	4.179	4.200	4.221	
I_{IN_RANGE}	User programmable input current limit range	R_{ISET} = 1kΩ to 10kΩ, EN = VSS	100		1000	mA
$I_{IN(LIM)}$	Input current limit, or fast-charge current	EN = FLOAT	435	467	500	mA
		EN = VSS		K_{ISET}/R_{ISET}		
K_{ISET}	Fast charge current factor	R_{ISET} = 1kΩ to 10kΩ, EN = VSS	900	1000	1100	AΩ
$V_{DO(IN-OUT)}$	$V_{IN} - V_{OUT}$	V_{IN} = 4.2V, I_{OUT} = 0.75 A		500	900	mV
ISET SHORT CIRCUIT PROTECTION						
R_{ISET_MAX}	Highest resistor value considered a short fault	R_{ISET}: 900Ω → 300Ω, I_{OUT} latches off, Cycle power to reset, Fault range > 1.10A	430		700	Ω
$t_{DGL-SHORT}$	Deglitch time transition from I_{SET} short to I_{OUT} disable	Clear fault by cycling VBUS or $\overline{EN}$		1.5		ms
I_{OUT-CL}	Maximum OUT current limit regulation (Clamp)		1.2		2	A
PRE-CHARGE AND CHARGE DONE						
V_{LOWV}	Pre-charge to fast-charge transition threshold	External power path control disabled, BGATE = VSS	2.4	2.5	2.6	V
		External power path control enabled	2.8	2.9	3.0	
$t_{DGL(LOWV)}$	Deglitch time on fast-charge to pre-charge transition	V_{BAT} rising or falling		25		ms
$I_{PRECHARGE}$	Precharge current to BAT during precharge mode	V_{BAT} = 0V to 2.9V, Battery FET connected, Current out of BAT	28	37	45	mA
		V_{BAT} = 0V to 2.5V, BGATE = VSS, Input current limit regulated to $I_{PRECHARGE}$	41.5	45	48.5	
I_{TERM}	Default termination current threshold	V_{IN} = 5V, I_{CHARGE} = 100 mA to 1 A	7.5	10.5	13.5	$\%I_{IN(LIM)}$
RECHARGE OR REFRESH						
V_{RCH}	Recharge detection threshold	V_{BAT} falling	$V_{BAT(REG)}$ –0.13V	$V_{BAT(REG)}$ –0.1V	$V_{BAT(REG)}$ –0.065V	V
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected	V_{BAT} falling		25		ms
EXTERNAL POWER PATH CONTROL						

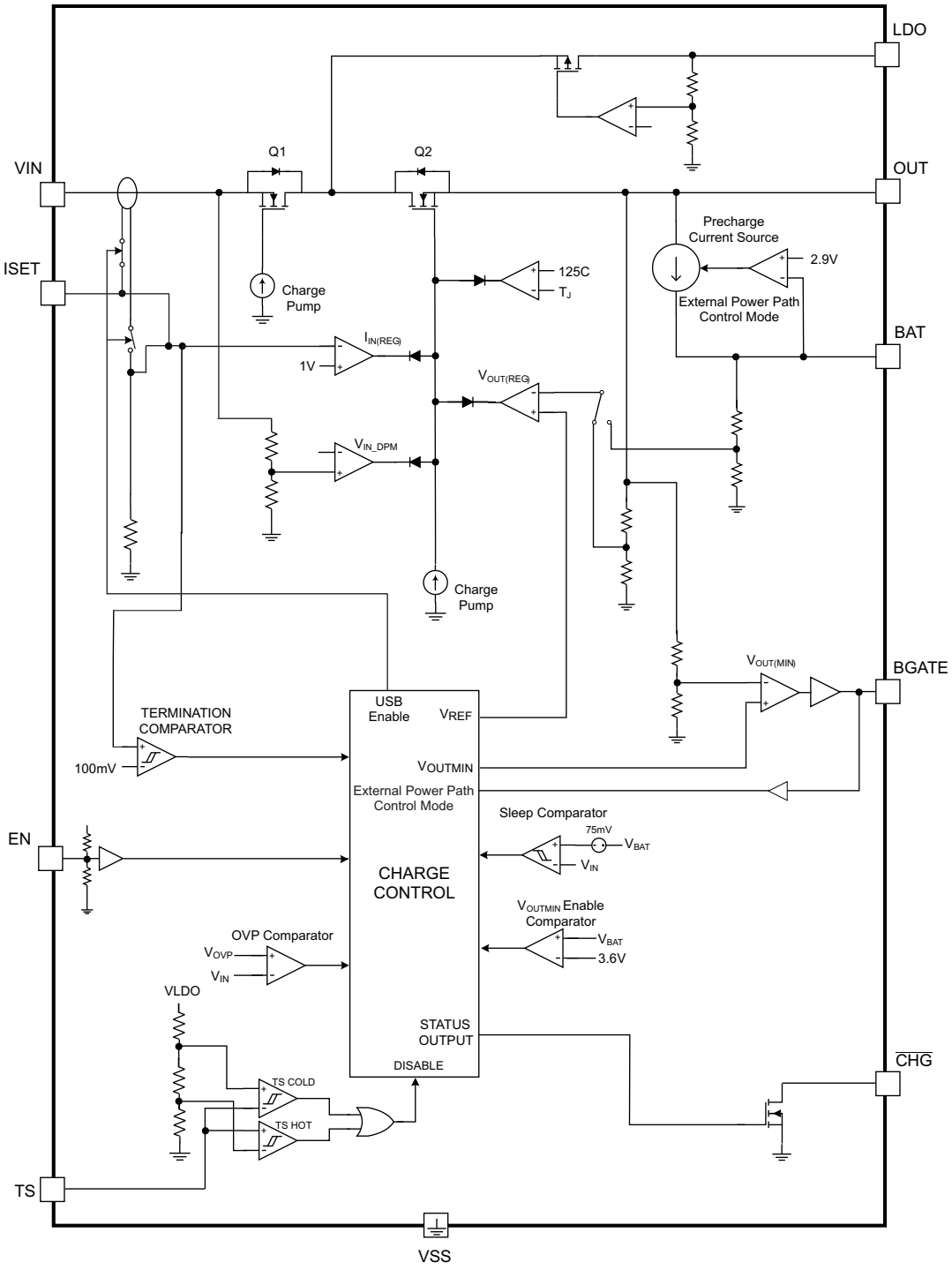
ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range 0°C ≤ T_J ≤ 125°C and VIN = 5V (unless otherwise noted)

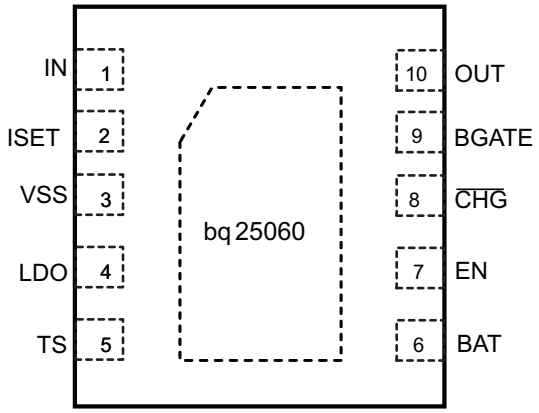
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{OUT(REG)}$	Output regulation voltage	V_{BAT} ≤ 2.9 V	3.4	3.5	3.6	V
		2.9 V < V_{BAT} ≤ 3.6V	3.44	3.59	3.75	V
		V_{BAT} > 3.6 V		V_{BAT} + $V_{drop(QBAT)}$		V
V_{SUPP1}	Enter supplement mode threshold	V_{BAT} = 3.4 V, V_{OUT} Falling		V_{OUT} ≤ V_{BAT} -0.06		V
V_{SUPP2}	Exit supplement mode threshold	V_{BAT} = 3.4 V, V_{OUT} Rising		V_{OUT} ≥ V_{BAT}-0.02		V
LDO						
V_{LDO}	LDO Output Voltage	V_{IN} = 5.5V, I_{LDO} = 0mA to 50mA	4.7	4.9	5.1	V
I_{LDO}	Maximum LDO Output Current		60			mA
V_{DO}	Dropout Voltage	V_{IN} = 4.5V, I_{LDO} = 50mA		200	300	mV
LOGIC LEVELS ON EN						
V_{IL}	Logic low input voltage				0.4	V
V_{IH}	Logic high input voltage		1.4			V
V_{FLT}	Logic FLOAT input voltage		600	850	1100	mV
$I_{FLT\_leakage}$	Maximum leakage sink or source current to keep in FLOAT				1	µA
I_{EN_DRIVE}	Minimal drive current from an external device for Low or High		8			µA
LOGIC LEVELS ON BGATE						
V_{IL}	Logic LOW input voltage				0.4	V
V_{IH}	Logic HIGH input voltage		1.4			V
BATTERY-PACK NTC MONITOR (TS)						
V_{COLD}	TS Cold Threshold	Temperature falling	24.4	25	25.6	% of V_{LDO}
$V_{HYS(COLD)}$	Hysteresis on Cold threshold	Temperature rising, BGATE disabled		1		% of V_{LDO}
V_{HOT}	TS Hot Threshold	Temperature rising	12	12.5	13	% of V_{LDO}
$V_{HYS(HOT)}$	Hysteresis on Hot Threshold	Temperature falling, BGATE disabled		1		% of V_{LDO}
$t_{dgl(TS)}$	Deglitch for TS Fault	IN or OUT TS Fault		25		ms
$\overline{CHG}$ OUTPUT						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.45	V
I_{IH}	Leakage current	$V_{/CHG}$ = 5 V			1	µA
THERMAL REGULATION						
$T_{J(REG)}$	Temperature Regulation Limit	T_J rising		125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	T_J falling		20		°C

DEVICE INFORMATION

SIMPLIFIED BLOCK DIAGRAM



PIN CONFIGURATION



10-pin 2mm x 3mm SON

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power supply. IN is connected to the external DC supply (AC adapter or USB port). Bypass IN to VSS with at least a 0.1µF ceramic capacitor.
ISET	2	I	Current programming input. Connect a resistor from ISET to VSS to program the input current limit when the user proagammable mode is selected by the EN pin. The resistor range is between 1kΩ and 10kΩ to set the current between 100 mA and 1A.
VSS	3	–	Ground terminal. Connect to the thermal pad and the ground plane of the circuit.
LDO	4	O	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO to VSS with a 0.1µF ceramic capacitor. LDO is enabled when $V_{UVLO} < V_{IN} < V_{OVP}$.
TS	5	I	Battery pack NTC monitoring input. Connect the battery pack NTC from TS to VSS to monitor battery pack temperature. The default pack temperature range is 0°C to 45°C thresholds.
EN	7	I	Enable input. Drive EN high to disable the IC. Connect EN to VSS to place the bq25060 in the user pgrammable mode where the input current is programmed using the ISET input. Leave EN flaoting to place the bq25060 in USB500 mode. See the Charger Enable section for details on using the EN interface.
$\overline{CHG}$	8	O	Charge status indicator open-drain output. $\overline{CHG}$ is pulled low while the device is charging the battery. $\overline{CHG}$ goes high impedance when the battery is fully charged and does not indicate subsequent recharge cycles.
BAT	6	O	Battery connection output. BAT is the sense input for the battery as well as the precharge current output. Connect BAT to the battery and bypass BAT to VSS with a 0.1µF ceramic capacitor.
BGATE	9	I/O	Battery P-Channel FET gate drive output. Connect BGATE to the gate of the external P-Channel FET that connects the battery to OUT. Connect BGATE to VSS if the external FET is not used. No external capacitor is recommended from BGATE to GND.
OUT	10	O	System output connection. OUT supplies the system with a minimum voltage of 3.4V (min.) to ensure system operation whenever an input adapter is connected regardless of the battery voltage. Bypass OUT to VSS with a minimum 1µF ceramic capacitor.
Thermal PAD	Pad	–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

APPLICATION CIRCUITS

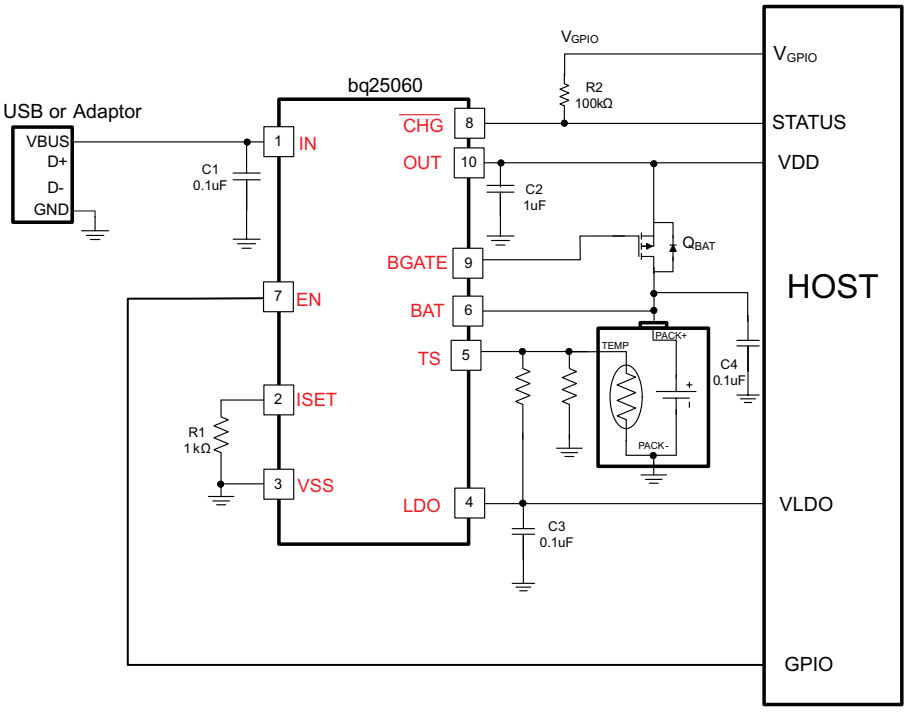


Figure 1. Typical Application Circuit Using the External Power Path Control Feature

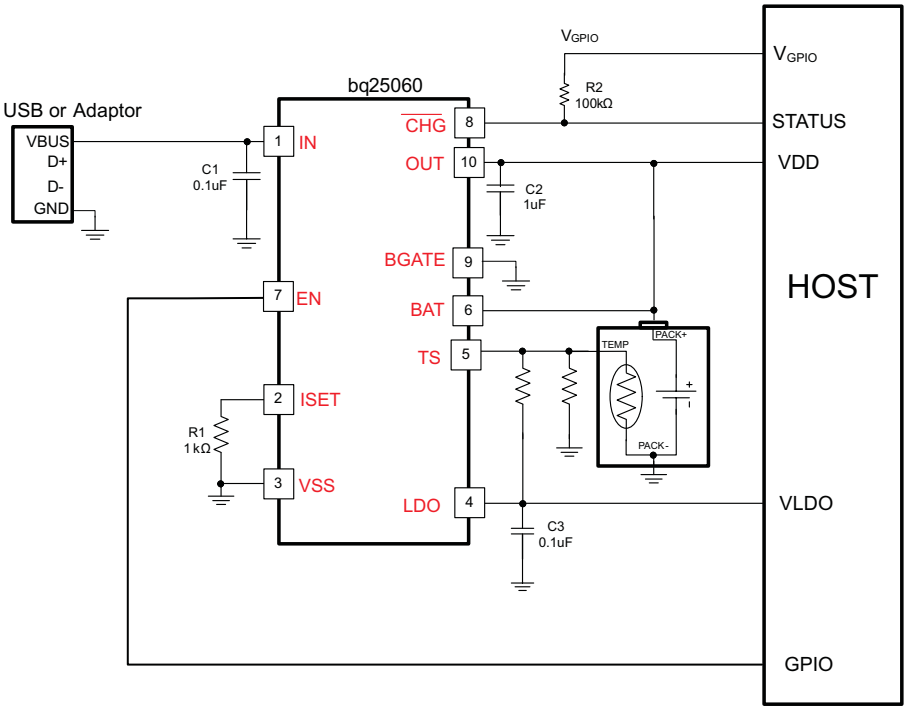


Figure 2. Typical Application Circuit Disabling the External Power Path Control Feature

TYPICAL CHARACTERISTICS

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

ADAPTER INSERTION

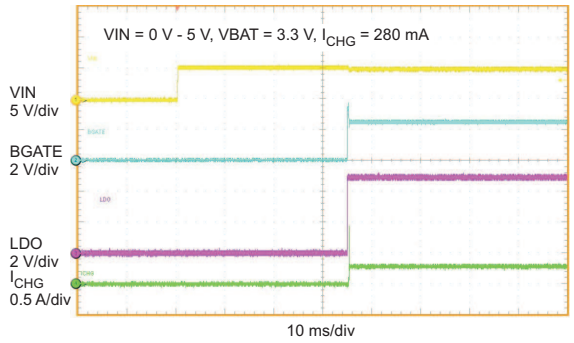


Figure 3.

ENABLE USING EN

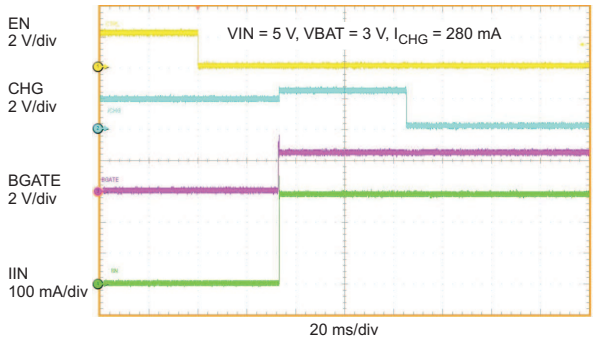


Figure 4.

DISABLE USING EN

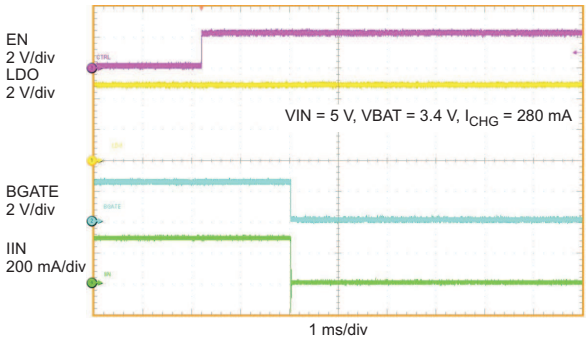


Figure 5.

INPUT OVP

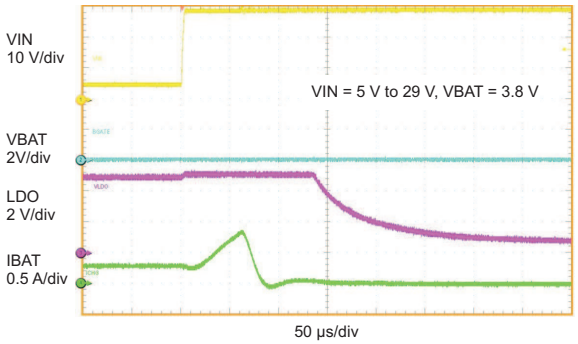


Figure 6.

PRE-CHARGE MODE TO MINIMUM OUTPUT REGULATION MODE

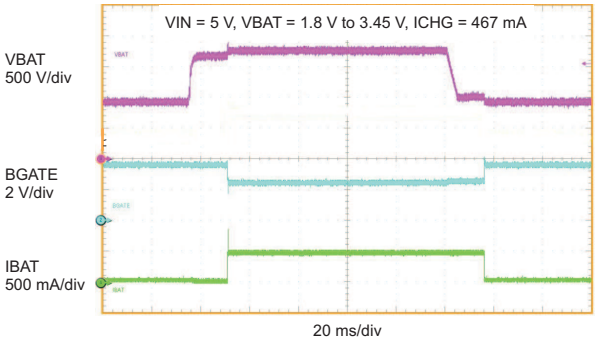


Figure 7.

MINIMUM OUTPUT REGULATION MODE TO CONSTANT CURRENT (CC) MODE

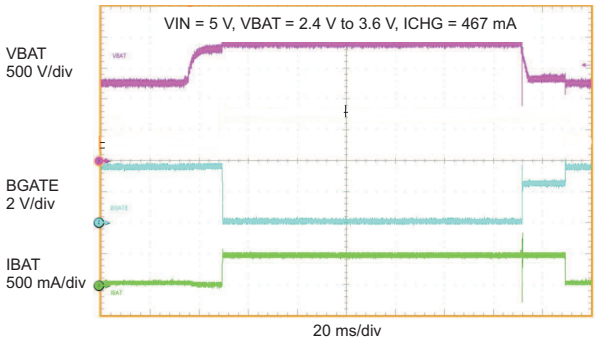


Figure 8.

TYPICAL CHARACTERISTICS (continued)

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

PRE-CHARGE TO CONSTANT VOLTAGE (CV) MODE

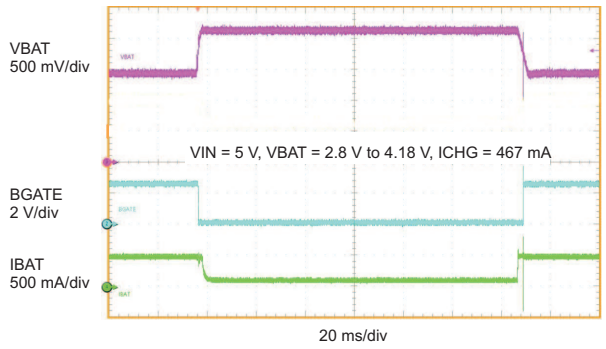


Figure 9.

VIN-DPM

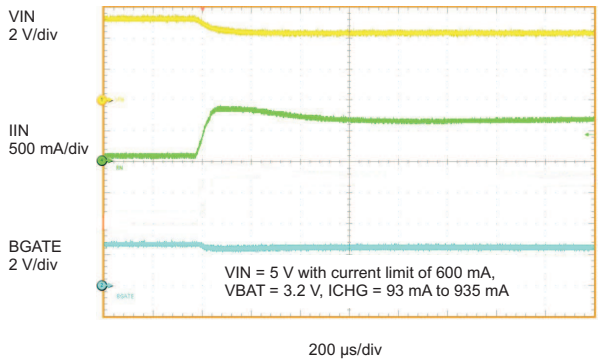


Figure 10.

SUPPLEMENT MODE

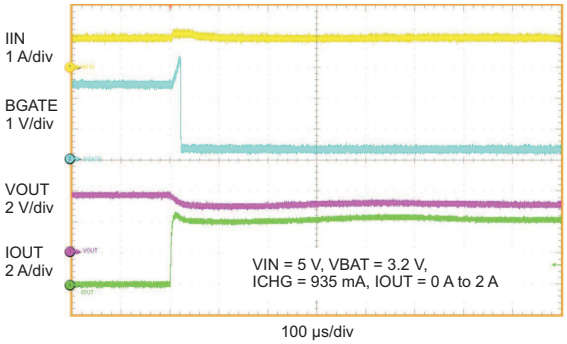


Figure 11.

CHARGE CYCLE DEMO

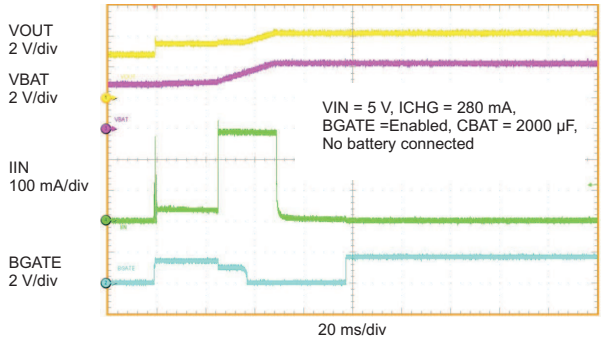


Figure 12.

BATTERY VOLTAGE vs CHARGE CURRENT

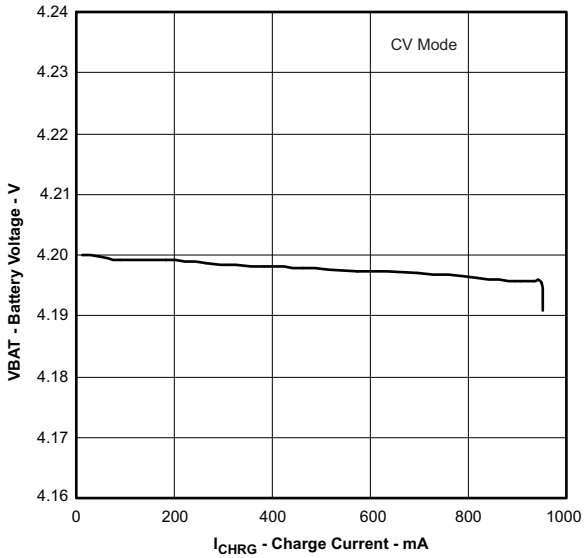


Figure 13.

R_{DSON} (From IN to OUT) vs JUNCTION TEMPERATURE

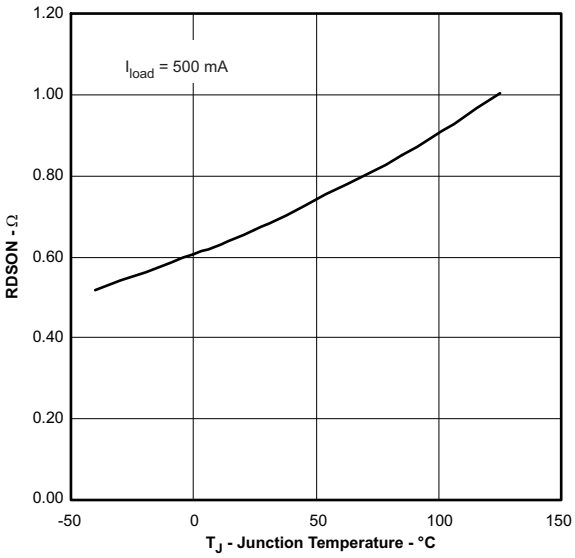


Figure 14.

TYPICAL CHARACTERISTICS (continued)

Using circuit in Figure 1, T_A = 25°C, unless otherwise specified

INPUT CURRENT LIMIT vs INPUT VOLTAGE

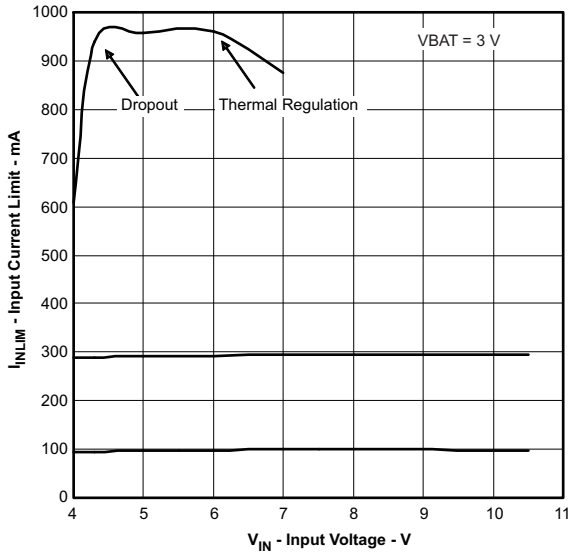


Figure 15.

OUTPUT VOLTAGE vs CHARGE CURRENT

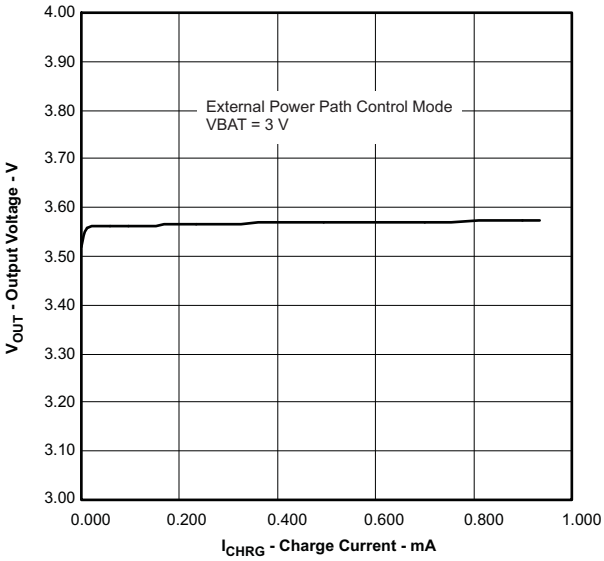


Figure 16.

DETAILED FUNCTIONAL DESCRIPTION

The bq25060 is a highly integrated Li-Ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC Adapter and charges a single-cell Li-Ion battery with up to 1A of charge current. The 30V input voltage range with input over-voltage protections supports low-cost unregulated adapters.

The bq25060 has a single power output that charges the battery. The system load is connected to OUT. The low-battery system startup circuitry maintains OUT pin voltage at $V_{OUT(REG)}$ whenever an input source is connected. This allows the system to start-up and run whenever an input source is connected regardless of the battery voltage. The charge current is programmable up to 1A using the EN input. Additionally, a 4.9V 50mA LDO is integrated into the IC for supplying low power external circuitry.

External FET Controller (BGATE)

The External Power Path Control feature is implemented using the BGATE output. BGATE is also used to enable/ disable the External Power Path Control feature. When power is first applied to either V_{BAT} or V_{IN} on the bq25060, the BGATE output is tested. If the BGATE pin is connected to VSS, the External Power Path Control feature is disabled. In order to enable the External Power Path Control feature after it has been disabled, the battery and the input source must be removed and reconnected and BGATE must NOT be connected to VSS.

With External Power Path Control enabled, BGATE is used to drive an external P-channel FET that connects the battery to the system output. The state of this FET is dependant on the battery voltage and the IC status. In discharge mode, BGATE is pulled to GND to turn the external FET on fully. During discharge mode, the output is connected directly to the battery. Discharge mode is entered under the following conditions:

1. IC disabled or no input power
2. Supplement mode

When not in one of these conditions, the BGATE output is controlled by the bq25060 and changes depending on which mode is required. See the *Charging Operation* section for more details.

Enable/ Disable External Power Path Control

When power is first applied to the bq25060, either at the IN or BAT input, the bq25060 checks the BGATE output. The device sources a small current out of BGATE for 2ms and monitors the voltage. If VBGATE is connected to ground and the voltage does not rise above logic High, the External Power Path Control feature is disabled and VLOWV is set to 2.5V. If the BGATE voltage rises above logic High, the External Power Path Control feature is enabled and V_{LOWV} is set to 2.9V. The bq25060 only does this check when power is initially applied. Power must removed from IN and BAT and then reapplied to initiate another check. Figure 17 illustrates the startup check procedure.

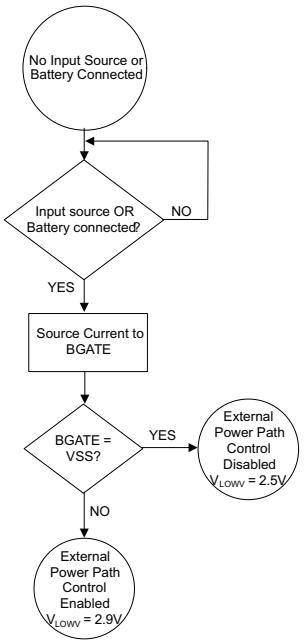


Figure 17. BGATE Monitor Sequence

Charging Operation

The bq25060 charges a battery in 3 stages while maintaining a minimum system output. When the bq25060 is enabled by EN, the battery voltage is monitored to verify which stage of charging must be used. The bq25060 charges in precharge mode, minimum output regulation mode, or normal CC/CV mode based on the battery voltage.

Charger Operation with External Power Path Control Mode Enabled

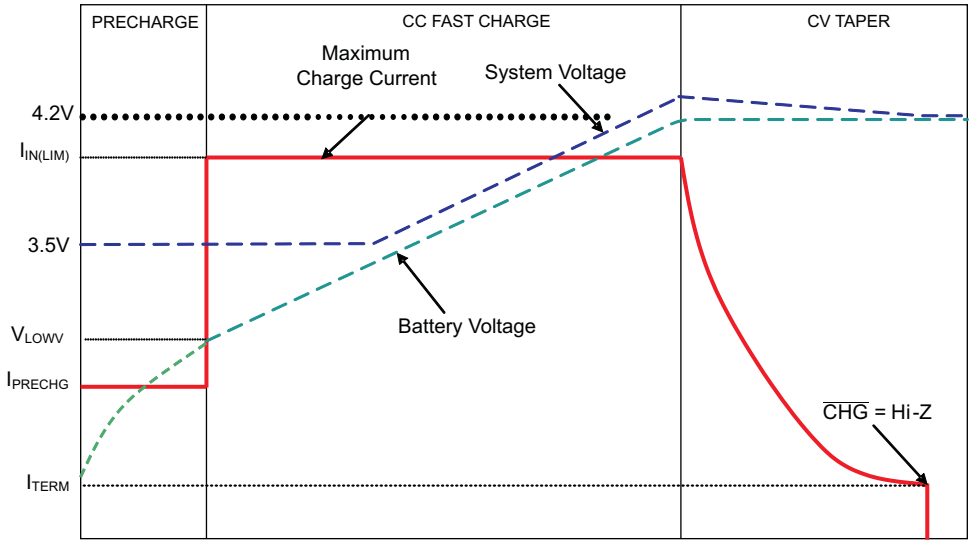


Figure 18. Typical Charging Cycle with External Power Path Control Enabled

Precharge Mode ($V_{BAT} \le V_{LOWV}$)

The bq25060 enters precharge mode when $V_{BAT} \le V_{LOWV}$. Upon entering precharge mode, the battery is charged with a 40mA current source and /CHG goes low. During precharge mode, V_{OUT} is regulated to 3.5V and the battery is charged from the internal fixed 40mA current source connected to the BAT output. With BGATE connected to GND, the system output is connected to the battery and therefore the system voltage is equal to the battery voltage.

Minimum Output Regulation Mode ($2.9V<V_{BAT}<3.6V$)

Once VBAT exceeds 2.9V, the bq25060 enters Minimum Output Regulation Mode. While $2.9V<V_{BAT}<3.6V$, V_{OUT} is regulated to $V_{OUT(REG)}$ by the external FET (QBAT) while the internal FETs between IN and OUT is used to regulate the fast charge current. The total current is shared between the output load and the battery. As the system current increases, the battery charge current decreases. In order to maintain the minimum output regulation voltage $V_{OUT(REG)}$, the system load must be less than the input current limit.

Normal CC/CV Mode

Once $V_{BAT}>3.6V$, QBAT is fully turned on and $V_{OUT} = V_{BAT} + V_{drop(Q1)}$. At this point, the bq25060 is in constant current (CC) mode where charge current is regulated using the internal FETs between IN and OUT. The V_{OUT} voltage is not regulated. The total current is shared between the output load and the battery. Once the battery voltage charges up to $V_{BAT(REG)}$, the bq25060 enters constant voltage (CV) mode where V_{BAT} is regulated to VBAT(REG) and the current is reduced. Once the input current falls below the termination threshold (I_{TERM}) BGATE is turned off and $\overline{CHG}$ goes high impedance. The system output is regulated to 4.2V and the battery is disconnected from OUT, however supplement mode is still available.

Charger Operation With External Power Path Control Mode Disabled (BGATE = VSS)

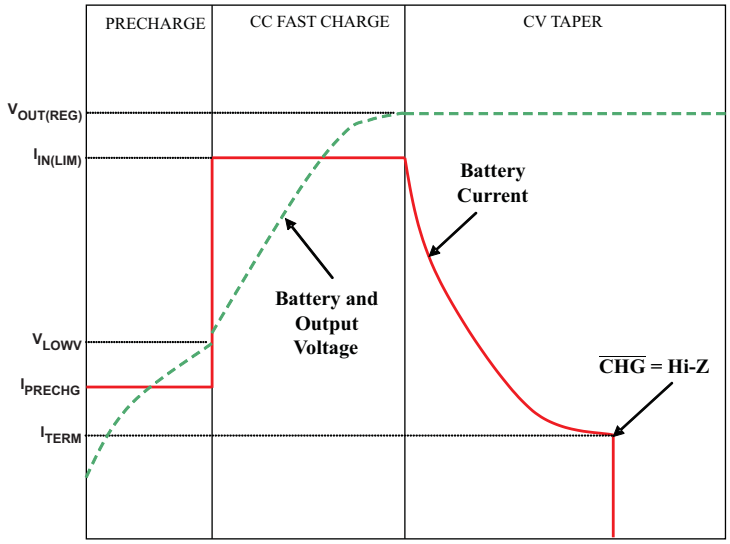


Figure 19. Charging Cycle with External Power Path Control Disabled (BGATE = VSS)

Precharge Mode ($V_{BAT} \le V_{LOWV}$)

The bq25060 enters precharge mode when $V_{BAT} \le V_{LOWV}$. Upon entering precharge mode, $\overline{CHG}$ goes low and the input current limit is set to $I_{PRECHARGE}$. With BGATE connected to GND, the system output is connected to the battery and therefore the system voltage is equal to the battery voltage. During precharge mode, the input current is regulated to 50mA and as such, only loads up to 50mA are supported.

Normal CC/CV Mode

Once $V_{BAT} > V_{LOWV}$, the bq25060 enters constant current (CC) mode where charge current is regulated using the internal MOSFETs between IN and OUT. The total current is shared between the output load and the battery. Once the battery voltage charges up to VBAT(REG), the bq25060 enters constant voltage (CV) mode where V_{BAT} is regulated to VBAT(REG) and the current is reduced. Once the input current falls below the termination threshold (I_{TERM}), $\overline{CHG}$ goes high impedance but the system remains charging and regulates the output to $V_{BAT(REG)}$.

Programmable Input Current Limit (ISET)

When the charger is enabled, and the user programmable current limit is selected by the EN input, internal circuits generate a current proportional to the input current at the ISET input. The current out of ISET is 1/1000 (±10%) of the charge current. This current, when applied to the external charge current programming resistor, R1 (Figure 1), generates an analog voltage that is regulated to program the fast charge current. Connect a resistor from ISET to VSS to program the input current limit using the following equation:

$$I_{IN\_LIMIT} = \frac{K_{ISET}}{R_{ISET}} = \frac{1000A \times \Omega}{R_{ISET}} \quad (1)$$

IIN_LIM is programmable from 100mA to 1A. The voltage at ISET can be monitored by an external host to calculate the charging current to the battery. The input current is related to the ISET voltage using the following equation:

$$I_{IN} = V_{ISET} \times \frac{1000}{R_{ISET}} \quad (2)$$

Monitoring the ISET voltage allows for the host to calculate the actual charging current and therefore perform more accurate termination. The input current to the system must be monitored and subtracted from the current into the bq25060 which is show by VISET.

Input Current Limit Control (EN)

The bq25060 contains a 3-state that controls the input current limit. Drive EN low to program the input current limit to the user defined value programmed using ISET. Drive EN high to place the bq25060 in USB suspend mode. In USB suspend mode, the input current into bq25060 is reduced and the external battery FET is held on (BGATE pulled to GND). Leaving EN unconnected or connected to a high impedance source programs the USB500 input current limit.

Table 1. EN Input Definition

EN	MODE
Low	ISET
Hi-Z	USB500
Hi	USB Suspend

Input Over Voltage Protection

The bq25060 contains an input over voltage protection circuit that disables the LDO output and charging when the input voltage rises above V_{OVP}. This prevents damage from faulty adapters. The OVP circuitry contains an deglitch that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than V_{OVP} is plugged in, the IC completes power up and then shuts down if the voltage remains above V_{OVP} after the deglitch. The LDO remains off and charging remains disabled until the input voltage falls below V_{OVP}.

Under-Voltage Lockout (UVLO)

The bq25060 remains in power down mode when the input voltage is below the under-voltage lockout threshold (VUVLO). During this mode, the control input (EN) is ignored. The LDO, the charge FET connected between IN and OUT are off and the status output ($\overline{CHG}$) is high impedance. Once the input voltage rises above V_{UVLO}, the internal circuitry is turned on and the normal operating procedures are followed.

Input DPM Mode (V_{IN}-DPM)

The input current into the bq25060 includes all load currents, i.e. the system load, LDO load, and battery charge current. The total input current is regulated by the input current limit of the bq25060. The bq25060 utilizes the V_{IN}-DPM mode for operation from current-limited input sources.

WIth V_{IN}-DPM enabled, the input voltage is monitored. If V_{IN} falls to $V_{IN\text{-}DPM}$, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq25060 from crashing poorly designed or incorrectly configured USB sources. Figure 20 shows the V_{IN}-DPM behavior to a current limited source. In this figure the input source has a 200mA current limit and the device has started up with the 285mA current limit.

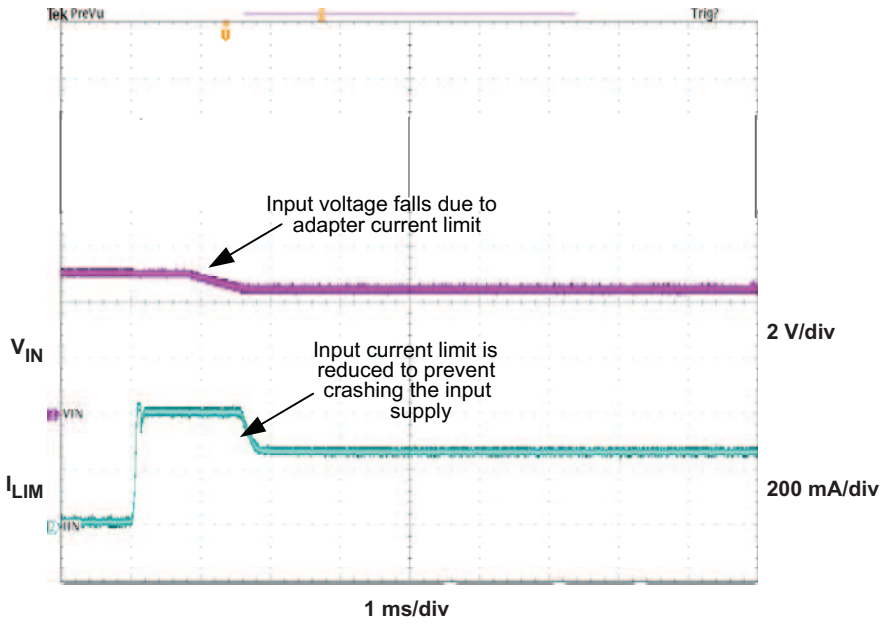


Figure 20. bq25060 V_{IN}-DPM

External NTC Monitoring (TS)

The bq25060 features a flexible, voltage based external battery pack temperature monitoring input. The TS input connects to the NTC thermistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions. During charging, the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (VCOLD to VHOT), charging is suspended. When the voltage measured at TS returns to within the operation window, charging is resumed. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ output goes to high impedance.

The temperature thresholds are programmed using a resistor divider from LDO to GND with the NTC thermistor connected to the center tap from TS to GND. See Figure 5 for the circuit example. The value of R1 and R2 are calculated using the following equations:

$$R1 = \frac{-R2 \times RHOT \times (0.125 - 1)}{0.125 \times (R2 + RHOT)} \quad (3)$$

$$R2 = \frac{-RHOT \times RCOLD \times (0.125 - 0.250)}{RHOT \times 0.250 \times (0.125 - 1) + RCOLD \times 0.125 \times (1 - 0.250)} \quad (4)$$

RHOT is the expected thermistor resistance at the programmed hot threshold; RCOLD is the expected thermistor resistance at the programmed cold threshold.

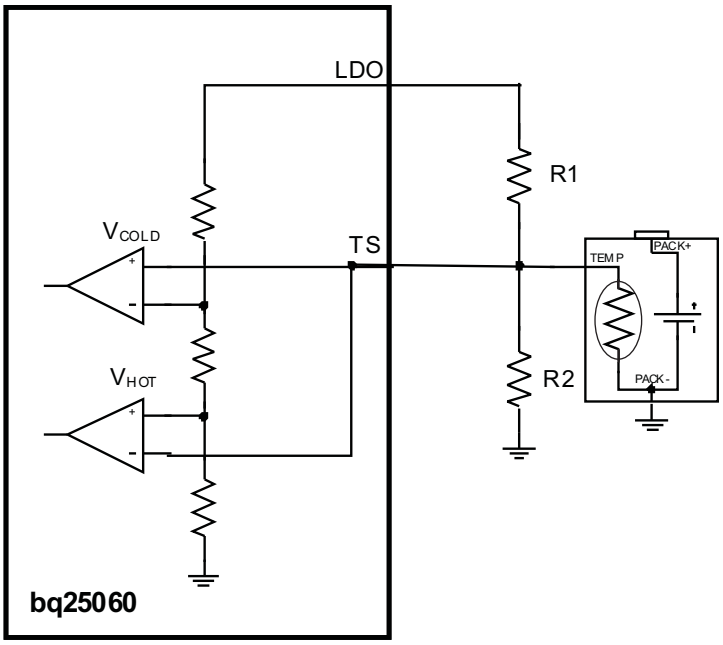


Figure 21. NTC Monitoring Function

50mA LDO (LDO)

The LDO output of the bq25060 is a low dropout linear regulator (LDO) that supplies up to 50mA while regulating to VLDO. The LDO is active whenever the input voltage is above VUVLO and below VOVP. It is not affected by the EN input. The LDO output is used to power circuitry such as USB transceivers in dead battery conditions. This allows the user to operate the product immediately after plugging the adapter in, instead of waiting for the battery to charge to useable levels.

Charge Status Indicator ($\overline{CHG}$)

The bq25060 contains an open drain $\overline{CHG}$ output that indicates charge cycles and faults. When charging a battery in precharge, fastcharge, or CV mode, the $\overline{CHG}$ output is pulled to VSS. Once the BAT output reaches regulation and the charge current falls below the termination threshold, $\overline{CHG}$ goes to high impedance to signal the battery is fully charged. The $\overline{CHG}$ output goes low during battery recharge cycles to signal the host to monitor for termination.

Additionally, $\overline{CHG}$ notifies the host if a NTC temperature fault has occurred. $\overline{CHG}$ goes to high impedance if a TS fault occurs. Connect $\overline{CHG}$ to the required logic level voltage through a 1kΩ to 100kΩ resistor to use the signal with a microprocessor. $I_{\overline{CHG}}$ must be below 5mA.

Thermal Regulation and Thermal Shutdown

The bq25060 contains a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high V_{IN} conditions. If the die temperature increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25060. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm.

APPLICATION INFORMATION

Selection of Input/ Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 0.1µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25060 requires a capacitor from OUT to GND for loop stability. Connect a 1µF ceramic capacitor from OUT to GND close to the pins for best results. More output capacitance may be required to minimize the output droop during large load transients. Connect a 0.1µF ceramic capacitor from BAT to GND to eliminate the potential ESD strike.

The LDO also requires an output capacitor for loop stability. Connect a 0.1µF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

bq25060 Charger Design Example

The following sections provide an example for determining the component values for use with the bq25060.

Requirements: Refer to Figure 1 and Figure 2 for Schematics of the Design Example.

- Supply voltage = 4.35~10.2V
- Input current limit is 0.5A
- Set 0°C~45°C operating range

Calculations

Input Current Limit Control (EN): Drive EN low to program the input current limit to the user defined value programmed using ISET. See Table 1 for other detail EN pin options.

Program the input current limit (ISET): Connect a resistor, RISET, from ISET to VSS to program the input current. The RISET is determined by:

$$R_{ISET} = \frac{K_{ISET}}{I_{IN\_LIMIT}} = \frac{1000A \times \Omega}{I_{IN\_LIMIT}} = 2000\Omega \quad (5)$$

Set 0°C to 45°C charger operating temperature range (TS): The value of R1 and R2 are:

$$R2 = \frac{-RHOT \times RCOLD \times (0.125 - 0.250)}{RHOT \times 0.250 \times (0.125 - 1) + RCOLD \times 0.125 \times (1 - 0.250)} = 11.3k\Omega \quad (6)$$

$$R1 = \frac{-R2 \times RHOT \times (0.125 - 1)}{0.125 \times (R2 + RHOT)} = 24.0k\Omega \quad (7)$$

RHOT: 4.911kΩ, the resistor value of Semitec NTC 103AT-2 at 45°C;

RCOLD: 27.28kΩ, the resistor value of Semitec NTC 103AT-2 at 0°C.

External FET Controller (BGATE): On Figure 1, BGATE drives an external P-channel FET that connects the battery to the system output. When power is first applied to either VBAT or VIN, the device sources a typical 50µA small current out of BGATE and monitors the voltage. If BGATE voltage is higher than logic high in first 1ms and stays high for at least 2ms, the external power path control feature is enabled and VLOWV is set to 2.9V. The OUT pin maintains voltage at VOUT(REG).

In Figure 2, BGATE is connected to Vss. The external power path control feature is disabled and VLOWV is set to 2.5V. The OUT pin shorts to BAT.

Status Indicators (CHG): The CHG pin is open drain output. If used, CHG pin should be pulled up via a resistor and possibly a LED to a power source. If monitored by a host, the host pull-up power source should be used.

Thermal Considerations

The bq25060 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (8)$$

Where:

T_J = chip junction temperature
T_A = ambient temperature
P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (9)$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile, Figure 18. If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25060, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25060 is packaged in a thermally enhanced SON package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25060DQCR	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN
BQ25060DQCR.A	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN
BQ25060DQCR.B	Active	Production	WSON (DQC) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN
BQ25060DQCT	Active	Production	WSON (DQC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN
BQ25060DQCT.A	Active	Production	WSON (DQC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN
BQ25060DQCT.B	Active	Production	WSON (DQC) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DAN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

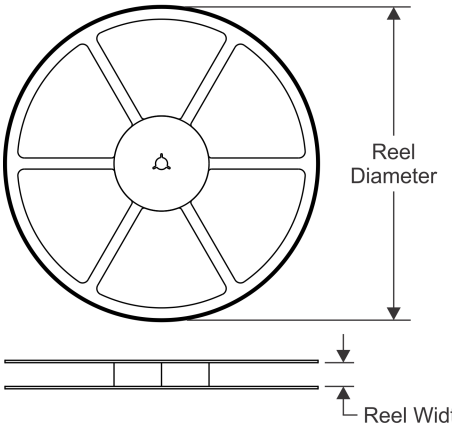
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

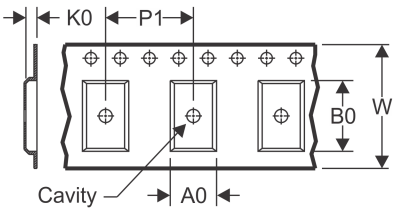
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

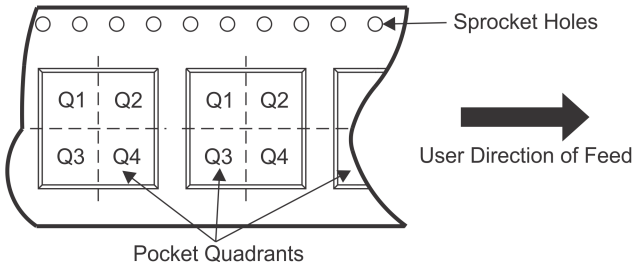


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

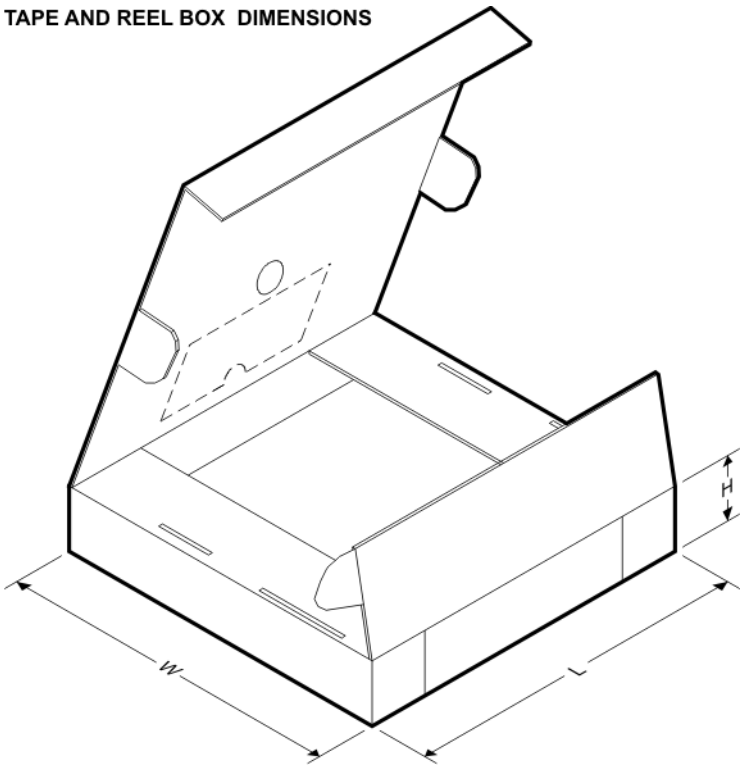
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25060DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ25060DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



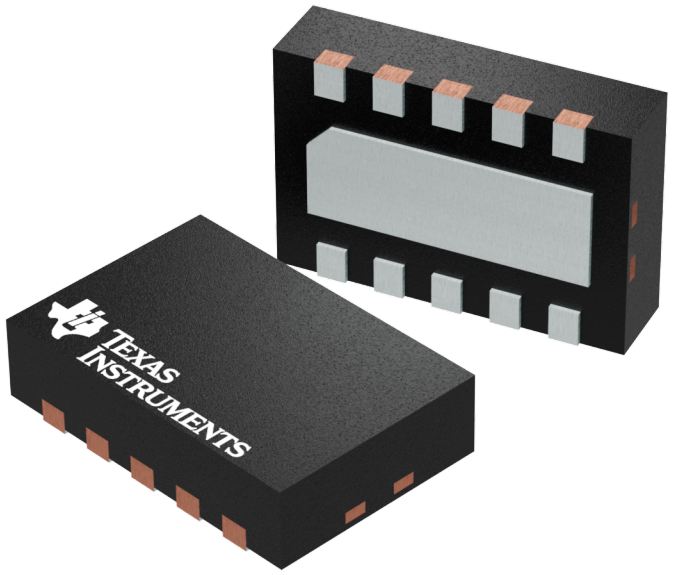
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25060DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
BQ25060DQCT	WSON	DQC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

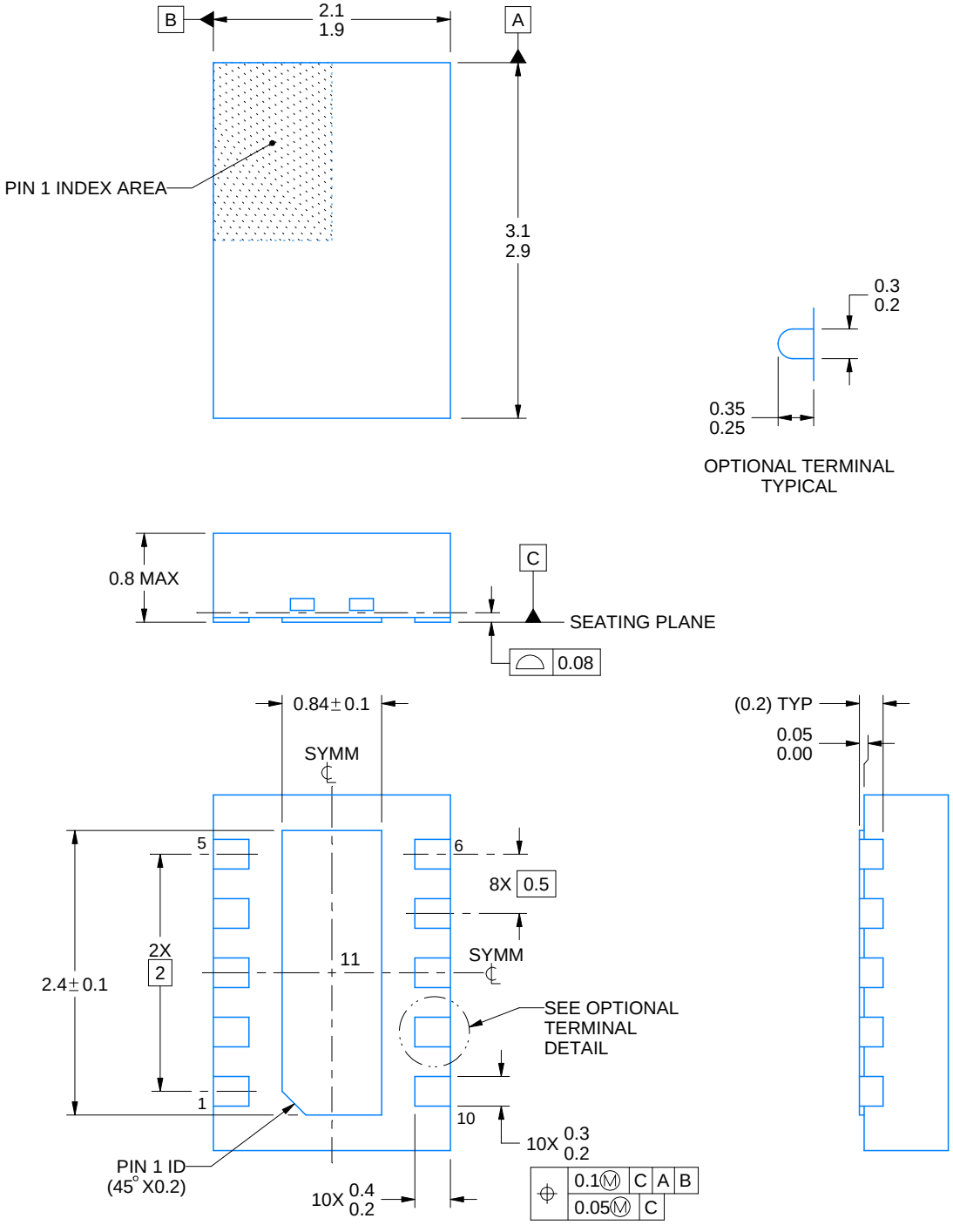
4209674/B

PACKAGE OUTLINE

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

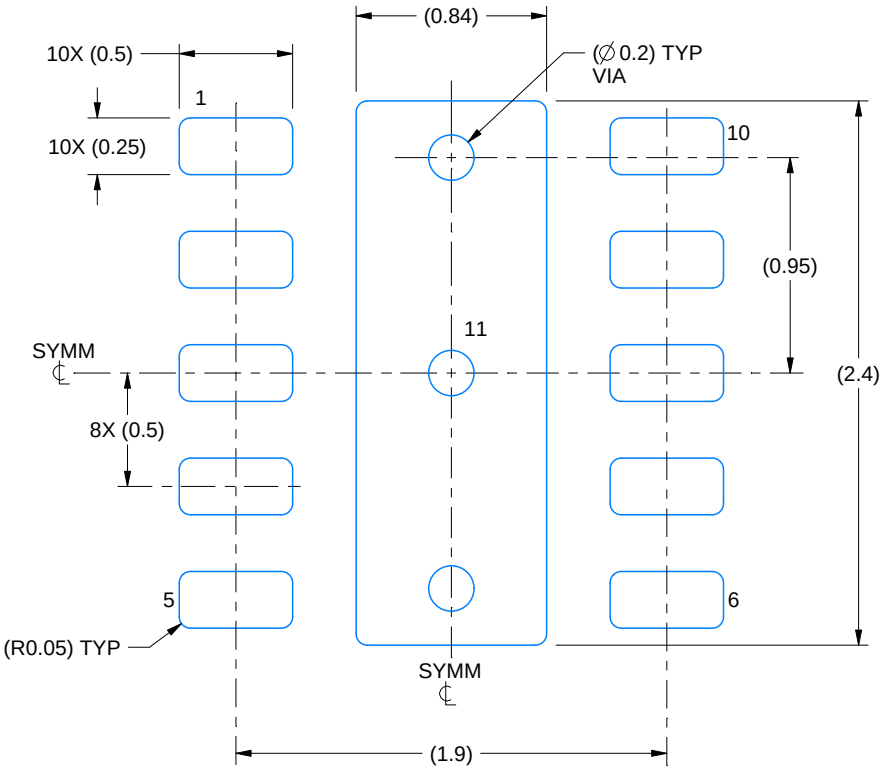
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

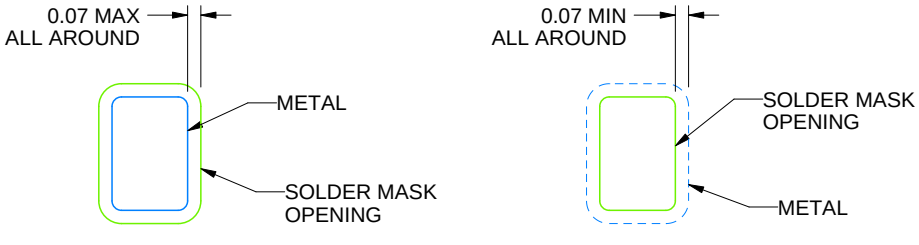
DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

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NOTES: (continued)

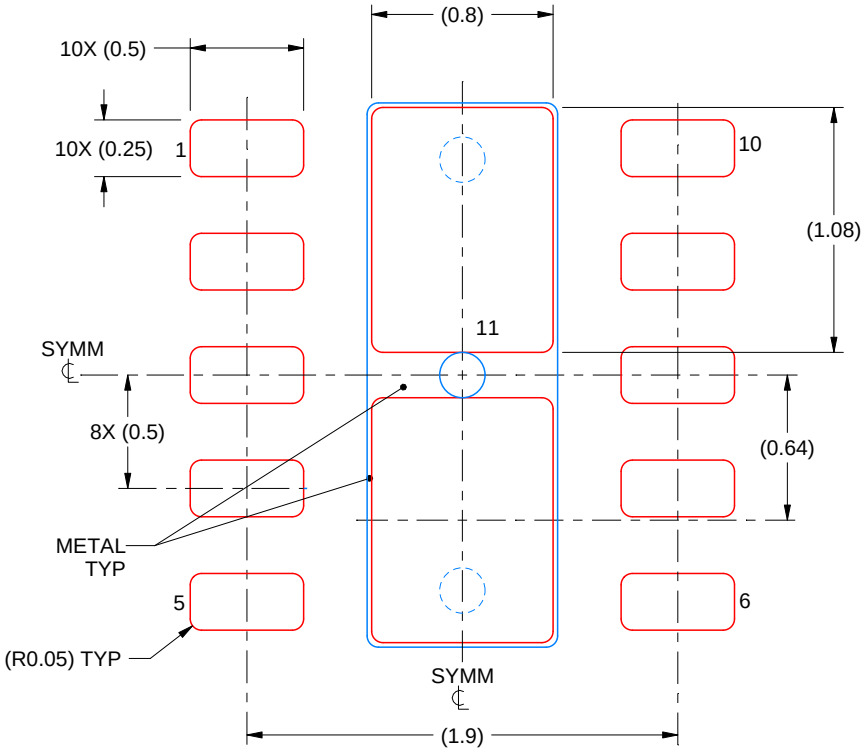
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025