Low-cost solution for measuring input power and RMS current

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Introduction

Real-time measurement of energy consumption, including measurement of real input power and input RMS current for off-line power supplies, is becoming ever more important nowadays. These measurements can be used to adjust power delivery and optimize energy usage. More specifically, data centers, which contain many servers, are interested in submetering at the server level to implement low-cost data services and intelligently manage power processing during lower-power operation. The usual method of measuring input power and current uses a dedicated power-metering chip and an extra sensing circuit. While the power-metering chip provides acceptable results, it significantly increases the cost and design effort. This article provides a novel, low-cost but accurate solution for measuring input power and RMS current. It utilizes the existing digital power-factor-correction (PFC) control chip and hardware, with simple two-point calibration and optimized mathematical calculations. This provides excellent measurement accuracy and greatly reduces the cost and design effort, while having no impact on normal PFC control.

Measurement setup

Figure 1 shows a conventional PFC setup controlled by a digital controller for isolated power. The input line and neutral voltages are both sensed through an attenuation network and are subsequently sampled by two separate analog-to-digital-converter (ADC) inputs. The current signal is sensed by a current shunt and is amplified and filtered by a signal-

conditioning circuit. It is then connected to an ADC for current-loop control. Since the input voltage and current measurements are already available, they can be used to measure the input power and RMS current as well. The same conventional PFC setup is used for these measurements. The traditional dedicated powermetering chip and extra sensing circuit are eliminated.

Current measurement and calibration

The current-sense signal-conditioning circuit (Figure 1) normally consists of an operational amplifier and a low-pass filter to amplify the small sensed signal and remove high-frequency noise. The signal is then measured by an ADC and reported in ADC counts. To get the real current value, the ADC counts need to be translated back to current in amperes. The relationship between ADC counts and amperes can be derived from the schematic; however, the component tolerances could make the measurement accuracy unacceptable. Therefore, a calibration is needed.

Given the circuit in Figure 1, at any moment the input current through the current shunt in milliamperes is

$$i = k_i C_i - m_i, \tag{1}$$

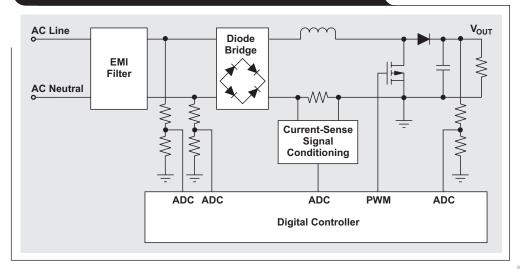
where k_i is the current-sense gain or slope, C_i is the ADC-conversion output (count), and m_i is the current-sense offset

For constant direct-current (DC) input, the average value equals the instantaneous value, so Equation 1 is still valid:

$$I_{DC} = k_i C_i - m_i$$
 (2)

Equation 2 indicates that a DC source can be used to calibrate the current-measurement circuit. A constant DC power is applied to the PFC input, and measurements are taken with a 25% load and then a 75% load. For comparison, a meter is used to provide benchmark measurements of actual input current for both load conditions. The count output of the ADC conversion is also read for both load

Figure 1. PFC setup for measuring input power and current



conditions to determine the accuracy of the digital controller. The controller uses the following mathematical relationships. For a 25% load,

$$I_{DC1} = k_i C_{i1} - m_i$$
. (3)

For a 75% load,

$$I_{DC2} = k_i C_{i2} - m_i$$
. (4)

The current slope and offset can be calculated from Equations 3 and 4:

$$k_{i} = \frac{I_{DC2} - I_{DC1}}{C_{i2} - C_{i1}}$$
 (5)

$$m_{i} = \frac{C_{i1}I_{DC2} - C_{i2}I_{DC1}}{C_{i2} - C_{i1}}$$
 (6)

The calculated k_i and m_i are decimals and could be less than 1, while most of the digital controllers in PFC applications use a fixed point in mathematical calculation. To reduce the rounding errors and maintain enough accuracy in the calculations, the small decimal values are multiplied by $2^{\rm N}$ and then rounded to the closest integer. For example, if the current-sense gain and offset for a PFC circuit are calculated as $k_i=1.59$ and $m_i=229.04$, then k_i will be multiplied by $2^{\rm N}$ and rounded to 407; and m_i will be multiplied by $2^{\rm N}$. The current slope and offset will respectively be

and

$$m_i = iin offset >> iin offset shift,$$

where iin_slope = 407, iin_slope_shift = 8, iin_offset = 229, and iin_offset_shift = 0.

When the input power and RMS current are calculated, if k_i and m_i are multipliers, then instead of using them directly, one can use iin_slope and iin_offset to do multiplication first. Then the result is right shifted by iin_slope_ shift and iin_offset_shift. For example, instead of the calculation $y = k_i \times x + m_i \times z$, the following can be used:

$$\begin{aligned} y &= [(iin_slope \times x) >> iin_slope_shift] \\ &+ [(iin_offset \times z) >> iin_offset_shift] \end{aligned}$$

Input-voltage measurement and calibration

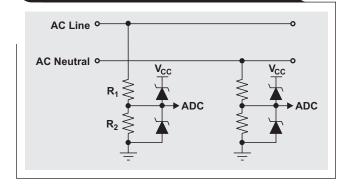
The voltage-sense circuit is quite simple and can be just a voltage divider, as shown in Figure 2. Usually there are clamp diodes to protect the ADC pins. Since the reverse leakage current of the diodes affects the ADC's measurement accuracy, diodes with low reverse leakage current should be chosen.

At any moment, the input voltage is

$$v = k_v C_v - m_v, \tag{7}$$

where k_v is the voltage-sense gain, C_v is the ADC-conversion output (count), and m_v is the voltage-sense offset. k_v and m_v can be calibrated in a way similar to calibrating the current-sense gain and offset. However, a much simpler way is to just calculate from the schematic. Since there is no calibration, the accuracy of the resistance

Figure 2. Voltage-sense circuit for AC input



used for the voltage divider affects measurement accuracy. Using low-tolerance resistors as the voltage divider is recommended—for example, 0.1% tolerance.

For a digital controller with a 12-bit ADC and referenced to 2.5 V, the input voltage is attenuated by the voltage divider to a magnitude of less than 2.5 V. Then the attenuated signal is converted to a digital signal by the ADC. Therefore,

$$C_{\rm v} = \frac{{\rm vR}_2}{2.5({\rm R}_1 + {\rm R}_2)} \times 4096.$$
 (8)

By rearranging Equation 8, the input voltage can be calculated as

$$v = \frac{2.5(R_1 + R_2)}{4096R_2} \times C_v.$$
 (9)

Therefore,

$$k_{v} = \frac{2.5(R_1 + R_2)}{4096R_2},$$
 (10)

and

$$m_{v} = 0.$$
 (11)

Similar to the input-current measurement, the voltagesense gain and offset need to be manipulated to accommodate a fixed-point microprocessor and to reduce the calculation error.

V_{IN} and I_{IN} correlation

Real input power is defined as

$$P = \frac{1}{T} \int_0^T v(t)i(t)dt.$$
 (12)

In discrete format, it is defined as

$$P = \frac{\sum [v(n)i(n)]}{N},$$
 (13)

where N is the total number of samples. Equation 13 indicates that V_{IN} and I_{IN} need to be sampled at the same time. However, V_{IN} and I_{IN} are sampled at different times by two different ADC channels. Even the small time discrepancy can contribute to a measurement error. In some

digital controllers, such as the Texas Instruments UCD3138, a mechanism called *dual sample-and-hold* is provided that allows these two channels to be sampled simultaneously, eliminating this error.

Due to the low-pass filter used in the current-sense circuit, the measured current signal is delayed and out of phase with the actual current. This is shown in Figure 3, where Channel 2 is the actual current signal; and Channel 1 is the same signal amplified, which then comes out of the low-pass filter. The amplified signal has a phase delay of about 220 μs . This delay needs to be compensated for; otherwise it will affect the accuracy of the input-power measurement. A simple way to compensate is to delay the V_{IN} -sense signal by about 220 μs , then use the delayed V_{IN} signal to do an input-power calculation. So if V_{IN} is measured every 20 μs , it needs to be delayed by 220/20 = 11 times.

Calculating real input power

Combining Equations 1, 7, and 13 yields

$$P = \frac{k_v k_i \sum C_v(n) C_i(n)}{N} - \frac{k_v m_i \sum C_v(n)}{N}$$
$$- \frac{k_i m_v \sum C_i(n)}{N} + m_v m_i.$$
(14)

 $V_{\rm IN}$ and $I_{\rm IN}$ are measured by ADCs in the standard interrupt loop, which has a limited time period and is mainly used for PFC loop control. Therefore, to save CPU calculation time and prevent overflow in the standard interrupt loop, only $C_{\rm v}(n)C_{\rm i}(n)$ is calculated in this loop. Also, the terms

$$\frac{\sum C_v(n)C_i(n)}{N}$$
, $\frac{\sum C_v(n)}{N}$, and $\frac{\sum C_i(n)}{N}$

from Equation 14 are implemented with infinite impulse response (IIR) filters. The final calculation of real input power is done in the background loop.

Calculating input RMS current

The current measurement by the digital controller in Figure 1 does not represent the total input current, since the contribution of the capacitance in the electromagnetic-interference (EMI) filter is not included. At high line voltage and light load, this filter current is not negligible any more and must be included for accurate input-current reporting.

Figure 4 shows a simplified EMI filter where the inductors are removed and the total capacitance is replaced with a single capacitor (C). In this figure, $I_{\rm EMI}$ is the RMS reactive current of the EMI capacitor, $I_{\rm Measure}$ is the input RMS current measured by the digital controller, and $I_{\rm IN}$ is the total input RMS current.

The reactive current produced by the EMI filter is

$$I_{EMI} = 2\pi f CV_{IN(RMS)}.$$
 (15)

To calculate the reactive current of the EMI capacitor, the input-voltage frequency first needs to be determined. The AC line and neutral voltage are sensed by two ADC channels and then rectified by firmware. The zero crossing is

Figure 3. Current-sense phase shift

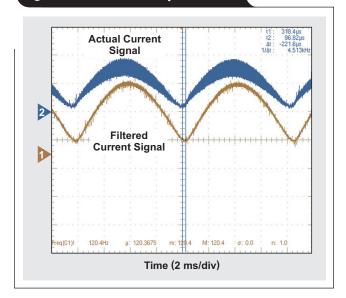
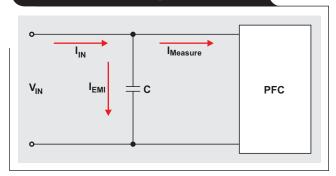


Figure 4. Current in simplified EMI filter



found by comparing the two ADC results. Since the input voltage is sampled at a fixed rate, the AC frequency can be calculated by counting the number of samples between two consecutive zero-crossing points. Once the input-voltage frequency is known, the reactive current of the EMI capacitor is calculated as

$$I_{EMI} = 2\pi f C \sqrt{\frac{k_v^2 \sum C_v^2(n)}{N} - \frac{2k_v m_v \sum C_v(n)}{N} + m_v^2}.$$
 (16)

As stated earlier, the voltage is measured in the standard interrupt loop; so, to save CPU calculation time and prevent overflow in this loop, only $C_v^2(\mathbf{n})$ is calculated in it. The terms

$$\frac{\sum C_v^2(n)}{N}$$
 and $\frac{\sum C_v(n)}{N}$

from Equation 16 are implemented with IIR filters. The final EMI reactive current is calculated in the background loop.

The current measured by the ADC is defined as

$$I_{\text{Measure(RMS)}} = \sqrt{\frac{1}{T} \int_{0}^{T} i(t)^{2} dt}.$$
 (17)

In discrete format, it is defined as

$$I_{\text{Measure(RMS)}} = \sqrt{\frac{\sum i_{\text{IN}}(n)^2}{N}}.$$
 (18)

Combining Equations 1 and 18 leads to

$$I_{\text{Measure(RMS)}} = \sqrt{\frac{k_i^2 \sum C_i^2(n)}{N} - \frac{2k_i m_i \sum C_i(n)}{N} + m_i^2}.$$
 (19)

As stated earlier, the current is measured in the standard interrupt loop; so only $\mathrm{C}^2_i(n)$ is calculated in this loop. The terms

$$\frac{\sum C_i^2(n)}{N}$$
 and $\frac{\sum C_i(n)}{N}$

from Equation 19 are implemented with IIR filters.

Finally, the EMI filter's reactive current (I_{EMI}) is added to $I_{Measure(RMS)}$ to get the total input current. I_{EMI} leads the measured current ($I_{Measure(RMS)}$) by 90°; therefore,

$$I_{\text{IN(RMS)}} = \sqrt{I_{\text{EMI}}^2 + I_{\text{Measure(RMS)}}^2}.$$
 (20)

The final input RMS current is calculated in the background loop.

Test results

This method of measuring input power and RMS current was tested on a 360-W PFC evaluation module. The results, shown in Table 1, demonstrate that this method provides excellent measurement accuracy.

Conclusion

A low-cost but accurate method of measuring input power and RMS current for off-line power supplies has been presented. This method uses the existing PFC controller chip and hardware, eliminating the traditional dedicated power-metering chip

and extra sensing circuit, with no impact on normal PFC control. In addition, it provides the following features:

- Extremely low cost
- Simple two-point calibration
- \bullet Simultaneous sampling of V_{IN} and I_{IN} with dual sample- and-hold
- Firmware EMI-current compensation
- Firmware current-sense, phase-shift compensation
- Optimized mathematical calculations with little overhead in CPU usage

Reference

 "Highly integrated digital controller for isolated power," UCD3138 Data Manual. Available: www.ti.com/slusap2-aaj

Related Web sites

Power Management:

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Table 1. Test results of measuring input power and RMS current

OUTPUT	P _{IN} (W)			I _{IN(RMS)} (mA)		
LOAD (%)	WITH METER	WITH DIGITAL CONTROLLER	DIFFERENCE	WITH METER	WITH DIGITAL CONTROLLER	DIFFERENCE
V _{IN(RMS)} = 110 V						
2.50	11.5	10.3	1.2	112	101	11.0
5	18.8	17.9	0.9	180	170	10.0
10	35.4	34.3	1.1	328	317	11.0
20	72.7	71.7	1.0	665	659	6.0
30	107.7	107.2	0.5	989	985	4.0
40	143.5	143.1	0.4	1314	1315	-1.0
50	181.0	180.4	0.6	1656	1661	-5.0
60	216.3	215.4	0.9	1980	1987	-7.0
70	251.6	250.4	1.2	2305	2315	-10.0
80	287.0	285.3	1.7	2631	2643	-12.0
90	324.9	322.8	2.1	2981	2994	-13.0
100	360.6	357.9	2.7	3313	3325	-12.0
V _{IN(RMS)} = 230 V						
2.50	11.0	9.1	1.9	88	87	1.0
5	19.0	16.8	2.2	111	105	6.0
10	36.5	34.5	2.0	177	168	9.0
20	71.1	69.1	2.0	320	311	9.0
30	107.7	106.0	1.7	477	469	8.0
40	144.9	143.1	1.8	637	631	6.0
50	179.4	177.6	1.8	786	782	4.0
60	216.1	214.6	1.5	945	942	3.0
70	253.1	251.6	1.5	1105	1106	-1.0
80	287.7	286.4	1.3	1256	1258	-2.0
90	324.5	322.9	1.6	1416	1419	-3.0
100	361.2	359.9	1.3	1576	1580	-4.0

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