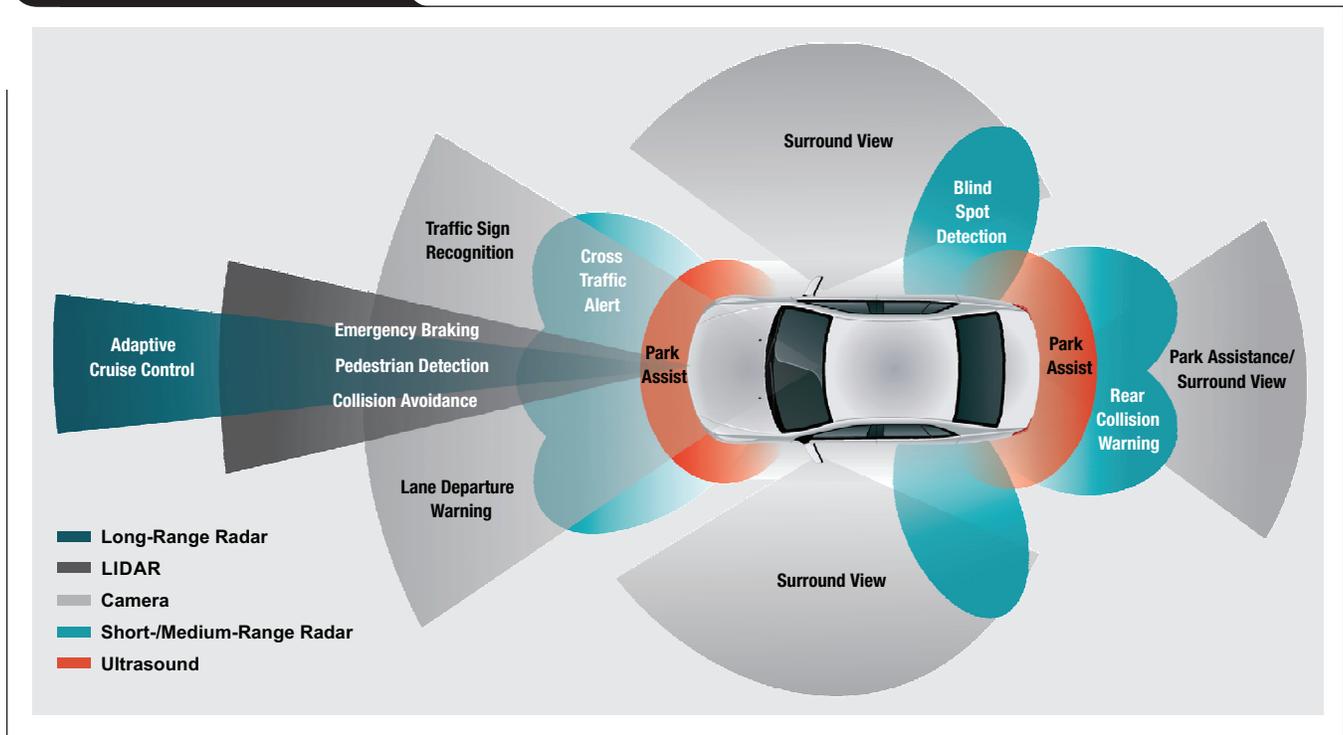


Managing pixel-clock input jitter for more robust serial-link communications

By Jason Syu
Validation Engineer

Figure 1. ADAS Applications



Introduction

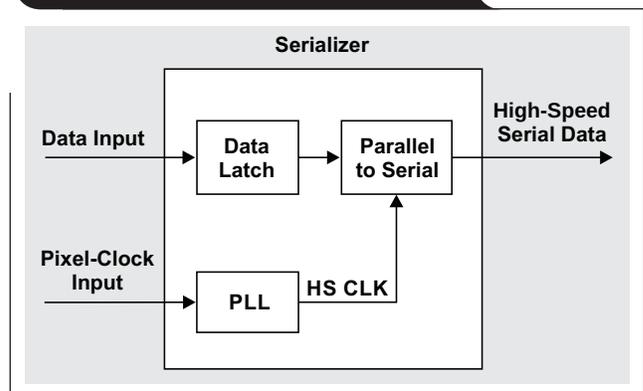
Modern-day automotive systems are packed with image sensors and displays for better driver safety and for enhanced infotainment. In many of these applications, large amounts of video data are transferred from the peripheral of the car to the central electrical control unit (ECU) for further processing. Examples of advance driver assistant systems (ADAS) are shown in Figure 1.^[1] A FPD-Link III SerDes chipset from Texas Instruments, such as the DS90UB933 and DS90UB964, utilizes a serializer to transport the video data from an image sensor at the vehicle’s periphery and sends the image data through a coaxial cable to the deserializer near the ECU for image processing and decision making. To design a robust communication link between a serializer, cable and deserializer, it is important to understand the effect of different jitter components in the system.

Serializer

Figure 2 illustrates a block diagram of a typical serializer. A serializer utilizes a PLL to phase lock to the reference pixel-clock input to derive the high-speed clock for

clocking out the high-speed serial data. Depending on the source of the clock input, whether it comes from an image sensor or a graphics processor, there is going to be some jitter modulated onto the pixel-clock input to the serializer. That jitter will go through the PLL’s jitter-transfer function, and a portion of that jitter will show up on the high-speed serial data.

Figure 2. Serializer block diagram



A typical serializer PLL has a low-passing jitter transfer function. The low-passing characteristic indicates that low-frequency jitter components pass through with minimal attenuation while high-frequency jitter components are attenuated from the input reference clock source. Figure 3 illustrates the magnitude response of a second-order jitter-transfer function. The passband of the PLL starts from low frequency all the way to the -3-dB bandwidth. The stopband refers to frequency range that is -40 dB or more. The transition region is the frequency range between the passband and the stopband.^[2]

In the case where both the channel mismatch and inter-symbol interference (ISI) are minimized, the transmitter output jitter consists of the jitter transferred from the pixel-clock input, and the serializer's intrinsic jitter. The transferred jitter can be approximated as the input clock jitter attenuated by the low-pass transfer function of the serializer PLL. From Figure 3, the transferred output jitter is predominantly lower frequency within the passband. In the transition region (jitter frequency between ω_0 and $10 \omega_0$), less jitter is transferred to the output. In the stopband, the higher-frequency jitter components are totally suppressed by the low-pass response of the PLL. In addition to the transferred jitter, there are some intrinsic jitters from the serializer itself. The intrinsic jitter consists of random jitter, a small amount of periodic jitter or data-dependent jitter due to the finite bandwidth of the output driver.

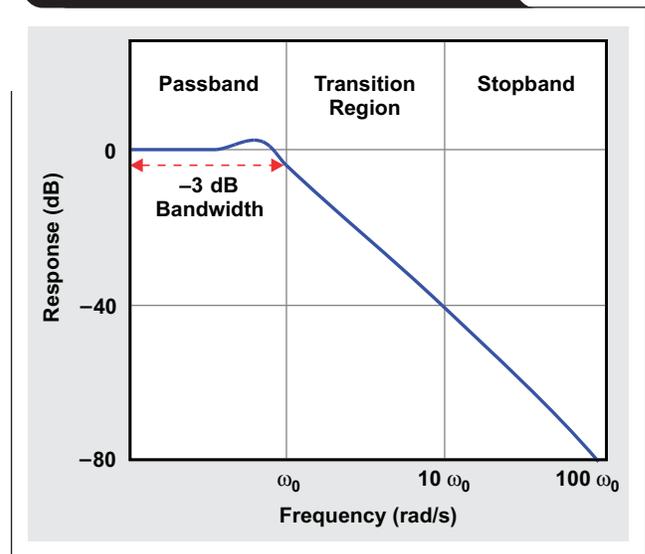
Hardware engineers can manage the jitter amplitude and jitter frequency of the pixel clock to ensure the downstream deserializer is able to lock and sample onto the serializer output.

Serial link

Figure 4 shows the signal path of a serial link consisting of a serializer, cable and deserializer. The serializer's output data propagates through a transmission channel comprised of a printed-circuit-board (PCB) trace, connector, cable, connector, and another PCB trace to the deserializer's input.

The transmission channel behaves as a bandwidth-limited lossy transmission line, so it will introduce

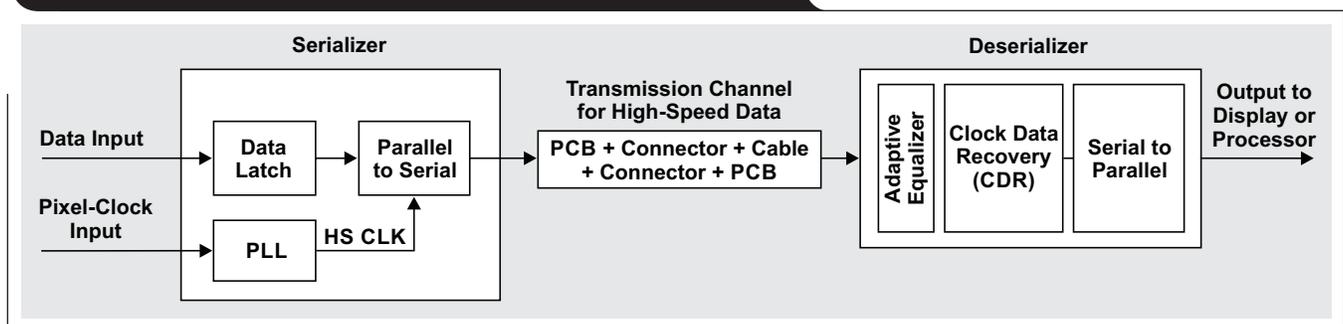
Figure 3. Second-order jitter-transfer function with corner frequency at ω_0



inter-symbol interference jitter (ISI). The signal appears at the end of the transmission channel and is made up of the serializer's intrinsic jitter, the transferred jitter from the pixel clock, and the ISI jitter from bandwidth limitation of the driver and transmission channel.

As the signal goes into the deserializer, an adaptive equalizer in the front end equalizes the transmission-channel distortion and reduces ISI. In the real world, due to imperfections, equalization is never perfect and a small amount of residual ISI still remains. For a bidirectional link used in the FPD-Link III SerDes, a small amount of residual jitter from the deserializer's echo canceller also exists. Therefore, the signal appears at the input of the deserializer's internal circuit for clock-data recovery (CDR) and is an aggregation of the serializer's intrinsic jitter, the transferred jitter from the pixel clock, and the residual jitter from the equalizer and the echo canceller. Hardware engineers must manage these jitter components to ensure the CDR circuit can handle the residual jitter.

Figure 4. Serializer-to-deserializer signal-path block diagram



Deserializer

Input Jitter tolerance (IJT) is a key parameter of a deserializer's clock-data-recovery (CDR) circuit. Figure 5a shows a typical IJT plot. It depicts the CDR circuit's ability to phase lock to the incoming data transitions, to reproduce the embedded high-speed clock, to re-sample and recover data correctly. Within the CDR circuit's loop bandwidth, the circuit is able to track large jitter amplitude. The CDR-circuit's jitter tolerance rolls off until it reaches minimum jitter amplitude at a very-high jitter frequency.

In Figure 5a, a normalized jitter amplitude of 1 unit interval (UI) is the maximum closed-eye phase deviation of the high-speed serial-link signal. For example, in an ADAS application of DS90UB933/DS90UB964 in RAW10 mode running at 100-MHz PCLK,

$$1 \text{ UI} = 1 / (100 \text{ MHz PCLK} \times \frac{1}{2} \times 28 \text{ bits}) = 714.28 \text{ ps.}$$

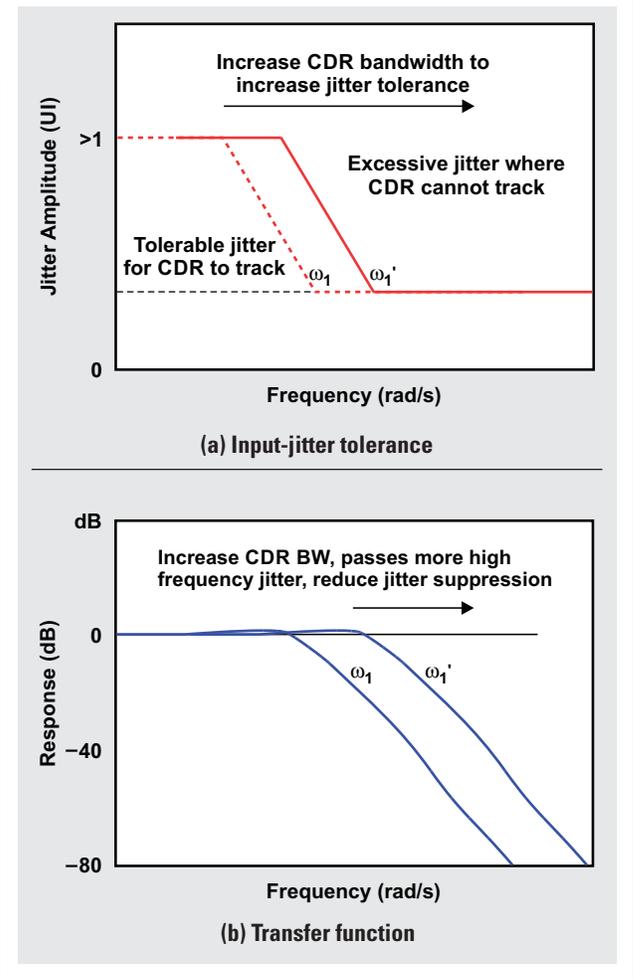
Or, in a IVI application of DS90UH925/DS90UH926 running at 75-MHz PCLK,

$$1 \text{ UI} = 1 / (75 \text{ MHz} \times 35 \text{ bits}) = 380.95 \text{ ps.}$$

As depicted in Figure 5b, increasing the deserializer CDR-circuit's loop bandwidth increases the receiver's jitter tolerance for high-frequency jitter. However, it also allows more high-frequency jitter at the deserializer's output. If too much jitter is at the deserializer's output, this could be an issue for the downstream device. Choosing a CDR circuit bandwidth is thus a trade-off between high IJT and low output jitter.

The implication from the serializer's jitter-transfer function and the deserializer's input-jitter tolerance is that there exists a system-level input-jitter tolerance for the pixel-clock input. This could be done by looking at both the serializer's jitter-transfer function and the deserializer's jitter-tolerance profile at the same time.

Figure 5. CDR circuit input-jitter tolerance and transfer function



Total-system input-jitter tolerance

Figure 6 shows the combined effect of the serializer's jitter transfer and the deserializer's IJT. In the passband of the serializer's jitter transfer function, low-frequency jitter components are passed to the deserializer, and the CDR circuit is able to track with its high IJT.

In the case where the serializer's PLL bandwidth and the deserializer's CDR bandwidth are within a decade, the transition regions of both the serializer's jitter-transfer function and deserializer's jitter tolerance will overlap. This results in a pixel-clock jitter-tolerance reduction in the overlapped region. A way to visualize this is to align the frequency axes of the serializer's jitter-transfer function with that of the deserializer's jitter-tolerance profile as depicted in Figure 6. The U-shape profile of the pixel-clock system-level input-jitter-tolerance (SIJT) profile is because the jitter components within the transition region are not fully suppressed.

For the very-high-frequency jitter (beyond $10 \omega_0$), the serializer's PLL effectively suppresses them, and the SIJT increases again. As long as the pixel-clock jitter is below the SIJT profile, the serializer's output jitter will be below the deserializer's input-jitter tolerance, and a robust link can be established.

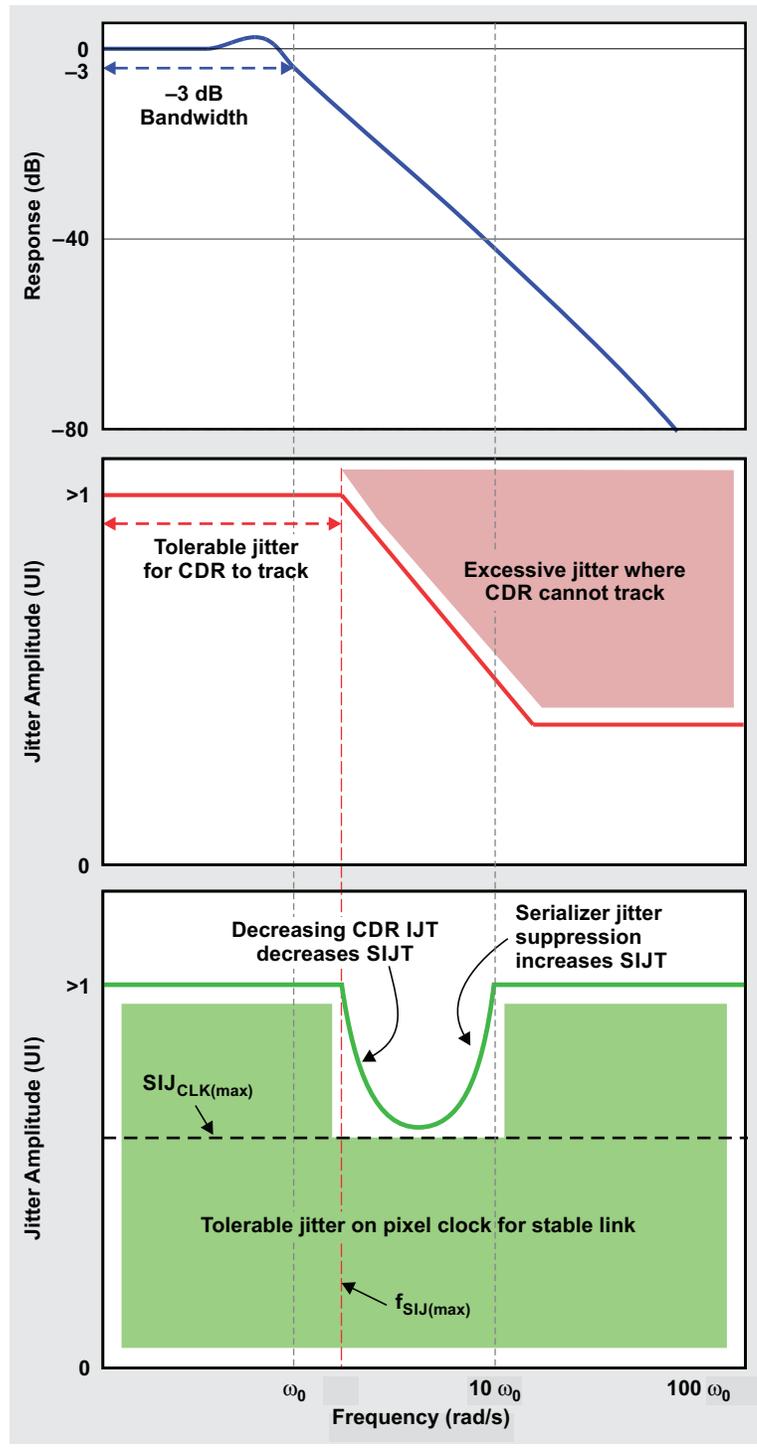
Managing pixel-clock input jitter

Two approaches should be considered for managing the pixel-clock input jitter into the SerDes system. The first approach is to obtain a low-jitter clock source, where its wideband jitter amplitude does not exceed $SIJ_{CLK(max)}$ as shown in Figure 6 (bottom). In this case, the input jitter is below the SIJT profile across all jitter frequencies. However, when a low-jitter clock source is hard to obtain, the second approach is to limit the jitter frequency below $f_{SIJ(max)}$.

When the jitter amplitude or jitter frequency on the pixel clock could not be limited effectively, a jitter cleaner such as TI's automotive-grade CDCE813 could be used to reduce the pixel-clock jitter. As a result, the SerDes system will not experience excessive jitter and a robust link can be established.

To balance the trade-off between jitter tolerance and jitter suppression, the FPD-Link III serializer has a typical -3-dB jitter-transfer bandwidth of around $f/40$, and the FPD-Link III deserializer has a typical CDR-loop bandwidth of around $f/15$, where f is the operating frame-rate frequency. Utilizing the serializer's jitter-transfer function and the receiver's jitter-tolerance curve, a hardware engineer can

Figure 6. Serializer PLL transfer function (top); deserializer jitter-tolerance profile (middle); the combined system-level input-jitter tolerance (SIJT) (bottom)*



*All unit intervals (UI) are based on the bit-width of the FPD-Link III forward channel high-speed signal.

identify the transition regions and properly manage either the pixel-clock jitter amplitude and/or attenuate its high jitter frequency to achieve a stable and robust link.

Conclusion

In order to achieve the desired bit error rate in a high-speed serial communication system, the hardware engineer needs to be mindful of the pixel-clock input jitter. The pixel-clock jitter must be managed properly, so that in conjunction with the serializer's jitter-transfer function and deserializer's IJT, a robust high-speed serial link can be established.

References

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2. E. W. Kamen and B. S. Heck, "Chapter 8 - Analysis of Continuous-Time Systems by Use of the Transfer Function Representation," in *Fundamentals of Signals and Systems Using the Web and MATLAB*, Upper Saddle River, New Jersey, Prentice Hall, 2007, ISBN 0131687379, 9780131687370
3. Mike Peng Li, "Jitter, Noise, and Signal Integrity at High-Speed," Prentice Hall., 2008, ISBN 0132429616, 9780132429610

Related Web sites

Product information:

TI's portfolio of FPD-Link III Serializers/Deserializers

DS90UB949-Q1

DS90UB940-Q1

DS90UB933-Q1

DS90UB934-Q1

DS90UB964-Q1

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