Analyzing the impact of clock noise on an RF-sampling DAC system

By Fanlong Li
China FAE (MGTS), China ZHA, Shanghai China

Introduction

The digital-to-analog converter (DAC) is a key component in a wireless communication system. With the development of modern complementary metal-oxide semiconductor (CMOS) technology, TI's latest DAC is a radio-frequency (RF) sampling DAC with gigahertz sampling.

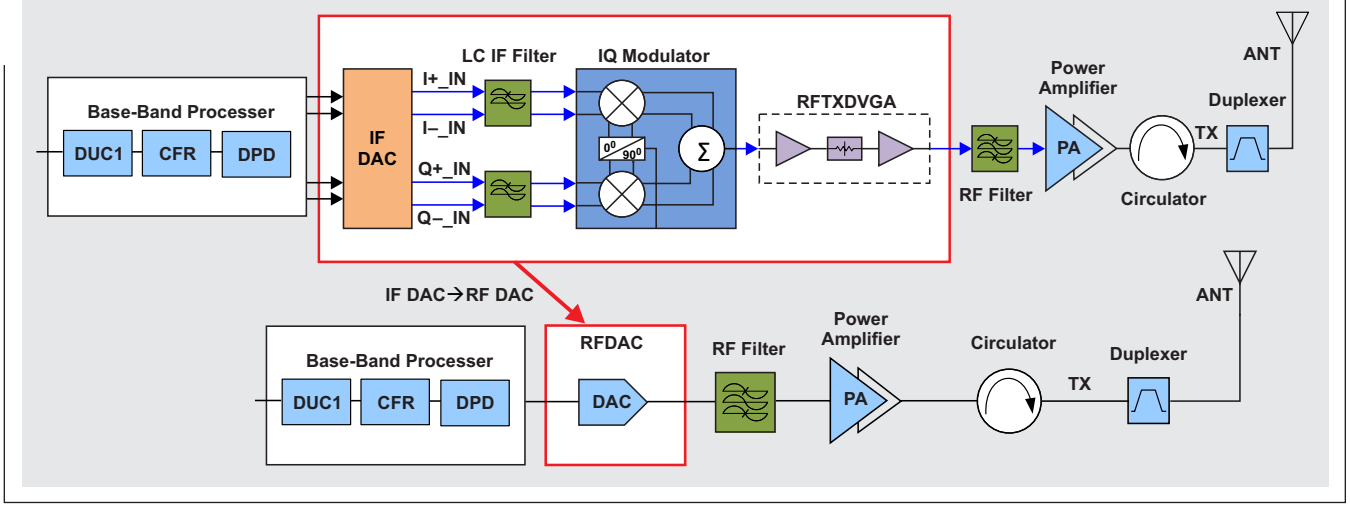
Compared to intermediate-frequency sampling DACs, RF-sampling DACs offer higher integration (Figure 1). Such DACs are popular in fourth-generation (4G) wireless systems such as macro frequency-division duplex (FDD) and time-division duplex (TDD) systems.

Because RF-sampling DACs sample at the RF frequency and are located close to the antenna port, their performance directly impacts the entire base-station transmission system. The high-speed sampling clock plays a very important role in RF-sampling DAC performance because noise on the sampling clock directly translates to the output of the DAC.

This article describes how to evaluate the impact of clock noise on high-speed DAC performance.

Two different kinds of clock noise, random noise and clock spurs, are the primary types of noise under consideration.

Figure 1. An RF-sampling DAC helps achieve highly-integrated solutions



Random noise

Random noise obeys Gaussian distribution and can be described or quantized by clock jitter in the time domain or by phase noise in the frequency domain.

Using a unipolar 3-bit DAC as an example and assuming there isn't jitter on the sampling clock, two equally spaced inputs will produce to two equally spaced outputs (See Figure 2a). As shown in the left graph in Figure 2b, if there is jitter on the sampling clock, then the sampling time of the DAC for a certain digital input code is not strictly defined, which is shown in the right graph in Figure 2b. Due to the random clock jitter, DAC sampling time will drift.

The quantized output of the DAC passes through a shaping filter to produce the analog output signal. If the sampling clock has no jitter, every sampling time is exactly correct, which results in the analog output signal shown in the left graph in Figure 2a. For a clock with jitter, however, the sampling time of the DAC will be unpredictable.

Assuming a sampling time shift is Δt, the sampling instance the analog output signal will show a corresponding amplitude shift, Δy, as shown in the right graph in Figure 2b. Δy is the amplitude error and considered noise caused by unpredictability.

Theoretical analysis of random clock noise on DAC performance

Now consider how clock noise impacts DAC output noise mathematically.

Again, the DAC output will generate current or voltage noise (Δy) caused by sampled clock jitter. Assuming that the clock jitter is random, the DAC output noise will also be random. The generated output noise will degrade the DAC output's signal-to-noise ratio (SNR).

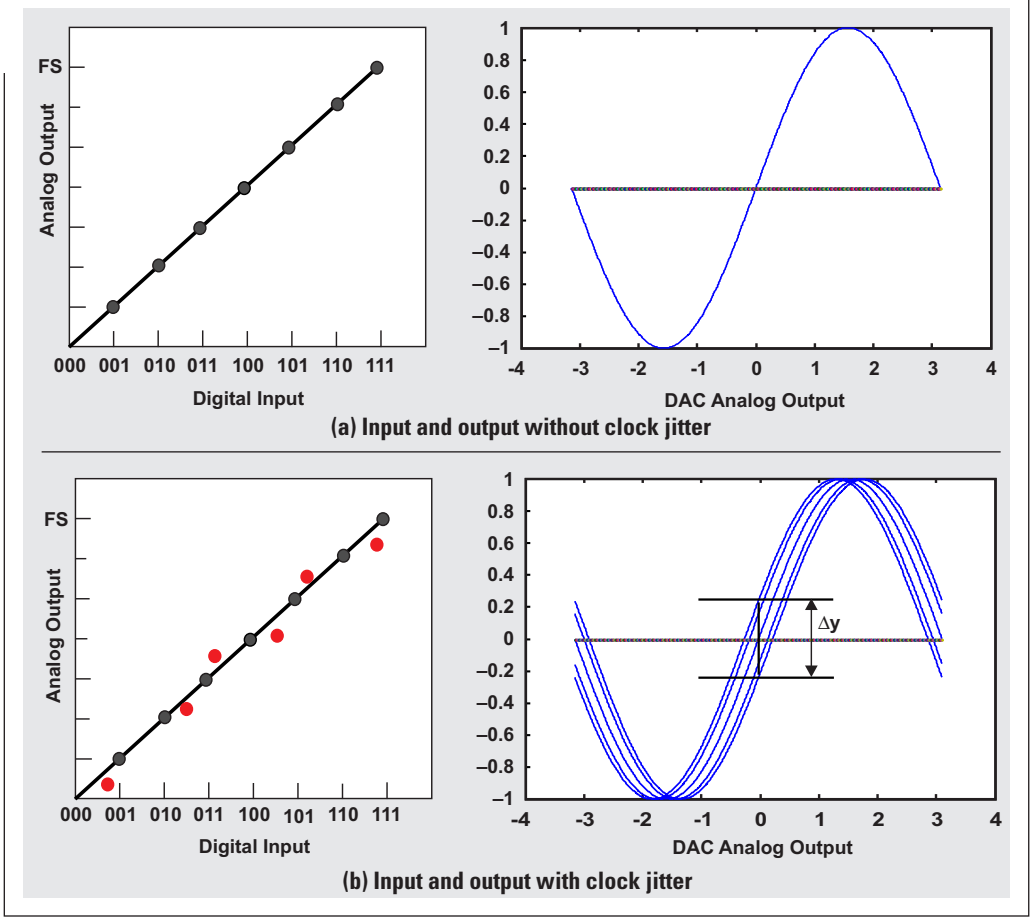
Reference 1 gives a theoretical analysis of random clock noise on analog-to-digital converter (ADC) performance in the frequency domain. But for a DAC, only the sinc function for the signal is required.

Equation 1 calculates the impact of clock noise on DAC performance:

$$SNR_{SIG}\ (dB) = SNR_{CLK}\ (dB) + 20\log\left(\frac{\pi}{\sin\left(\frac{\pi f_{SIG}}{f_{CLK}}\right)}\right)(dB) \quad (1)$$

where f_{SIG} is the signal frequency and f_{CLK} is the frequency of the DAC sampling clock.

Figure 2. DAC sampling with and without clock jitter



Theoretical analysis of clock spurs on DAC performance

Unlike the random properties of clock noise, a clock spur is a deterministic time error in the sampling clock. An interesting question to ponder is if there is a spur at a certain frequency offset from the center frequency of the DAC sampling clock, what kind of behavior will show at the output of the DAC, such as what is the spur's location and spur's amplitude?

First consider the clock-spur location at the DAC output. For any time-continuous signal $x_a(t)$, Equation 2 calculates the discrete sampled signal as:

$$x(nT_S) = x_a(t)\Big|_{t=nT_S} = x_a(t) \times p(t)$$
$$\text{and} \quad p(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_S) \ , \tag{2}$$

where $x(nT_S)$ is a discrete sampled signal and $p(t)$ is the impulse function, which also represents the ideal sampling function.

Equation 2 indicates that the sampling process will multiply the signal to be sampled with the period of impulse function, which is $T_S = 1/f_S$ in the time domain. In the frequency domain, because the sampling process is equivalently a convolution operation, the two signals will convolute together. If the sampling frequency, f_S, is known, then Equation 3 calculates the Fourier transformation of the impulse series as:

$$P(j\omega) = \frac{2\pi}{T_S} \times \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_S) \tag{3}$$

where $\omega_s = \frac{2\pi}{T_S} = 2\pi f_S$,

and $P(j\omega)$ is the discrete Fourier transformation of $p(t)$.

For a sampling clock with a fixed spur, Equation 4 gives the spectrum expression as:

$$P(j\omega) = \frac{2\pi}{T_{S1}} \times \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_{S1}) + \frac{2\pi}{T_{S2}} \times \alpha \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_{S1} - k2\pi\Delta f) \tag{4}$$

where $\omega_{S1} = \frac{2\pi}{T_{S1}} = 2\pi f_{S1}$, $\omega_{S2} = \frac{2\pi}{T_{S2}} = 2\pi(f_{S1} + \Delta f)$,

ω_{S2} stands for the spur frquency on DAC sample clock, and α is a constant.

Assuming that the spectrum expression of a time-continuous signal is $X_S(j\omega)$, Equation 5 provides the output signal spectrum when sampled by a clock signal with a fixed spur:

$$X_S(j\omega) = X_a(j\omega) * \left[\frac{2\pi}{T_{S1}} \times \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_{S1}) + \frac{2\pi}{T_{S2}} \times \alpha \sum_{k=-\infty}^{\infty} \delta(\omega - k\omega_{S1} - k2\pi\Delta f) \right] \tag{5a}$$

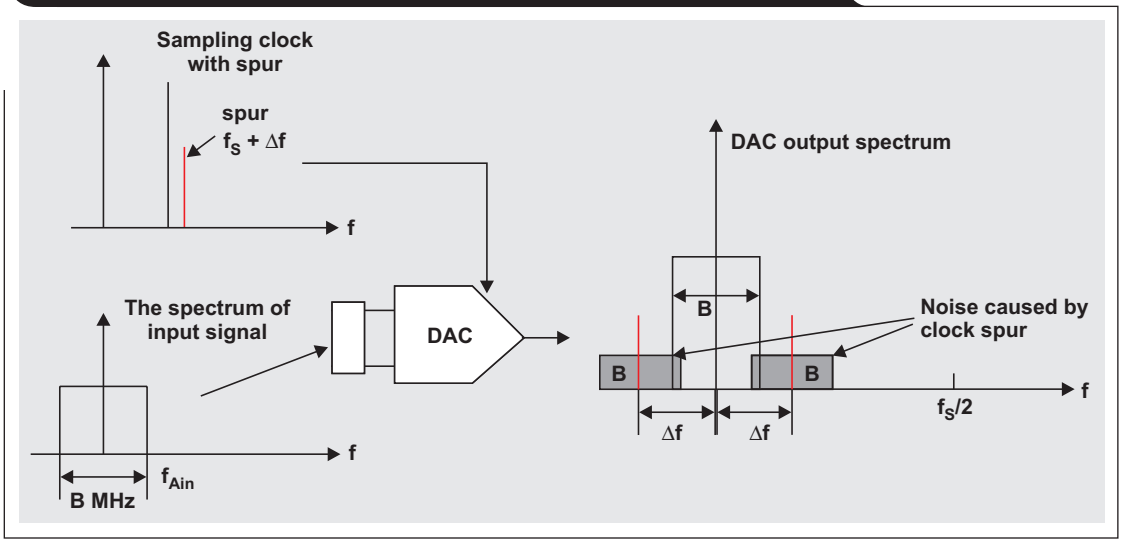
Therefore,

$$X_S(j\omega) = \frac{1}{T_S} \times \sum_{k=-\infty}^{\infty} X_a(j2\pi f - j2\pi k f_S) + \frac{\alpha}{T_S} \times \sum_{k=-\infty}^{\infty} X_a\left[j2\pi f - j2\pi k(f_S + \Delta f)\right] \tag{5b}$$

From Equation 5, note that the spur at the DAC output has the same frequency offset as in the sampling clock.

Figure 3 shows an example of a DAC clock with a spur to sample the bandwidth signal. For the spur amplitude changing at the DAC output, the signal noise ratio (SNR) of the DAC can be used to replace and thus follow Equation 1.

Figure 3. The clock spur's location transferred to the DAC output



In Figure 3, if the spur falls within the signal bandwidth shown as B, then the spur of the sampling clock will hit the signal and impact the band performance. On the other hand, the clock phase noise can be taken as an infinite number of spurs with infinitely-small frequency spacing.

In general, to get the double-band phase noise, integrate the single sideband phase noise and double it. For single sideband phase-noise integration, use these rules to determine the integration limits:

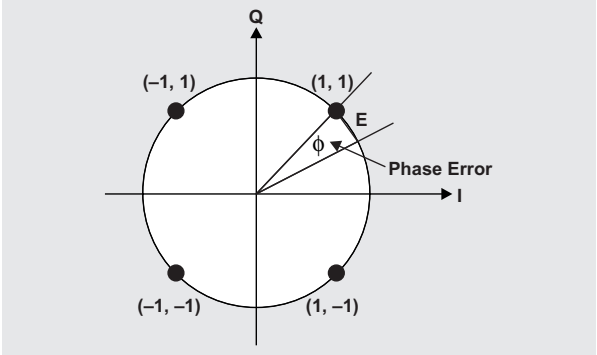
- A low limit of integration: In the time domain, the signal is frame-based. If the clock jitter frequency is less than the frame period, the slowly changing jitter can be taken as a constant for a certain frame. Within the frame, the phase changing of the carrier is almost zero and it will not do harm to demodulate. For a 20-MHz long-term evolution (LTE) signal, the frame period is 10 ms, which means 100 Hz, so the phase noise can be integrated from 100 Hz.
- A high limit of integration: Use half of the signal bandwidth. For a 20-MHz LTE signal, the upper limit is 10 MHz. Therefore, for a single sideband, the integral bandwidth is from 100 Hz to 10 MHz for a 20-MHz LTE signal.

Analyzing clock noise for DAC system specifications

After analyzing the location and magnitude of the clock noise transfer to the DAC output, use the noise level and noise-integration bandwidth to calculate the performance impairments. At a system level, the clock phase noise will affect the error vector magnitude (EVM) and spurious-free dynamic range (SFDR) of DAC output signals, especially when digitally modulating the output waveform.

The constellation plot in Figure 4 defines EVM. Starting from the definition, the relationship between EVM and clock phase noise can be determined in a DAC sampling system. Here, quadrature phase-shift keying (QPSK) modulation is the example, although the derivation still holds for other modulations.

Figure 4. QPSK-signal constellation plot with phase error



Equation 6 defines error vector magnitude (EVM) as the ratio between error vector and reference vector:

$$EVM = \sqrt{\frac{\int\left[x(t)-s(t)\right]^2 dt}{\int x(t)^2 dt}} \quad (6)$$

where x(t) is the vector of the reference signal and s(t) is the vector of the input signal.

Taking the QPSK constellation plot into consideration, the EVM can now be determined. Assuming that the radius in Figure 4 is R, according to the definition for error vector magnitude and trigonometric formula, the error vector (E) can be determined with Equation 7.

$$E^2 = 2R^2 - 2R^2 \times \cos(\phi) \quad (7)$$

When ϕ is small, according to the Taylor series, substitute $\cos(\phi) = 1 - (\phi^2/2)$ to get Equation 8, which shows the relationship between phase noise in radian and EVM.

$$EVM = \phi = 100\% \times \left(\frac{\pi}{180}\right) \times Phase\_Noise_{RMS} \quad (8)$$

where $Phase\_Noise_{RMS}$ is the root-mean-square (RMS) clock phase noise in degrees.

Equation 9 calculates the phase noise from the measured phase-noise plot:

$$Phase\_Noise_{RMS} = \frac{180}{\pi} \times \sqrt{2 \times \int_0^\infty L(f)df} \quad \text{(in degrees)} \quad (9)$$

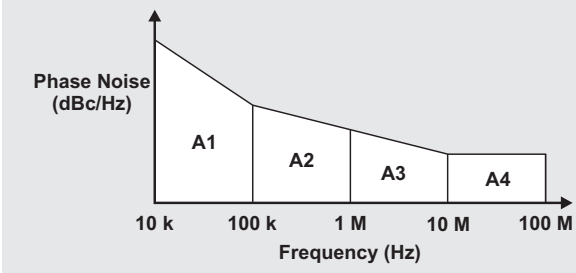
where L(f) is the power spectral density for the clock phase noise.

$$\text{Therefore, } EVM = 100\% \times \sqrt{2 \times \int_0^\infty L(f)df} \quad (10)$$

Equation 9 can be used to obtain the phase noise in radians by integrating the phase-noise power density over a certain bandwidth.

A simple way to get an approximate result of phase noise is to use the trapezium method (Figure 5). First, convert the decibels of phase noise into a linear value, and then calculate the area for A1, A2, A3, A4, etc. Get the total area and double it for double-side phase noise for the total phase noise in radians.

Figure 5. Phase-noise calculation using the trapezium method



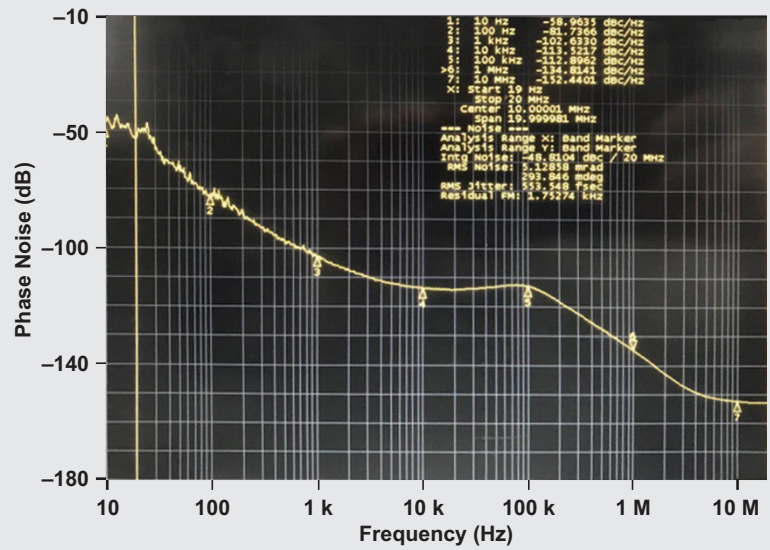
Here is a summary of the process for obtaining the impact of clock phase noise on a DAC:

- Measure the phase noise of the sampling clock and get the phase-noise plot.
- Calculate the DAC output noise according to Equation 1.
- Obtain the integration bandwidth for noise.
- Obtain the clock jitter in radians across a specific bandwidth according to the trapezium method.
- Calculate the error vector magnitude (EVM) according to Equation 9.

To obtain the impact of a clock spur on DAC SFDR, consider the impact of the sampling clock spur on DAC output with two pieces of information:

- Offset information: The frequency offset from the main output signal is the same as the spur offset frequency from the sampling clock.
- Amplitude information: The amplitude of a spur at the output can be replaced by SNR from Equation 1, which is similar to random noise.

Figure 6. A practical measurement of clock phase noise on EVM

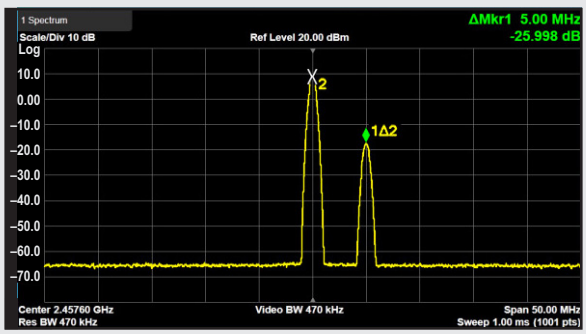


Calculations versus measurements

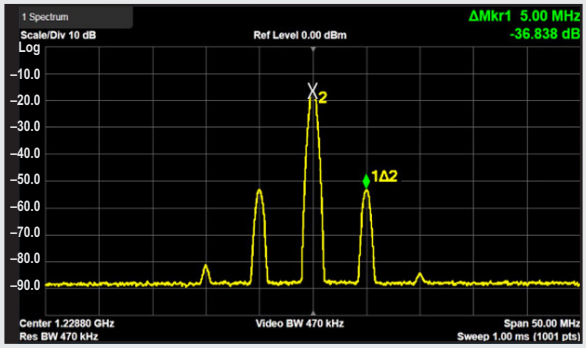
According to the trapezium method, the calculated EVM is 1.14%. The practical measurement is 0.512 × 2 = 1.02%, which matches the theoretical calculations very well. The measured EVM in the phase-noise plot is the single sideband result, which needs to be doubled when considering the double-sideband EVM shown in Figure 6.

Figure 7 shows the clock spur tested with the DAC38RF83 evaluation-module board using the external clock mode. Figure 7a is the clock spur input and Figure 7b is the clock spur output after the RF DAC with a 1.2288-GSPS signal. According to Equation 1, the clock spur at the DAC output is 36 dBc in theory, which matches the testing results well.

Figure 7. A practical measurement of spurs on both the sampling clock and DAC output



(a) Clock spur input



(b) Clock spur output

Conclusion

Clock noise from a RF-sampling DAC will impact its error vector magnitude (EVM) and SFDR. This was shown in this article through practical measurements and theoretical analysis of these phenomena. Application engineers and system designers can use the equations presented to perform transmit-chain budget analysis of the DAC output to determine if noise may be a problem in a clock design.

Reference

1. Thomas Neu, "Clocking the RF ADC: Should you worry about jitter or phase noise?" Analog Applications Journal (SLYT705), 1Q17.

TI Worldwide Technical Support

TI Support

Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

China: http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp

Japan: http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp

Technical support forums

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

e2e.ti.com

China: http://www.deyisupport.com/

Japan: http://e2e.ti.com/group/jp/

TI Training

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

China: http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968

Japan: https://training.ti.com/jp

A011617

SLYT751

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265