

OMAP5910 Decoupling/Filtering Techniques

Thanh Tran, Ph.D.

DSP/EEE Catalog, OMAP Applications

ABSTRACT

OMAP5910 consists many of critical signal and power supply pins that require special decoupling or filtering techniques to prevent excessive voltage ripples and noise/radiation. This application report outlines the important criteria to figure out the minimum number of bypass and bulk capacitors.

Contents

1	Introduction	2
2	Decoupling Techniques	2
	2.1 Capacitor Theory	2
	2.2 OMAP5910 Decoupling Strategy	3
	2.3 Switching Currents Estimation	4
	2.4 Calculating Decoupling Capacitor Value	5
	2.5 Selecting Bulk Capacitors	8
	2.6 Placing Decoupling Capacitors	9
3	Conclusion	10
4	References	10

List of Figures

Figure 1. Capacitor Equivalent Circuit	2
Figure 2. OMAP5910 GZG Package	4
Figure 3. Region 1 Decoupling Capacitors	6
Figure 4. Region 2 Decoupling Capacitors	7
Figure 5. Region 3 Decoupling Capacitors	7
Figure 6. Region 4 Decoupling Capacitors	8
Figure 7. Complete Diagram of Decoupling Capacitors	9

List of Tables

Table 1. Switching Current Estimation	4
---	---

Trademarks are the property of their respective owners.

1 Introduction

OMAP5910 is a true system-on-chip device, which has multiple power supply voltages connecting to different sections of the design that require different decoupling capacitors. The two main voltages are the core voltage, 1.6 V typical, and the input/output (I/O) voltage, 3.3 V typical. The core operating frequency is specified up to 150 MHz, while the highest I/O (external memory interface fast or EMIFF) frequency is only 75 MHz. All other ports are running less than 40 MHz. The speed of the ports is an important parameter to determine the type and value of the decoupling capacitor used to bypass that particular port. Another important parameter is the maximum allowable ripple on the power supply pins. In this document, the assumption is 10-mV maximum ripple, which should be acceptable for the high-speed, high-performance system designs.

2 Decoupling Techniques

The following shows the steps of figuring the number and value of capacitors being applied to filter the power supply pins of the OMAP5910.

1. Understand the capacitor theory and the resonant frequency.
2. Divide the device into 4 regions by drawing two symmetry lines across the part.
3. Determine the number of core voltage supply and I/O voltage supply pins.
4. Estimate the switching currents of the supply pins.
5. Calculate the bypass capacitor value.
6. Select the bulk capacitor value.
7. Place the bypass and bulk capacitors.

The above design flow is applicable to other OMAP devices as well.

2.1 Capacitor Theory

The key specification of the capacitor used for decoupling is the self-resonant frequency, where the capacitor remains capacitive up to this frequency and starts to appear as an inductor above this frequency. Figure 1 illustrates a series-equivalent circuit of the capacitor.

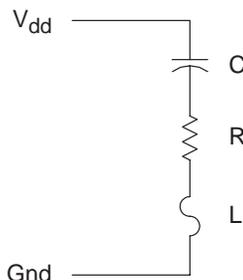


Figure 1. Capacitor Equivalent Circuit

Each capacitor has three different components: equivalent series resistance (ESR), equivalent series inductance (ESL), and the capacitance itself. The self-resonant frequency happens at the point where the impedance of the capacitor, Z_C , is equal to the impedance of the inductor, Z_L .

$$Z_C, \text{ capacitor} = \frac{1}{\omega C}, \text{ where } C \text{ is capacitance, and } \omega \text{ is } 2\pi \text{ times the frequency, } f.$$

$$Z_L, \text{ inductor} = \omega L, \text{ where } L \text{ is inductance.}$$

At resonant, Z_L is equal to Z_C or

$$\frac{1}{\omega C} = \omega L,$$

$$\omega^2 = \frac{1}{LC},$$

$$\omega = \frac{1}{\sqrt{LC}}, \text{ where } \omega = 2\pi f.$$

Therefore, the self-resonant frequency is

$$f = \frac{1}{2\pi\sqrt{LC}}.$$

As shown in the self-resonant equation, lower capacitance and lower inductance yield higher resonant frequency. For a given capacitance value, by choosing smaller surface mount component (for example 0603), higher self-resonant frequency is achieved because typically a smaller component package has lower parasitic and/or lead inductance. The whole decoupling concept is to provide a low-impedance path from the power supply to ground, to shunt the unwanted RF energy. Therefore, choosing a low-inductance but high-value capacitor (low impedance) is very important.

2.2 OMAP5910 Decoupling Strategy

The decoupling strategy proposed here is to first divide the OMAP 289-pin GZG package into four regions by drawing two symmetry lines across the part. After that, do the analysis of each region separately. Part of the analysis requires counting the number of core voltage pins, I/O voltage pins and signals, not including the ground pins. Also, pay special attention to the critical sections such as external memory interface fast (EMIFF), analog phase-locked loop (PLL), and other high-speed serial/parallel ports. See Figure 2.

Bottom View of the OMAP5910 Package

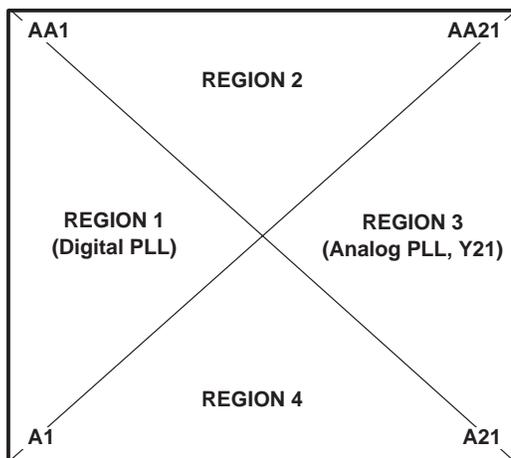


Figure 2. OMAP5910 GZG Package

REGION 1: 3 Core voltage pins, 8 I/O voltage pins, and 54 input/output pins

REGION 2: 3 Core voltage pins, 4 I/O voltage pins, and 59 input/output pins

REGION 3: 3 Core voltage pins, 3 I/O voltage pins, and 59 input/output pins

REGION 4: 4 Core voltage pins, 6 I/O voltage pins, and 55 input/output pins

The next step is to conservatively estimate the switching-current requirements for each region.

2.3 Switching Currents Estimation

Table 1 shows the calculations of switching currents for all four regions.

Table 1. Switching Current Estimation

Region	Estimated Peak Core Current	Estimated Peak I/O Current (all outputs switching at 4 mA)
Region 1	$\frac{170 \text{ mA}}{13} \times 6 = 78 \text{ mA}$	4 mA x 54 = 216 mA
Region 2	Same as 1, 78 mA	4 mA x 59 = 236 mA
Region 3	Same as 1, 78 mA	4 mA x 59 = 236 mA
Region 4	$\frac{170 \text{ mA}}{13} \times 8 = 104 \text{ mA}$	4 mA x 55 = 220 mA

In this table, the peak core current consumption is calculated based on a 170-mA specification in the data manual, plus 100% margin. For example, in region 1, $(170 \text{ mA}/13)(3 \text{ core pins})$ (2 margin) = 78 mA, and 13 is the total number of the core voltage pins. For the I/O, it is estimated by multiplying 4 mA with the total number of the inputs/outputs for each region. This is a very conservative approach, since it is assumed that all outputs and inputs are switching simultaneously.

2.4 Calculating Decoupling Capacitor Value

Since the core voltage and the I/O voltage are operating at different frequencies, it is necessary to decouple these power supplies using the correct capacitors. The following shows the steps to calculate and to select the decoupling capacitors for both the core and I/O supplies.

The capacitor charge current equation is

$$I = C \frac{dV}{dt}, \text{ where } I = \text{peak current, } dV = \text{maximum allowable ripple voltage, and } dt = \text{risetime.}$$

$$I = C \frac{\Delta V}{\Delta t},$$

Therefore,

$$C = I \frac{\Delta t}{\Delta V}.$$

(1)

To find the decoupling capacitance, plug the peak current, the risetime, and the maximum ripple voltage parameters into equation (1), and solve for C. It is safe to assume that the maximum ripple voltage is 10 mV, and the risetime is 1 ns, which is typical for OMAP5910.

Now, calculate the total capacitance required for each region, and then decide what type of capacitors to use.

$$\text{Region 1: Total core capacitance, } C = I \frac{\Delta t}{\Delta V} = 78 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.0078 \mu\text{F}$$

$$\text{Total I/O capacitance, } C = I \frac{\Delta t}{\Delta V} = 216 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.022 \mu\text{F}$$

Since there are 3 core voltage pins with an operating frequency of 150 MHz, and 8 I/O voltage pins with an operating frequency of 75 MHz, it is desired to have multiple capacitors for multiple supply pins, but there is a physical limitation due to PC board space. For the OMAP5910 GZG package, there is enough board space to place about 4 capacitors per region. In this case, select two capacitors with the total capacitance of around 0.0078 μF , and the self-resonant frequency of 150 MHz, to decouple the core voltage pins in region 1. Now, select two capacitors with the total capacitance of around 0.022 μF and the self-resonant frequency of 75 MHz to decouple the I/O voltage pins in region 1. As mentioned in section 1, region 1 consists of an EMIFF port, which operates as high as 75 MHz.

In summary, for core voltage in region 1, use two 0.0047- μF ceramic capacitors and, for the I/O voltage, use two 0.01- μF ceramic capacitors. See Figure 3.

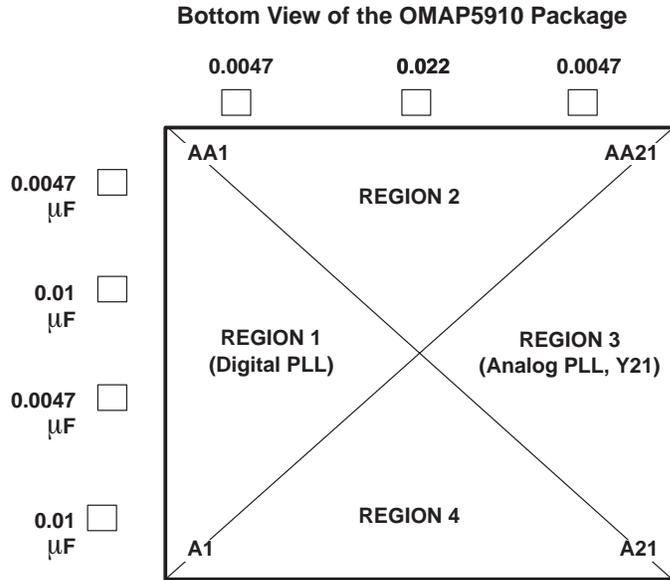


Figure 4. Region 2 Decoupling Capacitors

Region 3: Total core capacitance, $C = I \frac{\Delta t}{\Delta V} = 78 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.0078 \mu\text{F}$

Total I/O capacitance, $C = I \frac{\Delta t}{\Delta V} = 236 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.024 \mu\text{F}$

Region 3 is the same as Region 2. Therefore, for core voltage in Region 3, use two 0.0047- μF ceramic capacitors and, for the I/O voltage, use one 0.022- μF ceramic capacitor. See Figure 5.

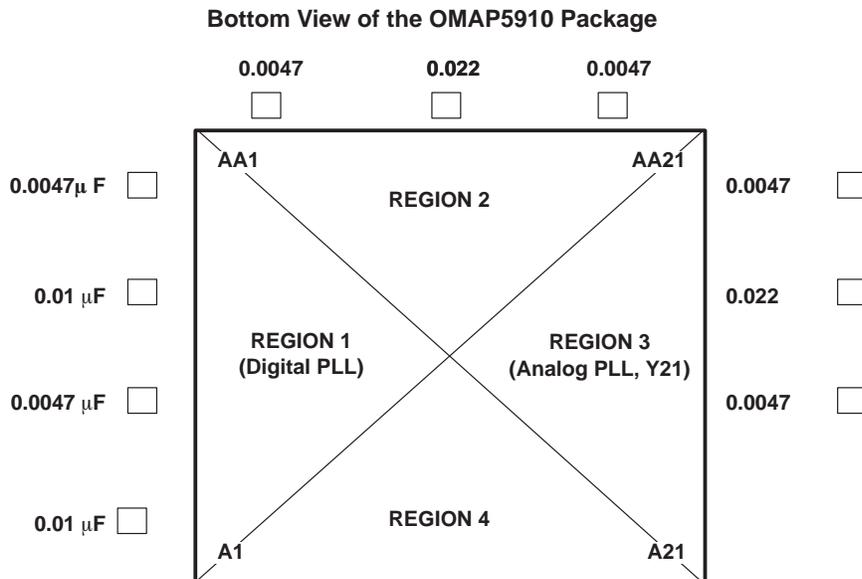


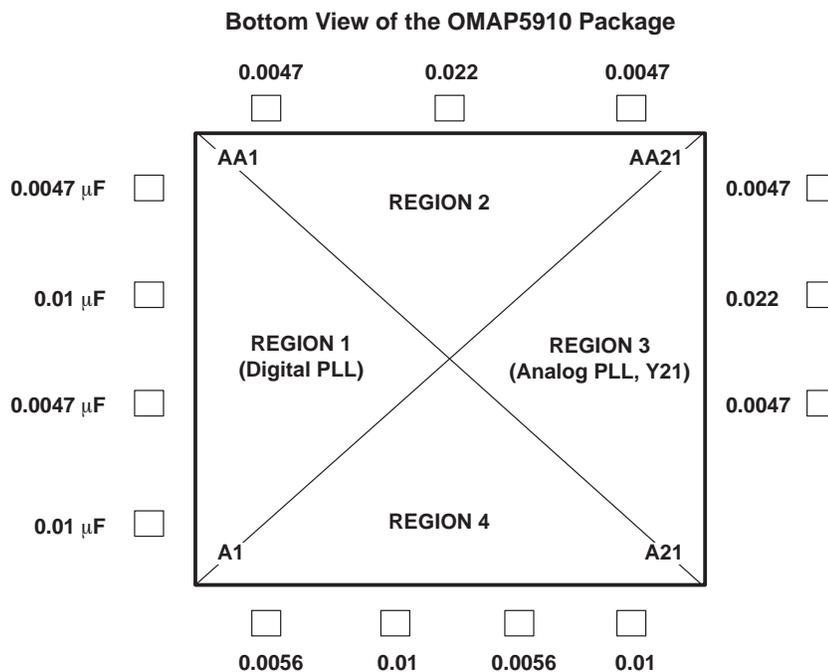
Figure 5. Region 3 Decoupling Capacitors

Region 4: Total core capacitance, $C = I \frac{\Delta t}{\Delta V} = 104 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.01 \mu\text{F}$

Total I/O capacitance, $C = I \frac{\Delta t}{\Delta V} = 220 \text{ mA} \frac{(1 \text{ nS})}{(10 \text{ mV})} = 0.022 \mu\text{F}$

Since there are 4 core voltage pins with operating frequencies of 150 MHz, and 6 I/O voltage pins with operating frequency of 40 MHz, it is desirable to have multiple capacitors for multiple supply pins. For the OMAP5910 GZG package, there is enough board space to place about 4 capacitors per region. In this case, select two capacitors with the total capacitance of around $0.01 \mu\text{F}$, and the self-resonant frequency of 150 MHz to decouple the core voltage pins in Region 4. Now, select two capacitors with the total capacitance of around $0.022 \mu\text{F}$ and the self-resonant frequency of 40 MHz, to decouple the I/O voltage pins of Region 4.

In summary, for core voltage in Region 4, use two $0.0056\text{-}\mu\text{F}$ ceramic capacitors and, for the I/O voltage, use two $0.01\text{-}\mu\text{F}$ ceramic capacitors. See Figure 6.



2.5 Selecting Bulk Capacitors

Bulk capacitors are not critical, but they are important to include in the design to filter the low-frequency ripple typically generated by switching the power supply, and to serve as recharge capacitors for the decoupling capacitors.

The general rule is to select the bulk capacitor value is to select at least ten times the total decoupling capacitance. For the core voltage,

$$10 \times (\text{total capacitance}) = 0.39 \mu\text{F}.$$

For the I/O voltage,

$$10 \times (\text{total capacitance}) = 0.84 \mu\text{F}.$$

The best technique is adding 4 bulk capacitors to 4 regions of the OMAP. The smallest bulk-capacitance value available is 4.7 μF . Select tantalum bulk capacitors, if possible. The other type that can also be used is a surface-mount electrolytic capacitor.

Figure 7 shows the complete diagram, which includes all the decoupling capacitors recommended for the OMAP5910.

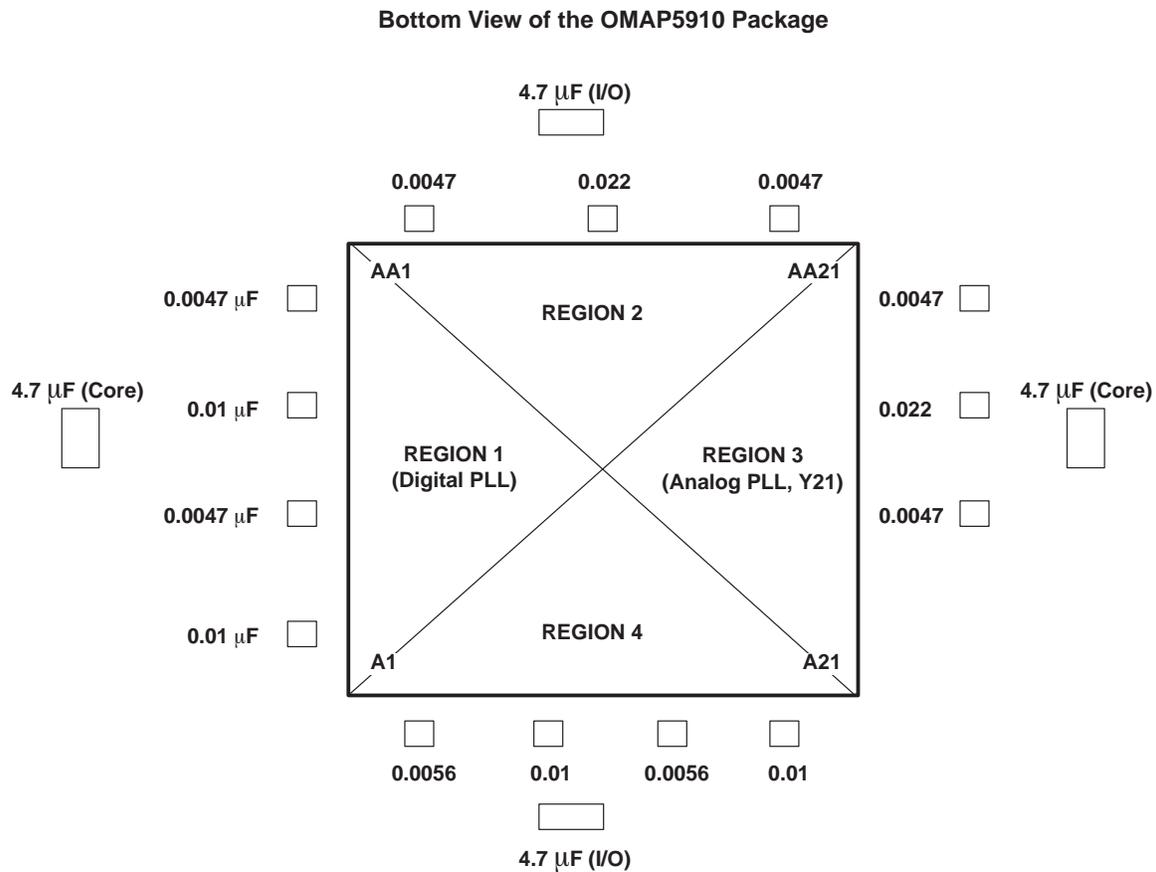


Figure 7. Complete Diagram of Decoupling Capacitors

2.6 Placing Decoupling Capacitors

It is very important to place all the decoupling capacitors as close to the pins as possible, and the bulk capacitors as close to the decoupling capacitors as possible. This minimizes the traces and, therefore, minimizes the current loops that help lower the radiation, while reducing the parasitic inductance. The best strategy is placing the decoupling capacitors on the bottom of the PC board and the bulk capacitors on the top. For the bulk capacitors, make sure to alternate between the core and the I/O, as shown in Figure 7. Placing the capacitors as recommended helps recharge the decoupling capacitors, while maintaining low-inductance paths.

3 Conclusion

This application report demonstrates strategies to calculate and determine the best method for decoupling the power-supply noise for the OMAP5910. In general, decoupling requires much iteration during the design phase, to reduce the electromagnetic interferences and power-supply noise, which are difficult to predict without thoroughly characterizing the system itself. This document is intended only to provide designers the proper starting point. It does not ensure that the recommended decoupling techniques outlined here work in all cases.

4 References

1. *OMAP5910 Dual-Core Processor Data Manual* (SPRS197).
2. *OMAP5910 Dual-Core Processor Technical Reference Manual* (SPRU602).
3. Howard Johnson and Martin Graham. *High-Speed Digital Design*. Prentice-Hall: New Jersey, 1993.
4. Henry Ott. *Noise Reduction Techniques In Electronic Systems*. John Wiley & Sons: 1988.
5. Mark Montrose. *Printed Circuit Board Design Techniques for EMC Compliance*. Wiley-Interscience: New York, 2000.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated