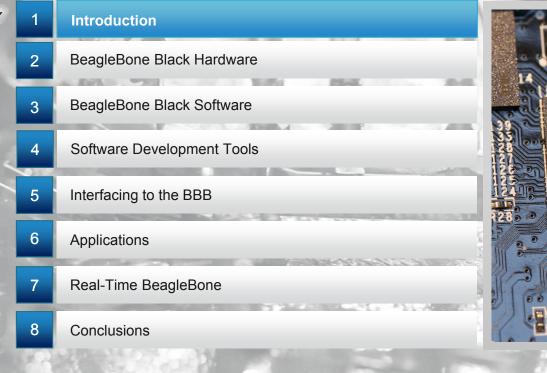
The BeagleBone Application in Engineering Education

Dr Derek Molloy, School of Electronic Engineering, Dublin City University, Ireland



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## **Overview** The BeagleBone: Application in Engineering Education





# Introduction Who am I?

- Dublin City University
  - 12,000 registered students
- Faculty of Engineering & Computing
- Research
  - Computer Vision, 3D Graphics
- Teaching
  - Electronics, 3D Graphics,
  - OOP & Embedded
- User of the Beaglebone!

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Teaching Innovations EE223 – Digital & Analogue Electronics (5 ECTS)

- 140 students p.a.
- Flipped labs
  - Borrow kit of components for a semester
  - Replace components free of charge (assume consumption)
  - Built in to summative assignments
- Encourage learning-by-discovery
- Supported by a YouTube channel
- Also deployed to fully on-line modality (DCU Connected)

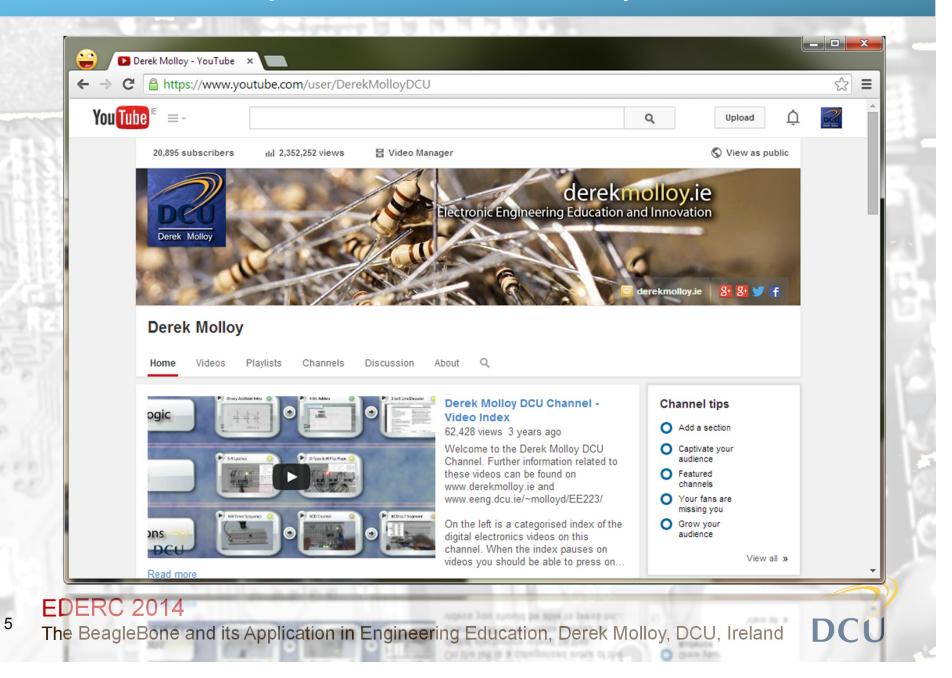
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DCU

## www.youtube.com/DerekMolloyDCU



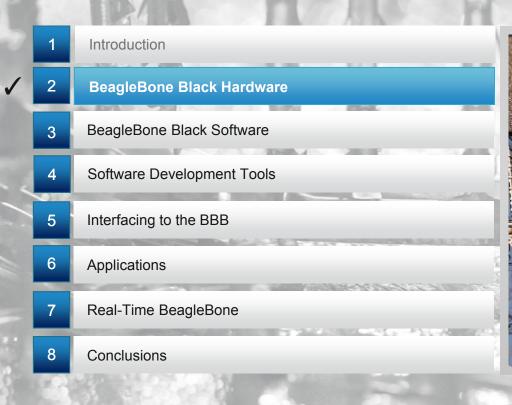
Teaching Innovations EE402 – OOP with Embedded Systems (7.5 ECTS)

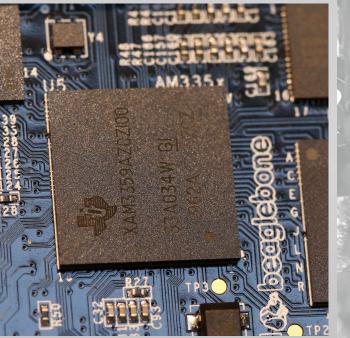
- 90-100 Students p.a.
- Object-oriented Programming
- C++, Qt, Java, embedded Linux
- Assignments, computer-based exam
  - Beaglebone-based wrap low-level hardware
  - TCP Client/Server assignment (IoT-like)
  - Supported by videos (screencast & YouTube)

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## **Overview** The BeagleBone: Application in Engineering Education





# BeagleBone Black Hardware Summary specification

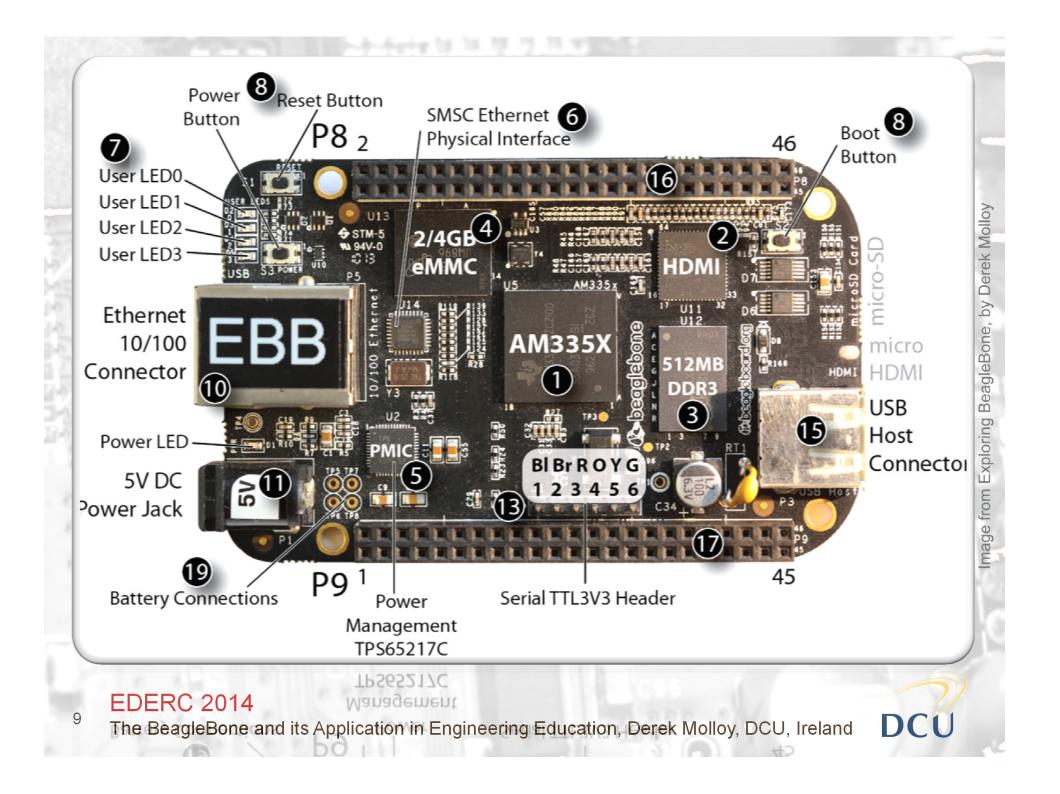
- AM335x 1GHz ARM A8 (2,000 MIPS)
- 512 MB DDR3 RAM
- 4 GB eMMC (rev.C) (plus SD card)
- HDMI Video output (3D graphics engine)
- 10/100 Ethernet (Wi-Fi, Bluetooth via USB)
- Huge range of interfaces (GPIOs, buses, USB)
- Low power (1W to 2.3W)

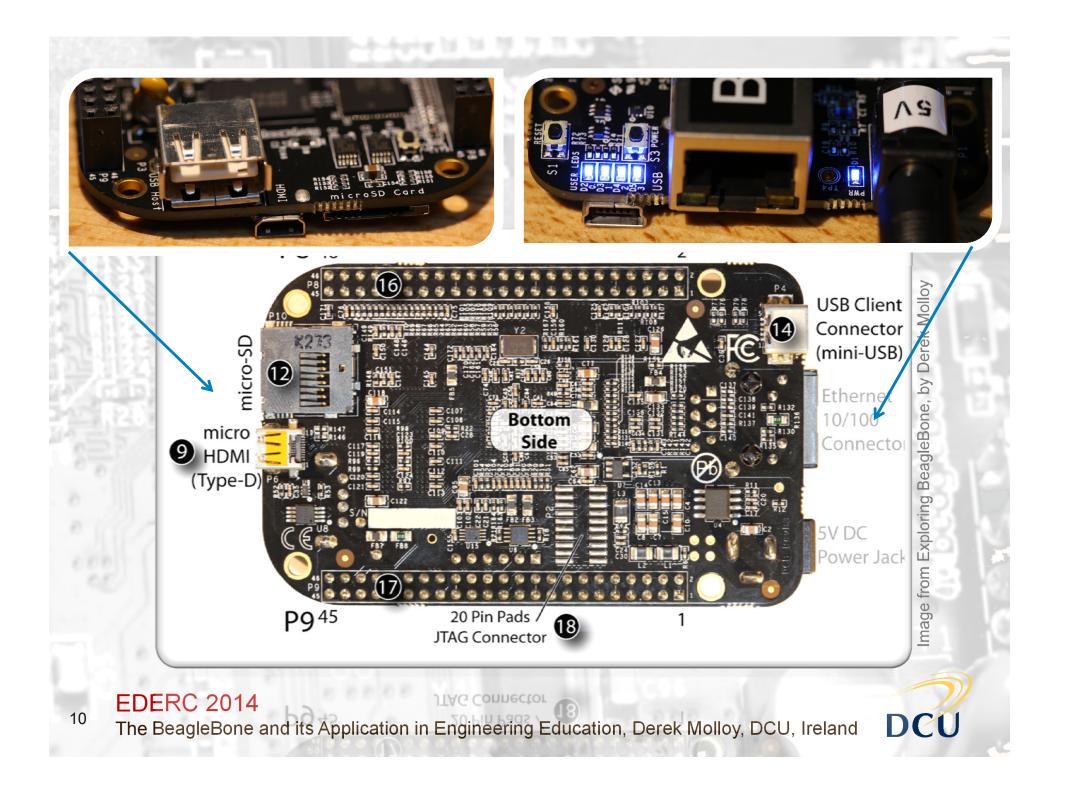
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## **P8 and P9 Headers**

## **Buses**

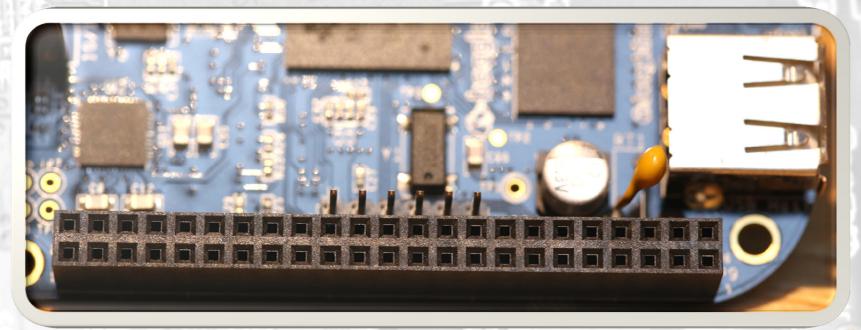
GPIOs (x65) PWM (x8) Analogue Inputs (x7) Timers (x4) Supplies (5V, 3.3V, 1.8V) 

 I<sup>2</sup>C (x2)
 MMC (x2)

 UART (x4)
 LCD

 CAN Bus (x2)
 McASP (x2)

 SPI (x2)
 GPMC



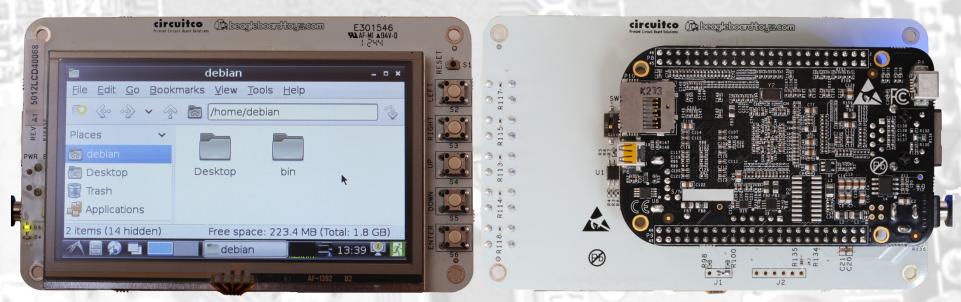
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# EDERC 2014 BeagleBone Black Hardware Capes • Daughter boards

- Attach to P8/P9 headers (stackable)

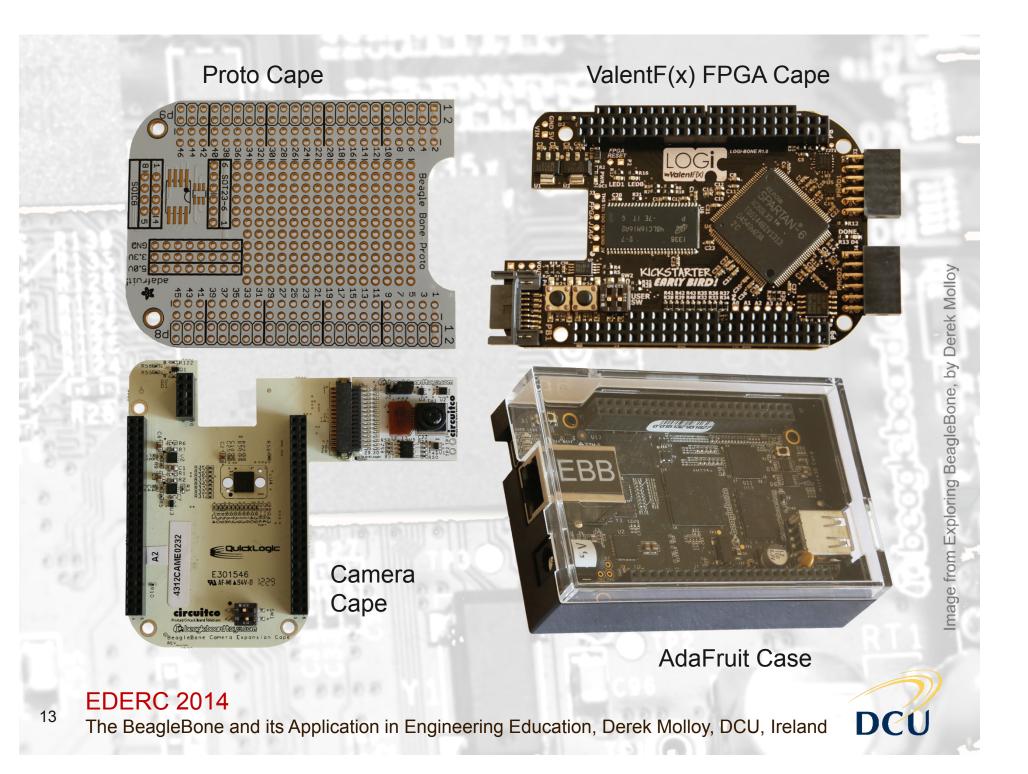


CircuitCo LCD4 Cape

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## Peripherals



Hardware Comparison BeagleBone Black versus Raspberry PI B+, Intel Galileo

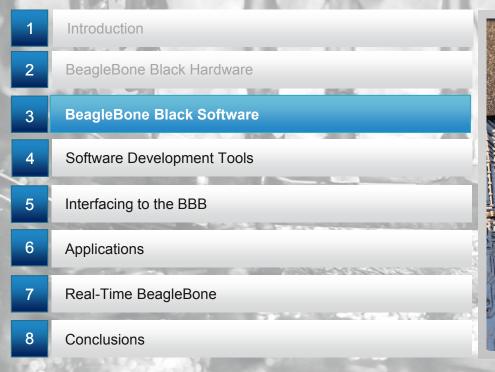
| igleBone Black   | Raspberry PI B+   | Intel Galileo  |
|--|---|--|
| ARM A8 1 GHz 🖌   | 2 ARM A11 700 MHz   | 3 32-bit 400 MHz Quark   |
| 512MB RAM  | 512MB RAM   | 256MB RAM  |
| \$45-55  | \$40 🗸  | \$80   |
| HDMI Video (not full HD)   | HDMI Video Full HD 🗸  | No video   |
| Ethernet 100   | Ethernet 100  | Ethernet 100   |
| Key Features:  | Key Features:   | Key Features:  |
| <ul> <li>eMMC 2GB/4GB</li> <li>Micro SD</li> <li>2 x Programmable real-<br/>time units</li> <li>7 x ADC inputs</li> <li>86 x GPIOs, many buses</li> <li>3D Graphics Accelerator</li> </ul> | <ul> <li>4 x USB slots</li> <li>H264 h/w decoder</li> <li>Micro SD</li> <li>Audio jack output</li> <li>40 GPIOs</li> <li>Camera and DSI display connector</li> <li>3D Graphics Accelerator</li> </ul> | <ul> <li>Arduino Compatible </li> <li>6 x ADC inputs</li> <li>Mini-PCI Express Slot </li> <li>RS-232 Serial Port</li> <li>14 x GPIOs</li> <li>8MB NOR Flash</li> <li>12-bit PWM available</li> </ul> |

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- No such thing!
  - mainline "Linux on an embedded system"
- Embedded Linux:
  - Linux is efficient and scalable
  - Huge number of open-source programs and tools
  - Excellent support for peripherals and devices
  - Downside for real-time non-preemptive by default
- Are non-Linux solutions:
  - TI StarterWare for ARM-based Sitara Processors
  - QNX Neutrino RTOS on OMAP and Sitara

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# BeagleBone Black (BBB) Linux on the BBB



Linux Distributions for BBB:

- Debian specifically packaged.
- Ångström

•

- Ubuntu, Arch etc.
- Boot from eMMC
- Boot from SD using boot image
- Flash eMMC
  - Use flasher image from SD card
- See <u>www.beagleboard.org</u>

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Power is applied or the CPU invokes the reset vector to start the program counter at a defined location in the boot ROM.

#### Texas Instruments Boot ROM (inside AM335x) Internal/First Stage Bootloader

(enough knowledge to access the SD card/eMMC/UART to find the MLO) Fixed at manufacture by Texas Instruments. Performs minimal peripheral configuration, finds boot image, loads x-loader. Derek Molloy

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DCU

#### The X-Loader (MLO on the FAT partition)

Second Stage Bootloader Provided by Texas Instruments. Sets up the pin muxing, initializes clocks & memory, and loads U-Boot.

#### U-Boot (u-boot.img on the FAT partition) Third Stage Bootloader

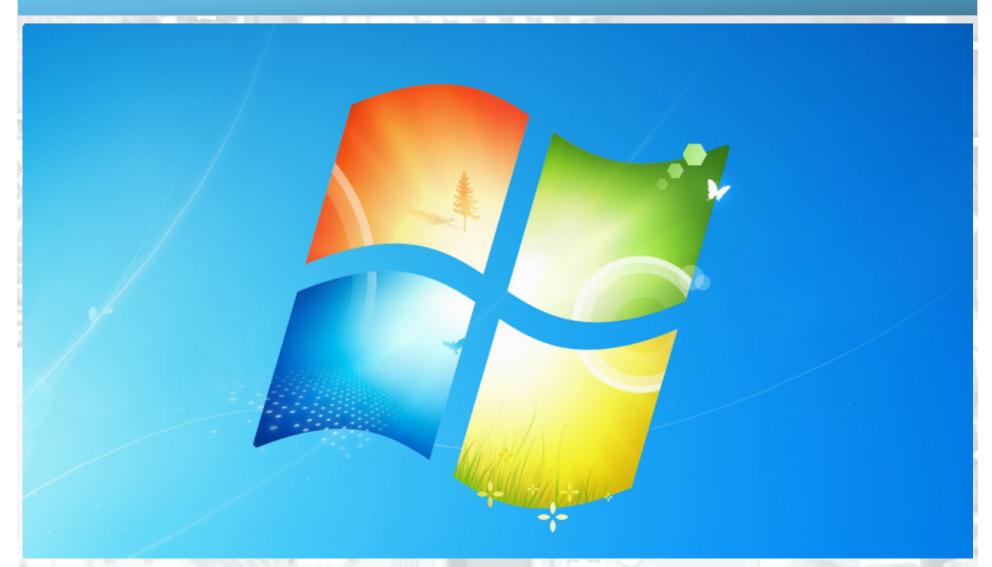
Specifies the root file system. Uses uEnv.txt configuration. Performs additional initialization. Loads and passes control to the Linux kernel.

#### Linux Kernel (Ext4 partition on SD card/eMMC)

Decompresses the kernel into memory, sets up peripherals USB, I<sup>2</sup>C, HDMI etc. Mounts the file system that contains all of the Linux applications.

Calls the first user-space process - init. Moves from kernel context to user context.

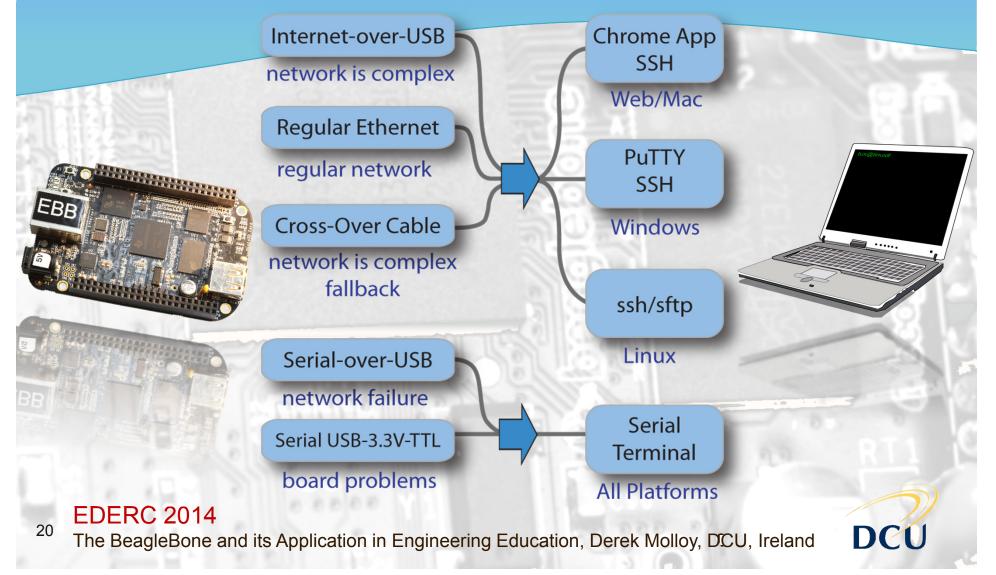
## Connecting to the BeagleBone (Windows):



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## Connecting to the BBB Physical Connections



# BeagleBone Black A First Circuit Example

PMI

GND

-

2

S

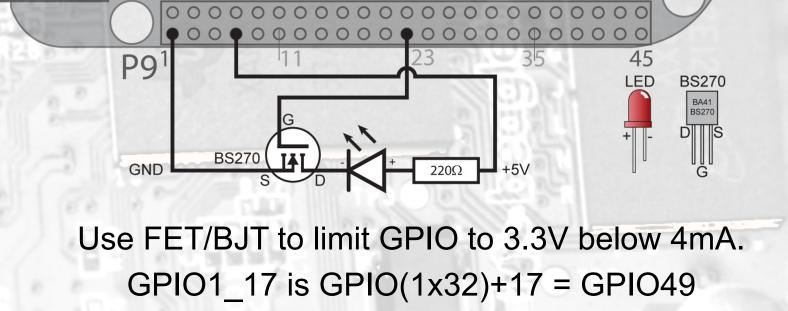
Power LED

5V Power

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GPIO

000 300

6.3

BeagleBone Black



**USB** 

Host

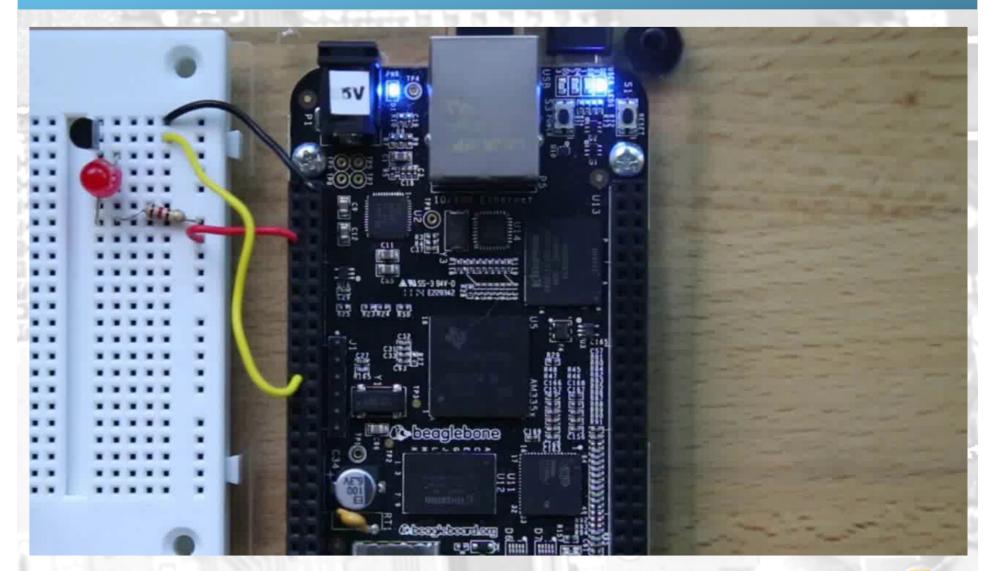
46



age from Exploring BeagleBone, by Derek Molloy

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## Connecting to the BeagleBone (Windows):

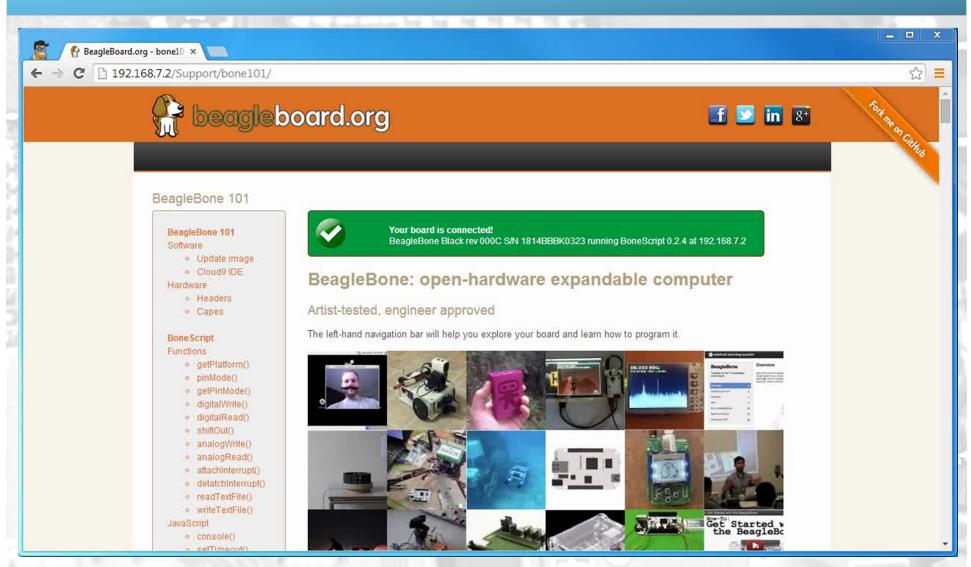


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## Cloud9 IDE, nodejs and BoneScript Example:

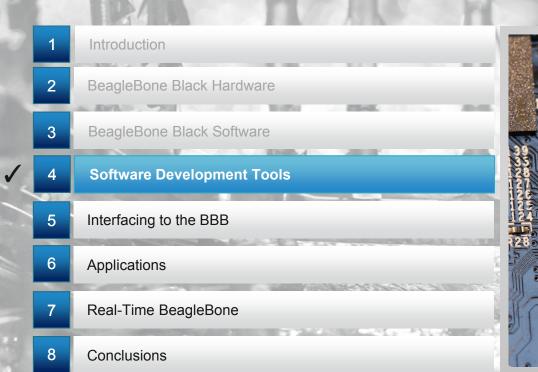


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# Software Development Tools Building C/C++ on the BBB



🗗 molloyd@beaglebone: ~

#### molloyd@beaglebone:~\$ ls \*.cpp

```
testEDERC.cpp
molloyd@beaglebone:~$ more testEDERC.cpp
#include <iostream>
using namespace std;
```

```
int main(){
    cout << "Hello EDERC 2014!" << endl;
    return 0;</pre>
```

```
molloyd@beaglebone:~$ g++ testEDERC.cpp -o testEDERC
molloyd@beaglebone:~$ ./testEDERC
Hello EDERC 2014!
molloyd@beaglebone:~$
```

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# Software Development Tools Cross-Platform Toolchain

- Difficult building large-scale projects on BBB
- Cross-development brings:
  - Typically faster build times
  - Single development point multiple BBB boards
  - Rich UI development environments
- Need a Toolchain
  - Tools (e.g., gcc, gdb) and libraries (e.g., glibc)

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## Cross-compile test running on desktop (64-bit x86) Linux:

```
molloyd@debian:~$ sudo apt-get install g++-4.7-arm-linux-gnueabihf
...
```

```
molloyd@debian:~$ nano testToolchain.cpp
molloyd@debian:~$ more testToolchain.cpp
```

```
#include<iostream>
```

```
using namespace std;
```

```
int main(){
    cout << "Testing Toolchain" << endl;
    return 0;</pre>
```

molloyd@debian:~\$ arm-linux-gnueabihf-g++ testToolchain.cpp -o testARM

- Transfer to BeagleBone (sftp, scp, rsync...) and execute on ARMHF
- Can install a chroot and QEMU to simulate ARM on the desktop Linux image
- Better to link to Integrated Development Environment (IDE) e.g., Eclipse, Qt Creator

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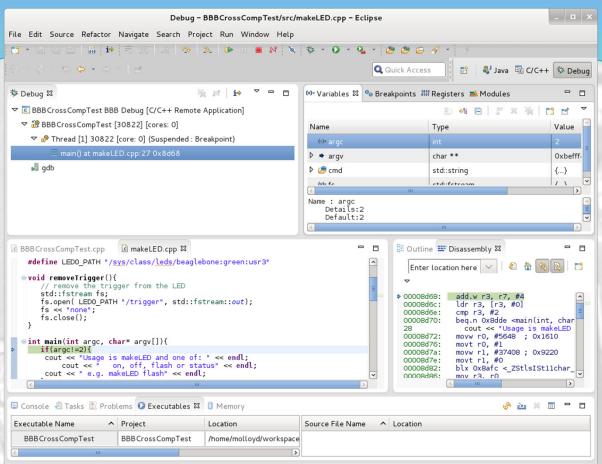
# Software Development Tools Eclipse CDT

## Supports:

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- Cross Platform
   Toolchains
- Multiple Languages
- Remote System
   Explorer (RSE)
- Remote Debug Git/GitHub Integration
- Doxygen Integration



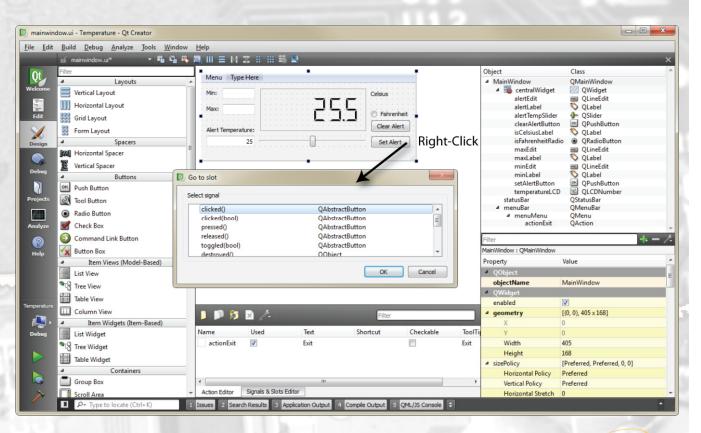
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# Software Development Tools Qt Creator

Supports:

- Cross Platform Toolchains
- Qt GUI Tools
- Remote System Support
- Remote Deploy & Debug Support
- Sockets, Threads, Networking etc.



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## Example Qt Integration Project (display, sensors, UI ...)

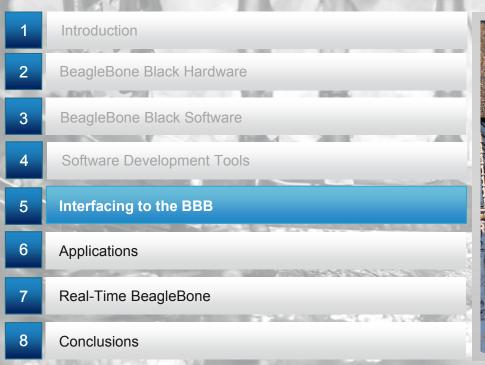
| 5012LCD40068   | circuites Charpterente          |                         |
|--|---------------------------------|-------------------------|
| ZECD   | Derek Molloy DCU QT Application |                         |
|  | Pitch Level: Accelerome         | eter Data:              |
| A REAL PROVIDE A REAL PROVIDA REAL PROVIDE A REAL PROVIDE A REAL PROVIDE A REAL P | Roll Level:                     | Roll In Rotation Level: |
|  |                                 |                         |

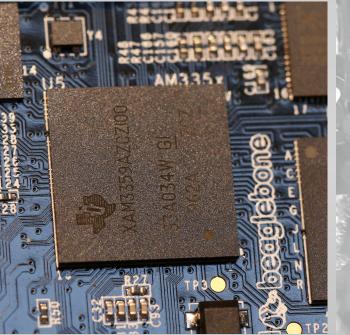
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## **Overview** The BeagleBone: Application in Engineering Education





Interfacing to the BBB Common Interface Types

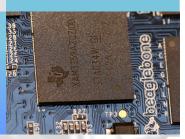
- GPIO Digital Output/Input
- Analog Input
- PWM Output
- Bus interfaces (e.g., I<sup>2</sup>C, SPI, UART)
- USB Devices
- The AM3358/9 has BGA with 324 pins
  - Only 2 x 46 pin headers on the BBB!
  - Need pin mux

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## Default P8 and P9 Pin assignments

|           |       |        |       |             |                         |       |        |       | States in the |                      |
|-----------|-------|--------|-------|-------------|-------------------------|-------|--------|-------|---------------|----------------------|
| Name      | P9    | $\cup$ |       | Name        | Name                    |       | $\cup$ | P8    | Name          | HH                   |
| GND       | P9_01 | 00     | P9_02 | GND         | GND                     | P8_01 | 00     | P8_02 | GND           | N.N.N.N              |
| DC_3.3V   | P9_03 | 00     | P9_04 | DC_3.3V     | GPIO1_6                 | P8_03 | 00     | P8_04 | GPIO1_7       | and a                |
| VDD_5V    | P9_05 | 00     | P9_06 | VDD_5V      | GPIO1_2                 | P8_05 | 00     | P8_06 | GPIO1_3       |                      |
| SYS_5V    | P9_07 | 00     | P9_08 | SYS_5V      | TIMER4                  | P8_07 | 00     | P8_08 | TIMER7        |                      |
| PWR_BUT   | P9_09 | 00     | P9_10 | SYS_RESETn  | TIMER5                  | P8_09 | 00     | P8_10 | TIMER6        | >                    |
| UART4_RXD | P9_11 | 00     | P9_12 | GPIO1_28    | GPIO1_13                | P8_11 | 00     | P8_12 | GPIO1_12      | ollo                 |
| UART4_TXD | P9_13 | 00     | P9_14 | EHRPWM1A    | EHRPWM2B                | P8_13 | 00     | P8_14 | GPIO0_26      | Derek Mollov         |
| GPIO1_16  | P9_15 | 00     | P9_16 | EHRPWM1B    | GPIO1_15                | P8_15 | 00     | P8_16 | GPIO1_14      | A A                  |
| I2C1_SCL  | P9_17 | 00     | P9_18 | I2C1_SDA    | GPIO0_27                | P8_17 | 00     | P8_18 | GPIO2_1       |                      |
| I2C2_SCL  | P9_19 | 00     | P9_20 | I2C2_SDA    | EHRPWM2A                | P8_19 | 00     | P8_20 | GPIO1_31      | 74                   |
| UART2_TXD | P9_21 | 00     | P9_22 | UART2_RXD   | 335GPIO1_30             | P8_21 | 00     | P8_22 | GPIO1_5       |                      |
| GPI01_17  | P9_23 | 00     | P9_24 | UART1_TXD   | GPIO1_4                 | P8_23 | 00     | P8_24 | GPIO1_1       |                      |
| GPIO3_21  | P9_25 | 00     | P9_26 | UART1_RXD   | GPIO1_0                 | P8_25 | 00     | P8_26 | GPIO1_29      | Exploring ReadleBone |
| GPIO3_19  | P9_27 | 00     | P9_28 | SPI1_CS0    | GPIO2_22                | P8_27 | 00     | P8_28 | GPIO2_24      |                      |
| SPI1_D0   | P9_29 | 00     | P9_30 | SPI1_D1     | GPIO2_23                | P8_29 | 00     | P8_30 | GPIO2_25      | ď                    |
| SPI1_SCLK | P9_31 | 00     | P9_32 | VADC        | UART5_CTSN              | P8_31 | 00     | P8_32 | UART5_RTSN    | i.                   |
| AIN4      | P9_33 | 00     | P9_34 | AGND        | UART4_RTSN              | P8_33 | 00     | P8_34 | UART3_RTSN    |                      |
| AIN6      | P9_35 | 00     | P9_36 | AIN5 DIZIVI | <sup>B</sup> UART4_CTSN | P8_35 | 00     | P8_36 | UART3_CTSN    | )<br>L               |
| AIN2      | P9_37 | 00     | P9_38 | AIN3 DDR    | UART5_TXD               | P8_37 | 00     | P8_38 | UART5_RXD     | from                 |
| AINO      | P9_39 | 00     | P9_40 | AIN1        | GPIO2_12                | P8_39 | 00     | P8_40 | GPIO2_13      | fro                  |
| GPIO3_20  | P9_41 | 00     | P9_42 | GPIO0_7     | GPIO2_10                | P8_41 | 00     | P8_42 | GPIO2_11      | anada                |
| GND       | P9_43 | 00     | P9_44 | GND         | GPIO2_8                 | P8_43 | 00     | P8_44 | GPIO2_9       | 8                    |
| GND       | P9_45 | 00     | P9_46 | GND         | GPIO2_6                 | P8_45 | 00     | P8_46 | GPIO2_7       |                      |

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## **P8 Header Pin Allocations:**

| Pin            | \$PINS | ADDR         | GPIO | Name                 | Mode7                  | Mode6               | Mode5               | Mode4               | Mode3               | Mode2               | Mode1          | Mode0          | CPU | Notes          |
|----------------|--------|--------------|------|----------------------|------------------------|---------------------|---------------------|---------------------|---------------------|---------------------|----------------|----------------|-----|----------------|
| P8_01          |        | Offset from: |      | DGND                 |                        |                     |                     |                     |                     |                     |                |                |     | Ground         |
| P8_02          |        | 44e10800     |      | DGND                 |                        |                     |                     |                     |                     |                     |                |                |     | Ground         |
| P8_03          | 6      | 0x818/018    | 38   | GPIO1_6              | gpio1[6]               |                     |                     |                     |                     |                     | mmc1_dat6      | gpmc_ad6       | R9  | Allocated emmo |
| P8_04          | 7      | 0x81c/01c    | 39   | GPI01_7              | gpio1[7]               |                     |                     |                     |                     |                     | mmc1_dat7      | gpmc_ad7       | Т9  | Allocated emm  |
| P8_05          | 2      | 0x808/008    | 34   | GPI01_2              | gpio1[2]               |                     |                     |                     |                     |                     | mmc1_dat2      | gpmc_ad2       | R8  | Allocated emm  |
| P8_06          | 3      | 0x80c/00c    | 35   | GPIO1_3              | gpio1[3]               |                     |                     |                     |                     |                     | mmc1_dat3      | gpmc_ad3       | Т8  | Allocated emme |
| P8_07          | 36     | 0x890/090    | 66   | TIMER4               | gpio2[2]               |                     |                     |                     |                     | timer4              |                | gpmc_advn_ale  | R7  |                |
| P8_08          | 37     | 0x894/094    | 67   | TIMER7               | gpio2[3]               |                     |                     |                     |                     | timer7              |                | gpmc_oen_ren   | T7  |                |
| P8_09          | 39     | 0x89c/09c    | 69   | TIMER5               | gpio2[5]               |                     |                     |                     |                     | timer5              |                | gpmc_be0n_cle  | T6  |                |
| P8_10          | 38     | 0x898/098    | 68   | TIMER6               | gpio2[4]               |                     |                     |                     |                     | timer6              |                | gpmc_wen       | U6  |                |
| P8_11          | 13     | 0x834/034    | 45   | GPI01_13             | gpio1[13]              | pr1_pru0_pru_r30_15 |                     | eQEP2B_in           | mmc2_dat1           | mmc1_dat5           | lcd_data18     | gpmc_ad13      | R12 |                |
| P8_12          | 12     | 0x830/030    | 44   | GPI01_12             | gpio1[12]              | pr1_pru0_pru_r30_14 |                     | EQEP2A_IN           | MMC2_DAT0           | MMC1_DAT4           | LCD_DATA19     | GPMC_AD12      | T12 |                |
| P8_13          | 9      | 0x824/024    | 23   | EHRPWM2B             | gpio0[23]              |                     |                     | ehrpwm2B            | mmc2_dat5           | mmc1_dat1           | lcd_data22     | gpmc_ad9       | T10 |                |
| P8_14          | 10     | 0x828/028    | 26   | GPI00_26             | gpio0[26]              |                     |                     | ehrpwm2_tripzone_in | mmc2_dat6           | mmc1_dat2           | lcd_data21     | gpmc_ad10      | T11 |                |
| P8_15          | 15     | 0x83c/03c    | 47   | GPI01_15             | gpio1[15]              | pr1_pru0_pru_r31_15 |                     | eQEP2_strobe        | mmc2_dat3           | mmc1_dat7           | lcd_data16     | gpmc_ad15      | U13 |                |
| P8_16          | 14     | 0x838/038    | 46   | GPI01_14             | gpio1[14]              | pr1_pru0_pru_r31_14 |                     | eQEP2_index         | mmc2_dat2           | mmc1_dat6           | lcd_data17     | gpmc_ad14      | V13 |                |
| P8_17          | 11     | 0x82c/02c    | 27   | GPI00_27             | gpio0[27]              |                     |                     | ehrpwm0_synco       | mmc2_dat7           | mmc1_dat3           | lcd_data20     | gpmc_ad11      | U12 |                |
| P8_18          | 35     | 0x88c/08c    | 65   | GPIO2_1              | gpio2[1]               | mcasp0_fsr          |                     |                     | mmc2_clk            | gpmc_wait1          | lcd_memory_clk | gpmc_clk_mux0  | V12 |                |
| P8_19          | 8      | 0x820/020    | 22   | EHRPWM2A             | gpio0[22]              |                     |                     | ehrpwm2A            | mmc2_dat4           | mmc1_dat0           | lcd_data23     | gpmc_ad8       | U10 |                |
| P8_20          | 33     | 0x884/084    | 63   | GPI01_31             | gpio1[31]              | pr1_pru1_pru_r31_13 | pr1_pru1_pru_r30_13 |                     |                     | mmc1_cmd            | gpmc_be1n      | gpmc_csn2      | V9  | Allocated emm  |
| P8_21          | 32     | 0x880/080    | 62   | GPI01_30             | gpio1[30]              | pr1_pru1_pru_r31_12 | pr1_pru1_pru_r30_12 |                     |                     | mmc1_clk            | gpmc_clk       | gpmc_csn1      | U9  | Allocated emm  |
| P8_22          | 5      | 0x814/014    | 37   | GPIO1_5              | gpio1[5]               |                     |                     |                     |                     |                     | mmc1_dat5      | gpmc_ad5       | V8  | Allocated emm  |
| P8_23          | 4      | 0x810/010    | 36   | GPIO1_4              | gpio1[4]               |                     |                     |                     |                     |                     | mmc1_dat4      | gpmc_ad4       | U8  | Allocated emm  |
| P8_24          | 1      | 0x804/004    | 33   | GPIO1_1              | gpio1[1]               |                     |                     |                     |                     |                     | mmc1_dat1      | gpmc_ad1       | V7  | Allocated emm  |
| P8_25          | 0      | 0x800/000    | 32   | GPIO1_0              | gpio1[0]               |                     |                     |                     |                     |                     | mmc1_dat0      | gpmc_ad0       | U7  | Allocated emm  |
| P8_26          | 31     | 0x87c/07c    | 61   | GPIO1_29             | gpio1[29]              |                     |                     |                     |                     |                     |                | gpmc_csn0      | V6  |                |
| P8_27          | 56     | 0x8e0/0e0    | 86   | GPI02_22             | gpio2[22]              | pr1_pru1_pru_r31_8  | pr1_pru1_pru_r30_8  |                     |                     |                     | gpmc_a8        | lcd_vsync      | U5  | Allocated HD   |
| P8_28          | 58     | 0x8e8/0e8    | 88   | GPI02_24             | gpio2[24]              | pr1_pru1_pru_r31_10 | pr1_pru1_pru_r30_10 |                     |                     |                     | gpmc_a10       | lcd_pclk       | V5  | Allocated HDM  |
| P8_29          | 57     | 0x8e4/0e4    | 87   | GPI02_23             | gpio2[23]              | pr1_pru1_pru_r31_9  | pr1_pru1_pru_r30_9  |                     |                     |                     | gpmc_a9        | lcd_hsync      | R5  | Allocated HD   |
| P8_30          | 59     | 0x8ec/0ec    | 89   | GPI02_25             | gpio2[25]              |                     |                     |                     |                     |                     | gpmc_a11       | lod_ac_bias_en | R6  | Allocated HDM  |
| P8_31          | 54     | 0x8d8/0d8    | 10   | UART5_CTSN           | gpio0[10]              | uart5 ctsn          |                     | uart5_rxd           | mcasp0 axr1         | eQEP1_index         | gpmc_a18       | lcd data14     | V4  | Allocated HDI  |
| P8_32          | 55     | 0x8dc/0dc    | 11   | UART5_RTSN           | gpio0[11]              | uart5_rtsn          |                     | mcasp0_axr3         | mcasp0_ahdkx        | eQEP1_strobe        | gpmc_a19       | lcd_data15     | T5  | Allocated HDI  |
| P8_33          | 53     | 0x8d4/0d4    | 9    | UART4_RTSN           | gpio0[9]               | uart4_rtsn          |                     | mcasp0_axr3         | mcasp0_fsr          | eQEP1B_in           | gpmc_a17       | lcd_data13     | V3  | Allocated HDN  |
| P8_34          | 51     | 0x8cc/0cc    | 81   | UART3_RTSN           | gpio2[17]              | uart3_rtsn          |                     | mcasp0_axr2         | mcasp0_ahclkr       | ehrpwm1B            | gpmc_a15       | lcd_data11     | U4  | Allocated HDN  |
| P8_35          | 52     | 0x8d0/0d0    | 8    | UART4_CTSN           | gpio0[8]               | uart4_ctsn          |                     | mcasp0_axr2         | mcasp0_aclkr        | eQEP1A_in           | gpmc_a16       | lcd_data12     | V2  | Allocated HDI  |
| P8_36          | 50     | 0x8c8/0c8    | 80   | UART3_CTSN           | gpio2[16]              | uart3_ctsn          |                     |                     | mcasp0_axr0         | ehrpwm1A            | gpmc_a14       | lcd_data10     | U3  | Allocated HDN  |
| P8_37          | 48     | 0x8c0/0c0    | 78   | UART5_TXD            | gpio2[14]              | uart2_ctsn          |                     | uart5_txd           | mcasp0_aclkx        | ehrpwm1_tripzone_in | gpmc_a12       | lcd_data8      | U1  | Allocated HDM  |
| P8 38          | 49     | 0x8c4/0c4    | 79   | UART5_RXD            | gpio2[15]              | uart2_rtsn          |                     | uart5_rxd           | mcasp0_fsx          | ehrpwm0_synco       | gpmc_a13       | lod data9      | U2  | Allocated HDI  |
| P8_39          | 46     | 0x8b8/0b8    | 76   | GPI02_12             | gpio2[12]              | pr1_pru1_pru_r31_6  | pr1_pru1_pru_r30_6  |                     | eQEP2_index         |                     | gpmc_a6        | lod data6      | T3  | Allocated HDI  |
| P8 40          | 47     | 0x8bc/0bc    | 77   | GPI02_13             | gpio2[12]              | pr1_pru1_pru_r31_7  | pr1_pru1_pru_r30_7  | pr1_edio_data_out7  | eQEP2_strobe        |                     | gpmc_a7        | lod data7      | T4  | Allocated HDI  |
| P8_41          | 44     | 0x8b0/0b0    | 74   | GPI02_10             | gpio2[10]              | pr1_pru1_pru_r31_4  | pr1_pru1_pru_r30_4  | p                   | eQEP2A_in           |                     | gpmc_a4        | lcd_data4      | T1  | Allocated HDM  |
| P8_42          | 45     | 0x8b4/0b4    | 75   | GPI02_10<br>GPI02_11 | gpio2[10]<br>gpio2[11] | pr1_pru1_pru_r31_5  | pr1_pru1_pru_r30_5  |                     | eQEP28_in           |                     | gpmc_a4        | lcd_data5      | T2  | Allocated HDM  |
| P8_43          | 42     | 0x8a8/0a8    | 72   | GPI02_11<br>GPI02_8  | gpio2[11]<br>gpio2[8]  | pr1_pru1_pru_r31_2  | pr1_pru1_pru_r30_2  |                     | ehrpwm2 tripzone in |                     | gpmc_a3        | lcd_data3      | R3  | Allocated HD/  |
| P8_44          | 42     | 0x8ac/0ac    | 72   | GPI02_8<br>GPI02_9   | gpio2[9]               |                     |                     |                     | ehrpwm0_synco       |                     |                | lcd_data2      | R4  | Allocated HDM  |
| P8_45          | 40     | 0x8a0/0a0    | 70   | GPI02_9<br>GPI02_6   | gpio2[9]<br>gpio2[6]   | pr1_pru1_pru_r31_3  | pr1_pru1_pru_r30_3  |                     |                     |                     | gpmc_a3        | lcd_data0      | R1  | Allocated HDM  |
| P8_45<br>P8_46 | 40     | 0x8a0/0a0    | 70   | GPI02_6<br>GPI02_7   |                        | pr1_pru1_pru_r31_0  | pr1_pru1_pru_r30_0  |                     | ehrpwm2A            |                     | gpmc_a0        | -              | R2  |                |
|                |        | 00034/034    | /1   | GMUZ /               | gpio2[7]               | pr1_pru1_pru_r31_1  | pr1_pru1_pru_r30_1  |                     | ehrpwm2B            |                     | gpmc_a1        | lcd data1      | rc2 | Allocated HDN  |

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## Interfacing to the BBB Device Tree Overlays

- 0x27 (0100111) Fast, Input, Pull-Down, Enabled and Mux Mode 7
- 0x37 (0110111) Fast, Input, Pull-Up, Enabled, Mux Mode 7
- 0x07 (0000111) Fast, Output, Pull-down, Enabled, Mux Mode 7
- 0x17 (0010111) Fast, Output, Pull-up, Enabled, Mux Mode 7

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# Interfacing to the BBB Cape Manager

molloyd@beaglebone:/lib/firmware\$ sudo su
root@beaglebone:/lib/firmware# echo EBB-GPIO-Example > \$SLOTS
root@beaglebone:/lib/firmware# cat \$SLOTS

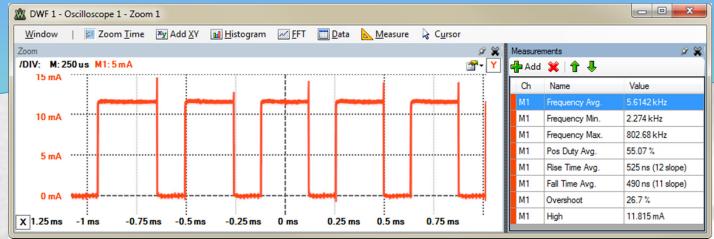
- 0: 54:PF---
- 1: 55:PF---
- 2: 56:PF---
- 3: 57:PF---
- 4: ff:P-O-L Bone-LT-eMMC-2G,00A0,Texas Instrument,BB-BONE-EMMC-2G
- 5: ff:P-O-L Bone-Black-HDMI,00A0,Texas Instrument,BB-BONELT-HDMI
- 6: ff:P-O-L Override Board Name,00A0,Override Manuf, EBB-GPIO-Example
- Allows pins to be allocated for capes
- Virtual capes
  - Build overlays using the device tree compiler
  - Can add and remove dynamically or on boot

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## Interfacing to the BBB Digital Output



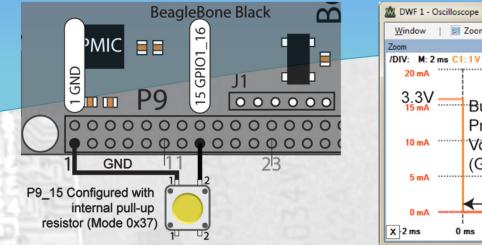
- C/C++ Linux userspace code available
  - Perfect for low-frequency switching
  - Limited switching frequency, suffers from jitter
  - Can directly memory switch (dangerous?)
  - Can use the PRU-ICSS

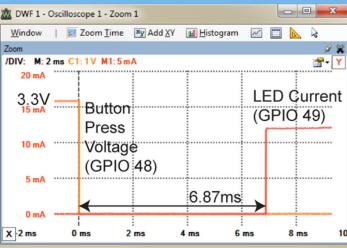
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## Interfacing to the BBB Digital Input





- C/C++ Linux userspace code available
  - Must configure internal resistor characteristics
  - Response latency as low as 324µS in Linux
  - GPIO-Keys allows for generalized interface
  - Can directly memory switch (dangerous?)
  - Can use the PRU-ICSS

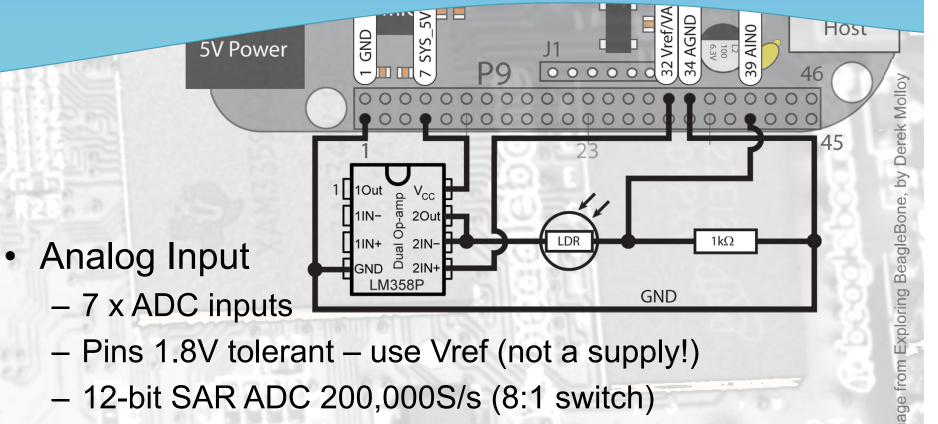
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## Interfacing to the BBB **Analogue Input**



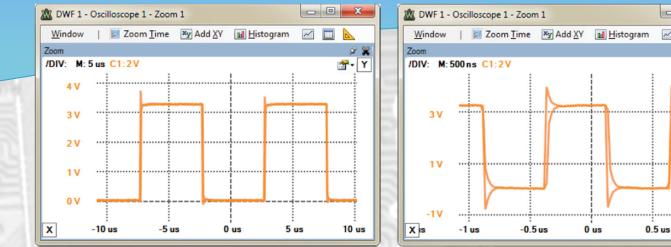
- 12-bit SAR ADC 200,000S/s (8:1 switch)
- Load device tree overlay, C/C++ code available

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# Interfacing to the BBB PWM Output 50% @ 100 kHz



Pulse Width Modulation (PWM) Outputs
 – 14 x PWM (configurable from Linux userspace)

/sys/devices/ocp.3/pwm\_test\_P9\_22.15\$ sudo su
/sys/devices/ocp.3/pwm\_test\_P9\_22.15# echo 5000 > duty
/sys/devices/ocp.3/pwm\_test\_P9\_22.15# echo 10000 > period
/sys/devices/ocp.3/pwm\_test\_P9\_22.15# echo 1 > run

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50% @ 1 MHz

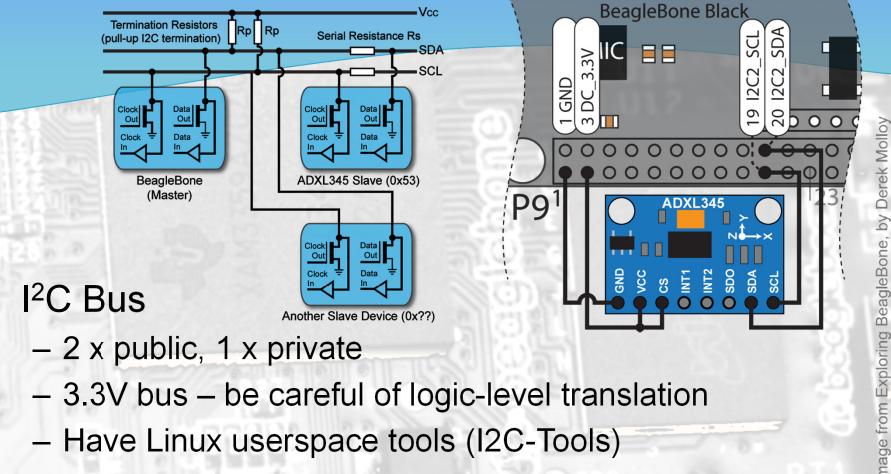
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## Interfacing to the BBB **I<sup>2</sup>C** Interface

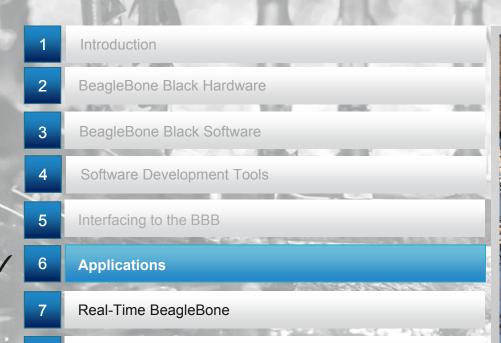


- 2 x public, 1 x private
- 3.3V bus be careful of logic-level translation
- Have Linux userspace tools (I2C-Tools)
- Can use Linux ioctl calls to control the bus in C/C++

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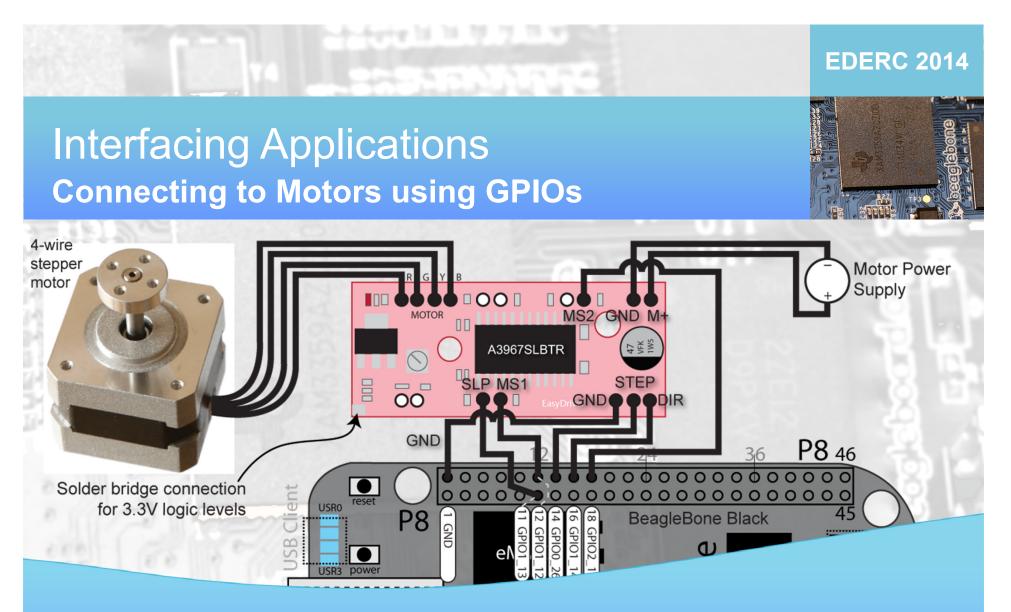
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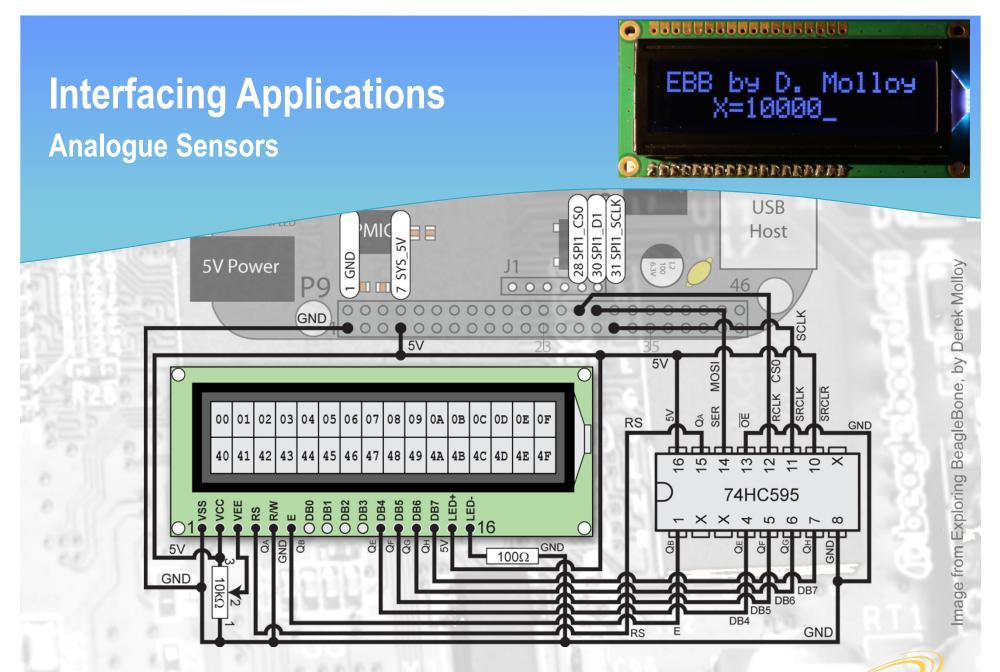


8 Conclusions





- Motor boards (e.g., TI DRV8835), stepper boards
- Interface to servo motors using PWM pins
- Can integrate Posix threads, wrap with classes



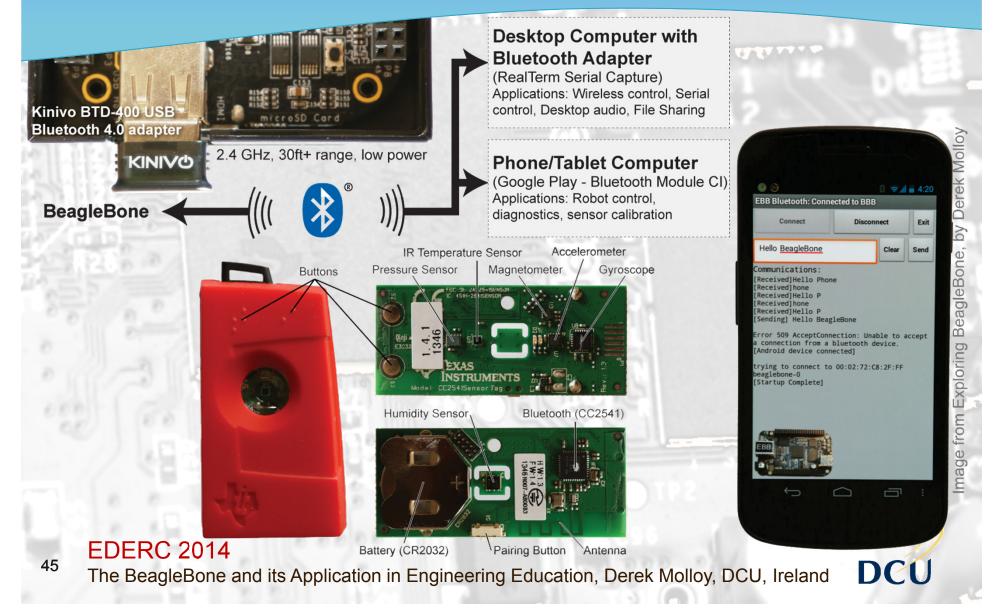
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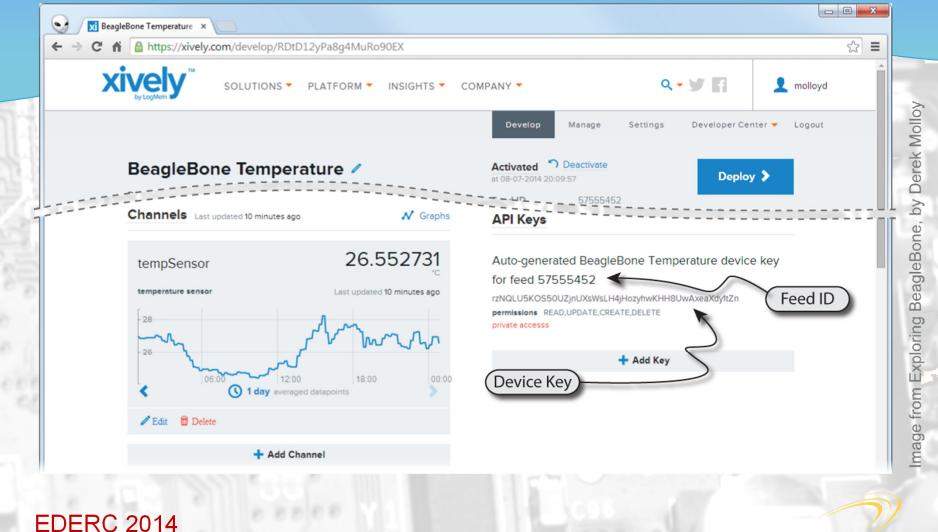
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## Interfacing Applications Analogue Sensors



### Interfacing Applications Platform as a Service (PaaS)

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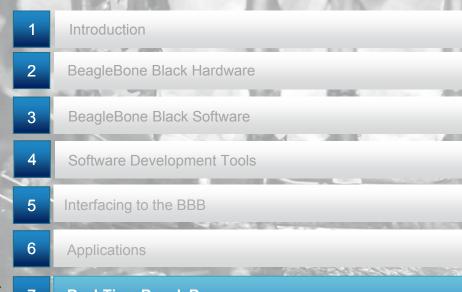




## Interfacing Applications Video, image processing, computer vision Audio input, output and streaming



### **Overview** The BeagleBone: Application in Engineering Education





Conclusions

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## Real-time BeagleBone Real-time on the BBB

- Limitations of non-preemptive Linux...
- Real-Time Kernels (preemptive Linux)
  - RT-Preempt patch (PREEMPT\_RT)
  - Xenomai co-kernel
- Interface BBB to Stellaris (e.g., using UART)
- Use the AM3358 PRU-ICSS
  - Programmable real-time units and industrial communication sub-system
  - 2 x PRUs @ 400 MHz, 5ns per instruction
  - small RISC ISA (~45 instructions)
  - 8KB instruction memory + 8KB data RAM for each PRU
  - 12KB shared memory and full access to Linux memory space

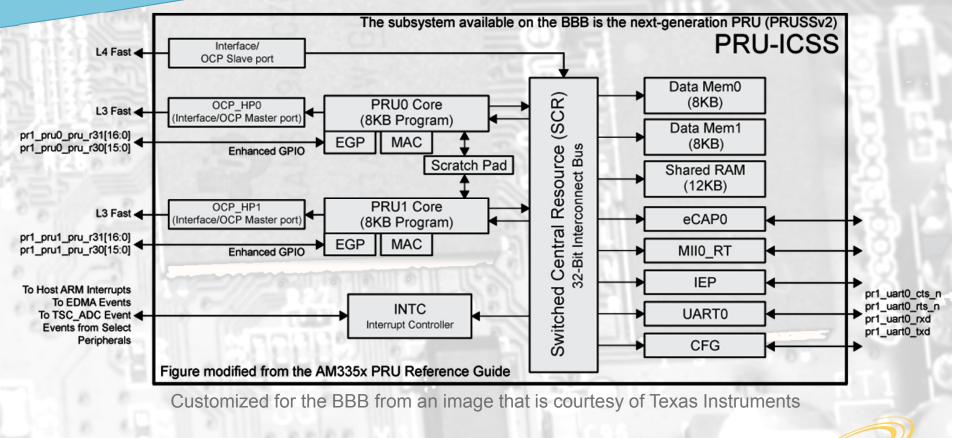
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## Real-time BeagleBone Architecture

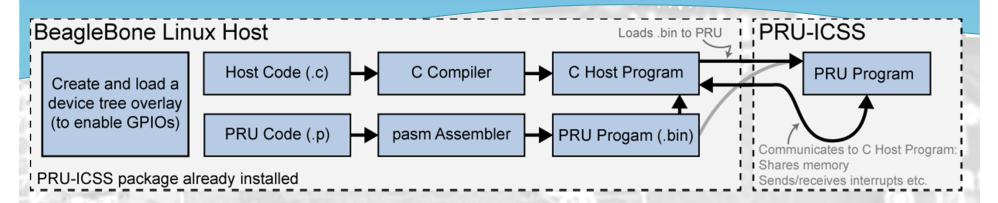


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## Real-Time BeagleBone Deploying Program to one of the PRUs



- PRU has access to Enhanced GPIOs
  - Use device tree overlay to set up the PRU EGPIOs
  - Access to Linux memory slower than PRU local memory
- C Host program loads PRU binary into PRU
  - Shares memory with the host (PRU memory mapped to userspace)
  - Use interrupts to trigger events

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### ledButton.p

| .origin 0<br>.entrypoint ST   | ART                 |     | start of program in PRU memory<br>program entry point (for a debugger)                                      |  |  |
|---|---------------------|-----|---|--|--|
| #define INS_PE<br>#define INS_PE  | _                   | //  | 5ns per instruction<br>two instructions per delay loop<br>set up a 50ms delay                               |  |  |
| #define PRU0_R  | 31_VEC_VALID 32     | PER | US / INS_PER_DELAY_LOOP)<br>allows notification of program completion<br>the event number that is sent back |  |  |
| START:<br>SET<br>MOV<br>DELAYON:  | r30.t5<br>r0, DELAY |     | turn on the output pin (LED on)<br>store the length of the delay in REGO                                    |  |  |
| SUB<br>QBNE<br>LEDOFF:  |                     |     | Decrement REG0 by 1<br>Loop to DELAYON, unless REG0=0   |  |  |
| CLR<br>MOV<br>DELAYOFF:   | r30.t5<br>r0, DELAY |     | clear the output bin (LED off)<br>Reset REGO to the length of the delay                                     |  |  |
| SUB<br>QBNE<br>QBBC   | DELAYOFF, r0, 0     | 11  | decrement REG0 by 1<br>Loop to DELAYOFF, unless REG0=0<br>is the button pressed? If not, loop               |  |  |
| END :<br>MOV<br>HALT  | r31.b0, PRU0_R31_   | VE  | notify the calling app that finished<br><b>C_VALID   PRU_EVTOUT_0</b><br>halt the pru program               |  |  |
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### ledButton.c

#include <stdio.h>
#include <prussdrv.h>
#include <pruss\_intc\_mapping.h>
#define PRU\_NUM 0 // using PRU0 for these examples

#### void main (void)

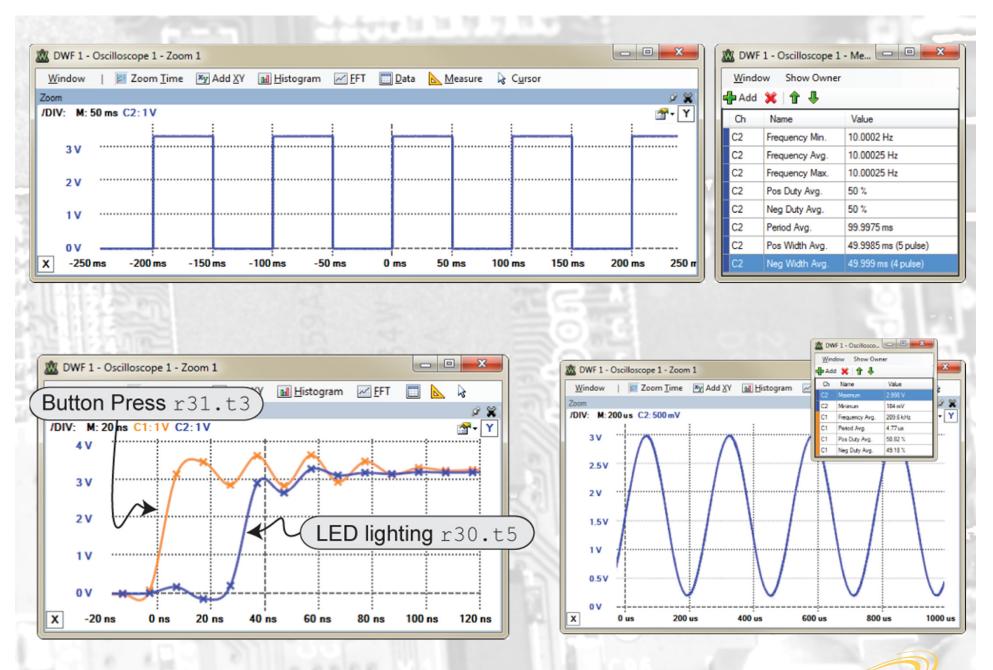
#### {

// Initialize structure used by prussdrv pruintc intc // PRUSS INTC INITDATA is found in pruss intc mapping.h tpruss intc initdata pruss intc initdata = PRUSS INTC INITDATA; // Allocate and initialize memory prussdrv init (); prussdrv open (PRU EVTOUT 0); // Map PRU's interrupts prussdrv pruintc init(&pruss intc initdata); // Load and execute the PRU program on the PRU prussdrv exec program (PRU NUM, "./ledButton.bin"); // Wait for event completion from PRU, returns the PRU EVTOUT 0 number int n = prussdrv pru wait event (PRU EVTOUT 0); printf("EBB PRU program completed, event number %d.\n", n); // Disable PRU and close memory mappings prussdrv pru disable(PRU NUM); prussdrv exit();

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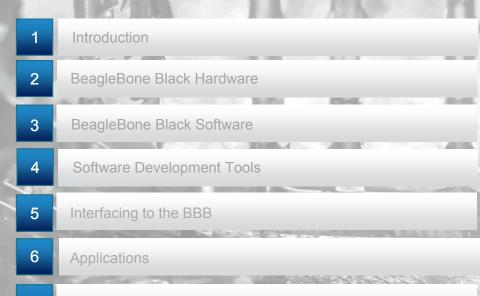


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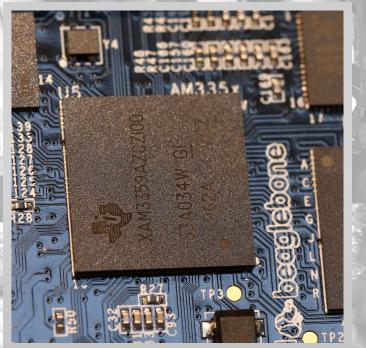


### **Overview** The BeagleBone: Application in Engineering Education



Real-Time BeagleBone

#### 8 Conclusions



### Conclusions

Positives and Negatives of the BBB in Education



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#### Positives

#### Low-cost per unit

Practical integration of electronics, software and Linux

Exposure to embedded Linux

USB-over-Internet on-campus

Easy to burn new image to eMMC

Great for project work

#### **Negatives**

Supply of boards constrained

Difficult to support range of software/hardware issues that can arise – especially corporate laptops!

Embedded Linux is a moving target

Device tree overlays complex

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#### Introduction

I have developed a full series of videos on the started. The Beadlebone original retailed for a videos will describe the Beaglebone Black, w cost of €45.

#### Getting Started

In the first video I introduce the Beaglebone DDR2 Memory. It has full support for 10/100 x 12-bit ADCs and support for canbus and the board. The Beaglebone boots using the M demonstrate the first steps with the board a values to the input/output pins and the 4



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BEAGLEBONE



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~ 576 pages Describes everything in this presentation (properly!)

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