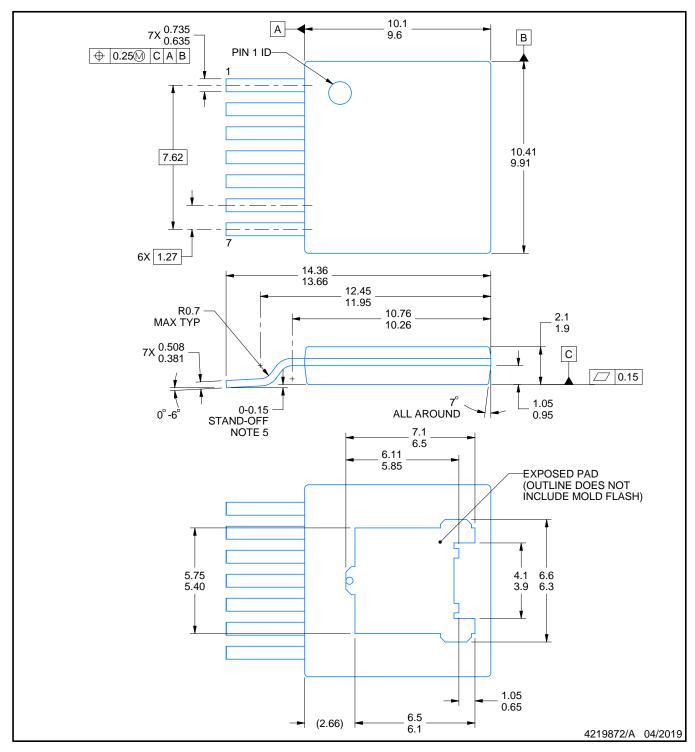


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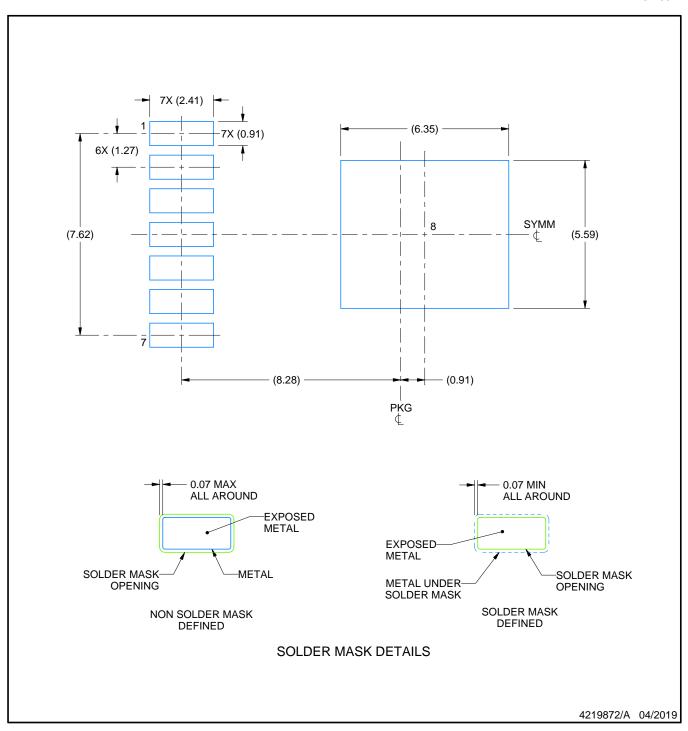
NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.
- Features may not exist and shape may vary per different assembly sites.
 Reference JEDEC registration TO-279B.
- 5. Under all conditions, leads must not be above Datum C



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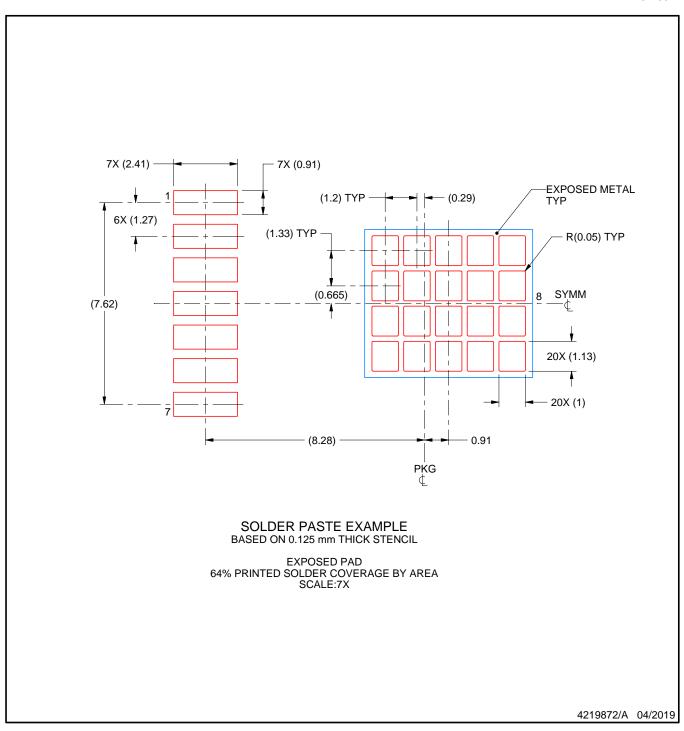
NOTES: (continued)



^{6.} This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).

^{7.} Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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NOTES: (continued)



^{8.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations

design recommendations.

9. Board assembly site may have different recommendations for stencil design.

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