Application Report
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Architectural Lighting Design Powered by All-In-One LED Driver TLC5970, with Integrated 36-V DC-DC Converter and Differential Signal Interface

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ABSTRACT

This application report describes how to power architectural lighting designs using the TLC5970, a three-channel, constant-current sink driver with a buck dc/dc converter and differential signal interface. A reference design is provided, along with the experimental results.

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1 Introduction

LED technology is advancing rapidly, creating opportunities for new, innovative lighting products. LED-based designs are completely changing the way lighting engineers approach the architectural-illumination segment of the market. There are a number of definitions for *architectural* lighting, but in the context of this application report, it is the illumination of buildings and other large structures for the purpose of enhancing their appearance and emotional impact. LEDs have many advantages versus traditional light sources, the key ones being higher efficacy (lumens output per watts input), long-life (50,000 hours and beyond), and the ability to produce billions of colors by mixing red, green, and blue LEDs. In the context of creating flexible, energy-friendly, low-maintenance methods of decorating skyscrapers, bridges, monuments, or other large edifices with light, LEDs are the clear choice. Architectural lighting differs from LED signage and video displays in several key ways that creates the need for specialized drivers for this purpose. Table 1 lists these differences.

Table 1. LED Display Versus Architectural Lighting

Feature	LED Display	Architectural Lighting
Pixel Pitch	5 mm to 25 mm	5 mm to > 30 m
LED Current	< 50 mA	20 mA to 350 mA
Data Communication	SPI	SPI, differential, single wire, DMX512
LED Driver Cascading	Usually fewer than 20 drivers	Modules unlimited
Display Structure	Cabinet / frame	Molds to shape of the architectural object. Can be straight or curved.
Power Distribution	AC input to 5-V dc output (typical case)	AC Input to intermediate dc (36 V or 24 V) or power transmission. Intermediate dc to VLED.
Control System	Video display control system	Light effects (color, brightness, pattern changing) control system

To facilitate the creation of innovative architectural lightscapes, Texas Instruments has developed the TLC5970 3-channel, 12-bit pulse-width modulated (PWM) LED driver with integrated buck dc-dc converter. It has a number of features making it ideally suited for architectural lighting applications. Key highlights are shown in Table 2.

Table 2. TLC5970 Key Features

Feature		Benefit
Flexible control signal interface: Can support single-ended or differential inputs.		Single-ended - low communications wire count, pixel spacing to 2 meters.
		Differential - robust signal interface, pixel distances of over 30 meters.
Data transfer rate: 20 MHz with unlimited driver cascading.		Fast data update to create a variety of visual effects with long cascaded drivers.
Integrated dc-dc conversion with automatic LED anode voltage control.		Matches standard 12-V, 24-V, or 36-V power supplies to LED string voltage for energy efficiency, lower-weight power transmission system, and compact size.
LED and driver protection: LED open, buck short-circuit, prethermal warning, and Thermal shutdown.		Protects LEDs and LED driver from abnormal and fault conditions.
12-bit grayscale PWM		68 billion color combinations
7-bit global brightness control		Universal adjustment of led brightness
7-bit dot correction		Compensate for variations in LED forward voltage and brightness for setting true white balance
Accuracy	Channel-to-channel: ±1% (typ)	Precision LED current matching between pixels for uniform light appearance
	Device-to-device: ±3% (typ)	
Integrated EEPROM		Flexible configuration: stores dot correction data for white balancing LED pixels
0-mA to 150-mA constant current per channel		Can be used with modern high-brightness LEDs.

In addition to these features, several other flexible features of the TLC5970 are:

- While the optimal use of the TLC5970 is for driving RGB LEDs in a single RGB pixel format, mono and bicolor LED configurations can be easily implemented.
- The outputs of the TLC5970 can be combined in parallel for driving LEDs at higher currents (up to 450 mA)
- The buck converter is not required for operation. A single 5-V power supply can be used to power the TLC5970, and single string LEDs connected to each output.

By comparison, standard LED drivers used in LED signage have some similar features, but the lack of long-distance communication and high current capability make them less suited for many architectural lighting applications.

2 TLC5970 Initial Configuration

Figure 1 shows the TLC5970 initial configuration flow.

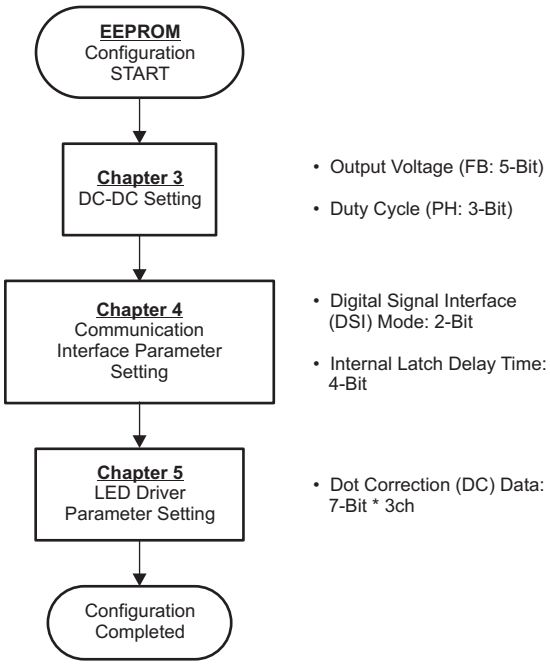


Figure 1. TLC5970 Initial EEPROM Setting Flow

The TLC5970 integrates EEPROM preprogramming capability for application flexibility, and minimizes the external parts. Only five parameters must be considered on TLC5970 initial setup: two for the dc-dc converter, two for the differential communication interface, and one for the LED driver.

It is necessary to write these EEPROM register values with the standard sequence shown in Figure 2. VROM voltage (19 ±0.5 V) is required to write these EEPROM values.

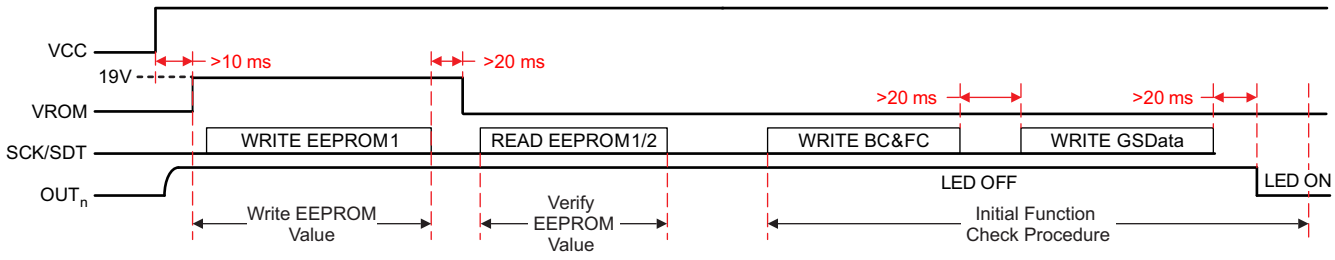


Figure 2. TLC5970 Initial EEPROM Configuration and Verification

3 Buck Converter Design

The TLC5970 integrates a high-efficiency buck converter for the LED supply, and always operates in pulse frequency modulation (PFM) mode to provide the best efficiency to the LED load. The output voltage is automatically regulated depending on LED load conditions:

1. *Preboost* function. The buck converter is programmed to start before the LEDs turn on. This compensates the steep drop in output voltage caused by the LEDs inrush current when turning on.
2. Automatically optimizes lowest OUT_n voltage to 1 V in order to avoid unnecessary power dissipation. In spite of the LED forward voltage change as a result of temperature or current changes, the integrated analog-to-digital converter (ADC) reads the OUT_n voltage levels. Based on this information, the buck converter output is automatically optimized to keep the lowest OUT_n to 1 V. Figure 3 illustrates this automatically-adjusting VLED capability at heat and cool cycles.

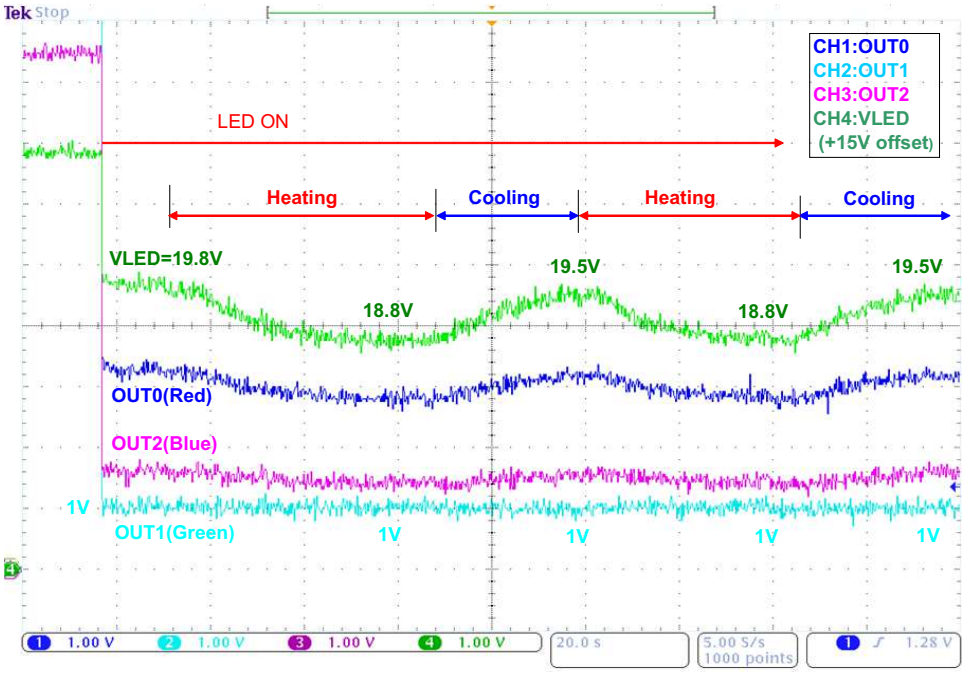


Figure 3. TLC5970 Output Voltage Optimization on Heat and Cool Cycle, Four Series LEDs and 150 mA/CH

The following three steps of the dc-dc converter design are described in the next sections:

1. Setting the target voltage, VLED
2. Setting the dc-dc duty cycle, D
3. Selecting the Inductance based on current consumption

3.1 Setting the Target Voltage, VLED

The first step of dc-dc converter design is always to set the target output voltage to supply the three LED strings.

Here, the target output voltage is defined by the series count of LEDs multiplied by the LED forward voltage (V_f) plus the minimum sustaining voltage on OUT_n to keep the required constant current, as shown in Equation 1. The TLC5970 is designed to automatically keep this minimum voltage at 1.0 V. Figure 4 shows this scheme.

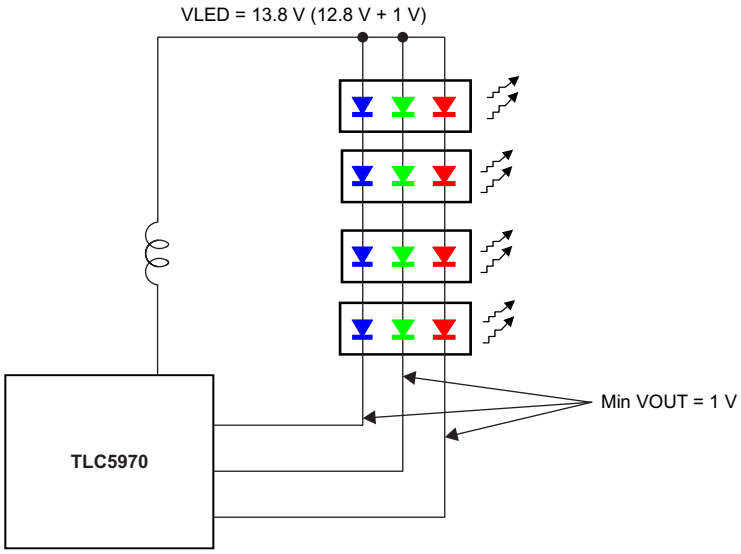


Figure 4. DC-DC Output Voltage Autoadjusted for LED Strings

For example, if your configuration uses four series-connected LEDs and the LED forward voltage is 3.2 V for the required LED current range, then the target output voltage is 13.8 V.

$$VLED = V_f \times Series\_LED\_Count + 1.0\ (V) \quad (1)$$

When using the TLC5970, set the target output voltage by setting an EEPROM register value instead of adding external feedback resistors, as shown in Equation 2:

$$VLED = 7\ V + \frac{10\ V \times DATA\ (decimal)}{32} \quad (2)$$

where DATA = decimal value defined in the EEPROM register (see Table 3).

Next, set the initial target output voltage, as shown in Table 3. In this case, the selected code is 21 (decimal) or 15h.

Table 3. TLC5970 Target Output Voltage Setting

DATA (hex)	Target Voltage (V)	DATA (hex)	Target Voltage (V)
00 (Default)	7.0	10	12.2
01	7.3	11	12.5
02	7.6	12	12.8
03	8.0	13	13.1
04	8.3	14	13.5
05	8.6	15	13.8
06	8.9	16	14.1
07	9.3	17	14.4
08	9.6	18	14.7
09	9.9	19	15.1
0A	10.2	1A	15.4
0B	10.5	1B	15.7
0C	10.9	1C	16.0
0D	11.2	1D	16.4
0E	11.5	1E	16.7
0F	11.8	1F	17.0

3.2 Setting the Duty Cycle, D

The next task for the dc-dc converter design is to define the duty ratio for buck converter operation. The maximum output voltage is calculated with VLED = D × VIN for the typical case. Here, the maximum and minimum duty ratio requirements are estimated as shown in the following equations:.

$$D_{Max} = \frac{VLED_{Max}}{VIN_{Min}}$$

$$D_{Min} = \frac{VLED_{Min}}{VIN_{Max}} \quad (3)$$

Figure 5 illustrates the case of V_{IN_Source} = 32 V, V_{IN_End} = 24 V, the total power-supply current = approximately 2 A, and each TLC5970 power consumption = 80 mA. The initial board VIN (V_{IN_Source}) is higher than the VIN of the last cascaded board (V_{IN_End}) as a result of the parasitic resistance of the power and ground cable wire. Here, VIN_{Min} should be considered as the lowest voltage of the total system, V_{IN_End}.

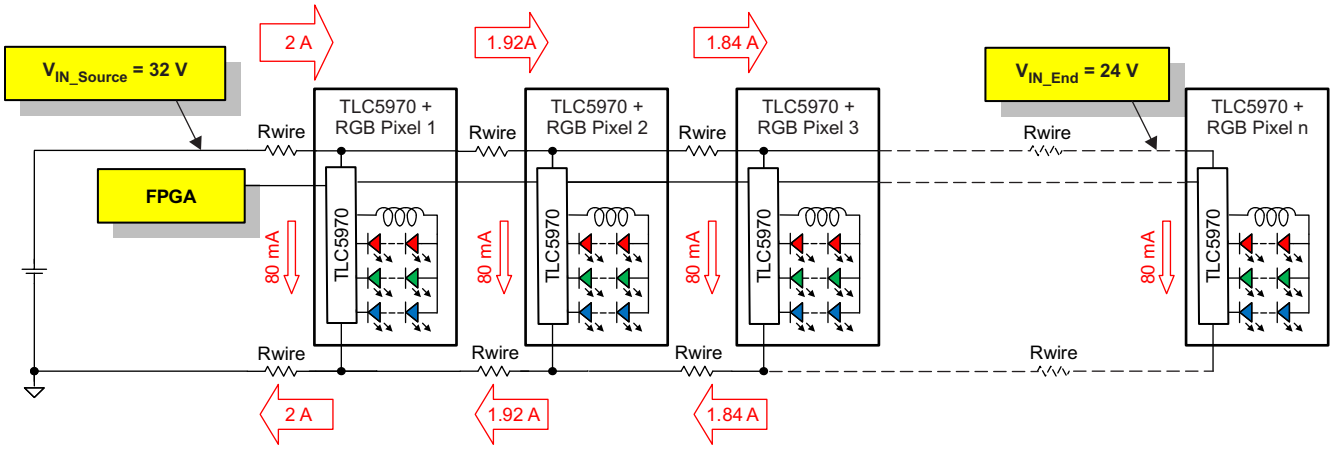


Figure 5. Typical LED Pixels Cascaded Connection

Table 4 lists the maximum duty cycle calculation for the case of VIN_{Max} = 32 V , VIN_{Min} = 24V, and $LEDV_f$ = 3.2 V .

Table 4. Maximum Duty Cycle Calculation

VIN_{Min}	LEDs in Series	VLED	Duty Cycle
24V	1	4.2V	17.5%
24V	2	7.4V	30.8%
24V	3	10.6V	44.2%
24V	4	13.8V	57.5%

Referencing the TLC5970 data sheet (SBVS140), the duty ratio setting code is listed in Table 5. In the case of the four series-connected LEDs, the selected DATA is 4d to cover 57.5% of the maximum duty cycle requirement. The TLC5970 duty cycle setting is limited to 86% in order to keep enough blanking time for any case. The blanking time is set to least 100 ns.

Table 5. TLC5970 DC-DC Duty-Cycle Setting Code

DATA	Duty Cycle (%)
0(Default)	18
1	30
2	42
3	55
4	67
5	80
6	86
7	86

Figure 6 shows the PFM operation of the TLC5970 integrated dc-dc converter.

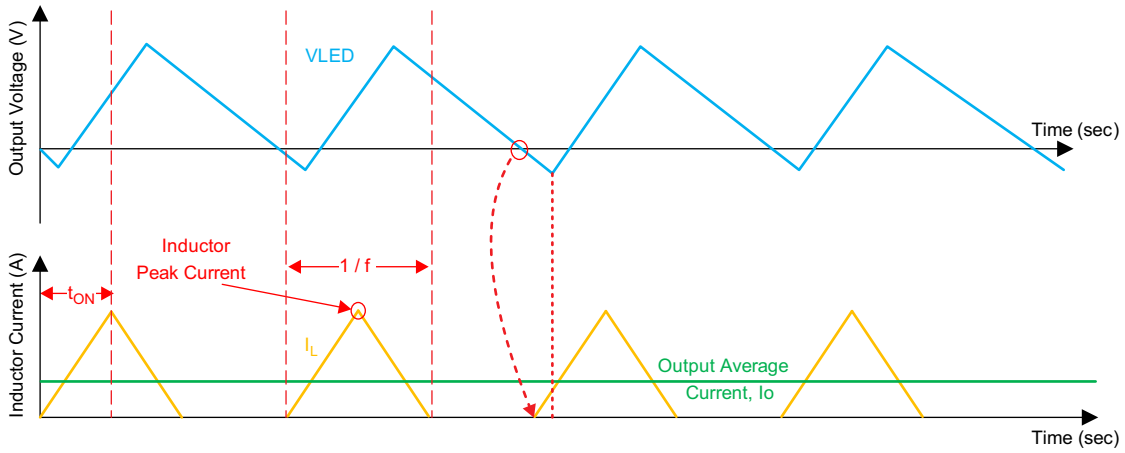


Figure 6. TLC5970 DC-DC Converter PFM Operation

The turn-on time is defined by the selected duty cycle (D) and the operating frequency of the dc-dc converter (f). It is 1.25 MHz typical and 1.5 MHz maximum.

$$t_{ON} = \frac{D}{f} \quad (4)$$

In steady state, the average inductor current should be equal to the load current. In the TLC5970, the dc-dc load is defined by the TLC5970 itself, LED currents, and serial interface consumption currents. The PFM operational switching frequency is defined by the required output average current, duty cycle D, and the inductor value (selected in the next section).

3.3 Calculate the Power Consumption of the DC-DC Converter

To select the appropriate inductor, estimate the power consumption of the dc-dc converter. The output current of the TLC5970 buck converter is divided into two portions:

1. Serial interface current (I_{FBn}) portion. The TLC5970 serial interface is powered from the FB pin; therefore, take I_{FBn} into consideration as part of the buck converter output current.
2. LED driver portion (I_{OUT0} + I_{OUT1} + I_{OUT2}).

Figure 7 shows the dc-dc output current flow.

$$I_{OUT(BUCK)} = I_{FBn} + \sum_{n=0}^{2} I_{OUTn} \quad (5)$$

According to the TLC5970 data sheet (SBVS140), I_{FB2} is used and the current-per-channel is set to 60 mA; the dc-dc converter output total current is calculated as $I_{OUT(BUCK)}$ = 60 mA + 60 mA × 3 = 240 mA. Refer to Section 4.2 for more details.

NOTE: The current consumption of the serial interface is not negligible because the TLC5970 integrates a powerful differential signal interface to be capable of transferring through more than 30 meters of cable. Also, the TLC5970 differential signal interface is designed to be powered up from the dc-dc output node (FB). Therefore, consider the serial interface current when calculating the dc-dc output current consumption.

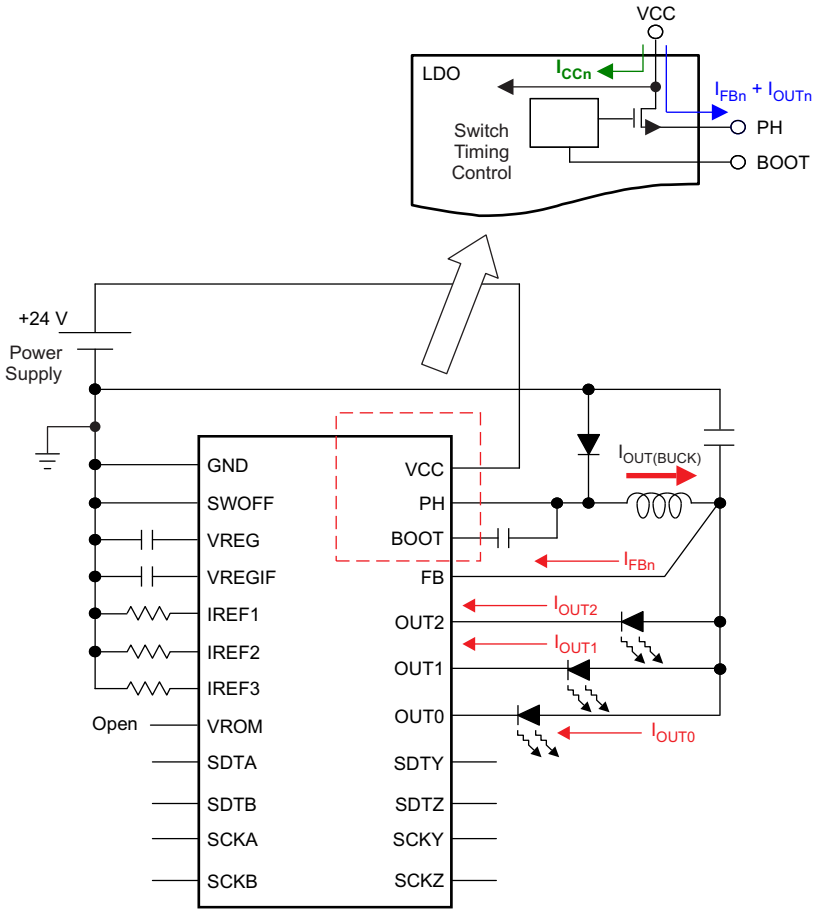


Figure 7. Power Consumption of the TLC5970

3.4 Selecting the Appropriate Inductor

Lastly, select the appropriate inductor. Because the TLC5970 integrates the high-side FET, the only required external components are the inductor, diode, and boot capacitance. The only guideline is that the peak inductor current must be less than 2 A.

The inductor current flows directly into the TLC5970 device; therefore, the current value must be lower in order to prevent the TLC5970 from permanent damage. This section describes how to select the appropriate inductor.

With the average output current given, the maximum peak inductor current (I_{LPK}) is calculated using Equation 7, and includes a 25% margin:

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{D}{D_{Min}}$$

Where η = buck converter efficiency; use 0.9 for reference. (6)

When using D = 67% , D_{Min} = 41% in the case of four series-connected LEDs with a 24-V input voltage, and the peak inductor current I_{LPK} is calculated as 1.08 A.

The minimum inductance value (L) is calculated as shown in Equation 7, according to the given input and output voltage conditions:

$$L > \frac{(VIN_{Max} - VLED_{Min}) \times D}{I_{LPK} \times f} \quad (7)$$

Applying dc-dc operating maximum frequency f as 1.5 MHz, L should be larger than 7 µH. See Appendix A for a more detailed description.

3.5 DC-DC Start Up Sequence

The TLC5970 dc-dc converter start up sequence is shown in Figure 8. After VCC is powered up, the VREG output reaches the undervoltage lockout (UVLO) release voltage (4.1 V, typical). All functions of the TLC5970 start, and the dc-dc converter starts in soft-start operation. This operation can take 800 ms maximum, and all LOD/OVP/SCP protection functions (see Table 13) are disabled during this mode. After soft-start operation, the TLC5970 goes to normal operating mode, and all protection functions are available.

NOTE: The VCC power-up sequence should be less than 800 ms. If VCC stays at a lower voltage (such as 6 V) even after 800 ms, the dc-dc converter short-circuit protection (SCP) may be induced, and as a result, dc-dc operation stops. SCP monitors whether the output node (FB) voltage continues to remain less than 4 V in normal operation.

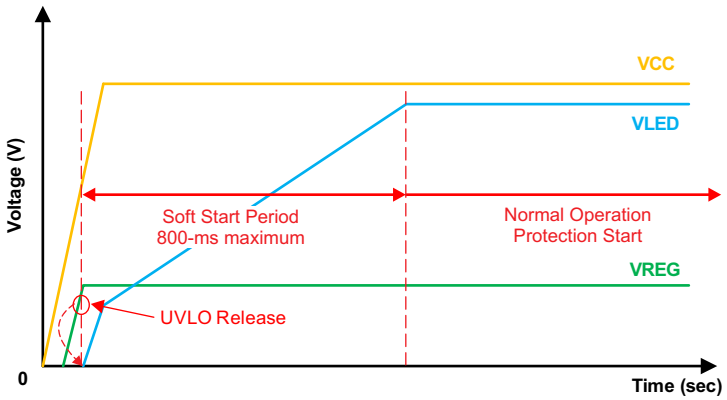


Figure 8. Start-up Sequence of the TLC5970 DC-DC Converter

4 Serial Interface Data Communication

The TLC5970 is equipped with a high-speed, reliable differential interface. This section describes how to configure the serial interface for an architectural lighting application to finalize the second step in the initialization flow chart in Figure 1.

4.1 Setting up the Data Communication Speed

The TLC5970 has three interface transfer modes; which one is selected depends on the communication line quality. The fastest mode is specified to 20-MHz data communication speed with the highest-quality environment for the data line. The slowest mode specifies 10-MHz communication, but the timing requirement is not as critical as for the fastest mode. The selected mode is set in an EEPROM register.

Make sure to note whether the difference of these communication modes only affects the output data timing of the TLC5970. Do not be concerned about the timing if just one part is used. Appropriate mode selection and the data-line quality (twisted pair connection, impedance matching wire) is essential if you require high-speed, long-wire communication. The different available modes help to fulfill the timing requirements dependent on the application.Table 6 shows a data communication mode comparison.

Table 6. TLC5970 Differential Interface Mode EEPROM: DSI

DATA	Mode	Cascade Count	Pixel Pitch	Speed
0	Mode 0 (Default)	50 (at 1 MHz)	≤ 30 m	≤ 10 MHz
1	Mode 1	Unlimited	≤ 50 m	≤ 15 MHz
2	Mode 2	Unlimited	≤ 50 m	≤ 20 MHz
3	Mode 2	Unlimited	≤ 50 m	≤ 20 MHz

Figure 9 illustrates the output timing difference based on differential signal interface (DSI) communication mode 0, 1, or 2; DSI mode 0 is the default. The clock and data information is passed though an internal buffer of the TLC5970. Data are acquired at the positive edge of the data clock, and the data line output is triggered by the negative edge of the data clock. Therefore, while the input data timing is simple, there is limited capability for a faster data transfer rate and wire length.

Table 7. Shift Clock Output Pulse-Width Error at DSI Mode 0

Parameter		Test Conditions	MIN	TYP	MAX	UNIT
t_{W_ERR}	Shift clock output pulse-width error	High-level pulse width of (SCKA to SCKB) – high-level pulse width of (SCKY to SCKZ) with DSI mode 0	–10		10	ns

The cascading number of mode 0 can be estimated from the below specifiaction item

$$n = \frac{\text{Duty}}{\text{Communication Frequency} \times \left| t_{W\_ERR} \right|} \quad (8)$$

With 1-MHz communication and 50% duty, the cascaded connection number at mode 0 is limited to 50 pieces in the worst case.

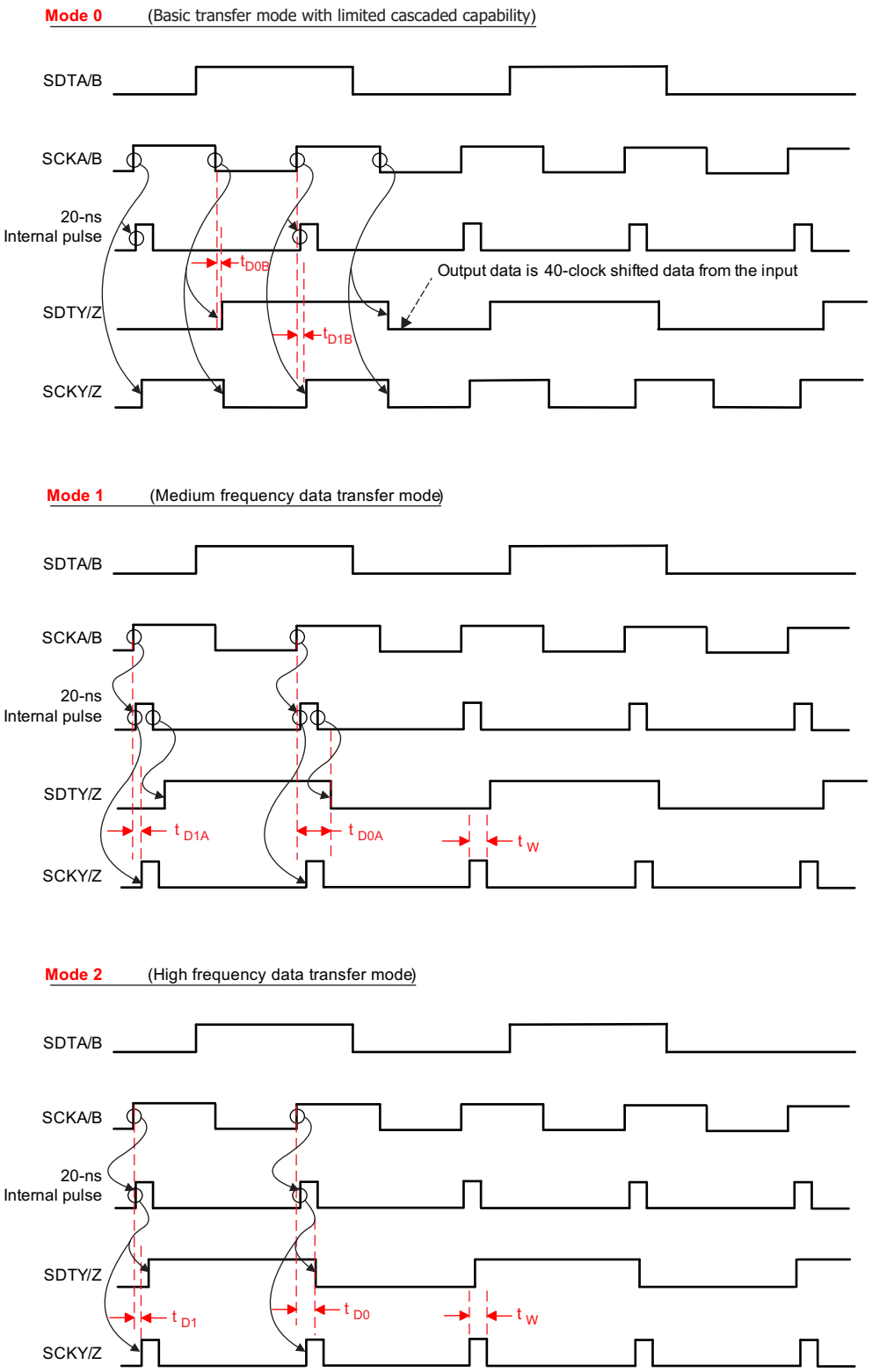


Figure 9. Timing Chart Comparison DSI for Modes 0, 1, and 2

DSI modes 1 and 2 are implemented in the TLC5970 for to allow for faster and unlimited cascading communication, even with a longer cable. The TLC5970 generates a clock with the minimum required pulse width and the data output is synchronized to this internal clock. Mode 2 requires the highest level of data line quality to ensure high-speed communication.

Figure 10 demonstrates actual experimental results with a cascaded connection. Mode 0 reaches a faster transfer speed than mode 2 when a shorter cable length is used (for example, 10 m). However, the transfer rate for mode 0 degrades faster than the other modes as the cable length increases.

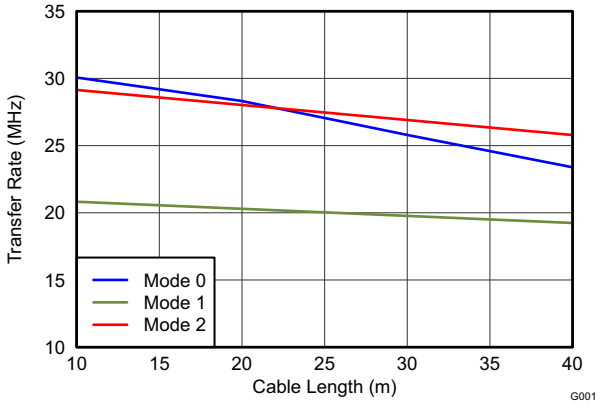


Figure 10. Data Transfer Rate vs Cable Length, T_A= +25°C

NOTE: The DSI register setting affects only the TLC5970 output timing. The data input timing of the TLC5970 connected to the controller is independent of the DSI mode selection.

If longer wire length and less than 15-MHz communication is required, mode 1 is preferred. In case you need longer wire and the fastest communication, select mode 2; however, mode 2 requires the highest level of data line quality. Mode 0 is useful in cases where few devices are cascaded, or where a slower rate communication frequency, such as 100 kHz, is required.

4.2 Setting Additional RL_{DIF} for > 2-m, 20-MHz Communication

The TLC5970 has internal 10-kΩ resistors in the differential interface, as shown in Figure 11.

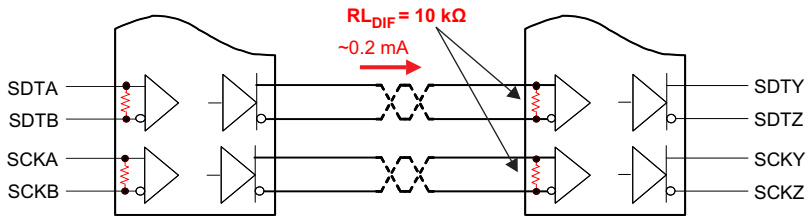


Figure 11. Differential Interface Termination RL_{DIF} = 10 kΩ (Default)

It is also possible to select the appropriate matching impedance between the differential inputs for higher data-line quality (that is, > 2-m wire length, and > 20-MHz high-speed communication). The TLC5970 is designed to drive 100-Ω common impedance, which is similar to the characteristic impedance of normal twisted-pair cable, as shown in Figure 12. For this design, make sure to consider the first-stage drivability of the TLC5970. Also, any additional TLC5970 current consumption from the dc-dc output (FB) must be taken into consideration because the TLC5970 serial interface is powered from FB. Table 8 shows the power consumption differences by RL_{DIF} setting.

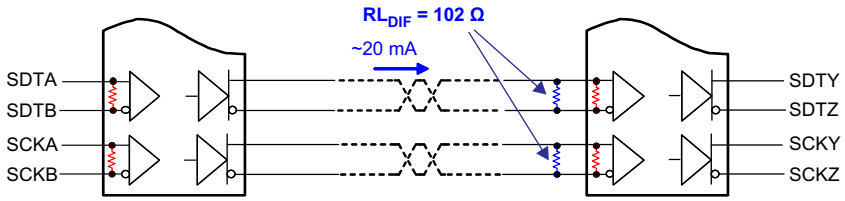


Figure 12. Differential Interface Terminate with RL_{DIF} = 102 Ω

Table 8. FB Output Current Depends on RL_{DIF} (1)

Symbol	Test Conditions	Min	Max	Unit
I_{FB2}	At FB pin. SDTA / SDTB = 10 MHz, SCKA / SCKB = 20 MHz with 0-V to 3-V swing, **CL_{DIF} = 15 pF**, PH/BOOT = open, FB = 7 V to 17 V, V(OUT_n) = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal oscillator mode, and auto repeat mode **SDTY-SDTY / SCKY-SCKZ = RL_{DIF} = 10 kΩ**	36	60	mA
I_{FB3}	At FB pin. SDTA / SDTB = 10 MHz, SCKA / SCKB = 20 MHz with 0-V to 3-V swing, **CL_{DIF} = 50 pF**, PH/BOOT = open, FB = 7 V to 17 V, V(OUT_n) = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal csillator mode, and auto repeat mode **SDTY-SDTY / SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω**	65	115	mA
I_{FB4}	At FB pin. SDTA / SDTB = 10 MHz, SCKA / SCKB = 20 MHz with 0-V to 3-V swing, **CL_{DIF} = 50 pF**, PH/BOOT = open, FB = 7 V to 17 V, V(OUT_n) = 1.0 V, GSn = FFFh, DCn = BC = 7Fh, R_{IREF} = 2 kΩ, internal csillator mode, and auto repeat mode **SDTY-SDTY / SCKY-SCKZ = RL_{DIF} = 2 × 51 Ω**	68	130	mA

(1) Test condition differences shown in **bold** text.

4.3 Internal Latch Generation Timing

The appropriate differential interface mode and the proper termination policy have already been selected. The other key design portion for the differential interface is the internal register data latch timing. The TLC5970 automatically generates the latch timing internally by recognizing the *blank* data input period and begins to light the LEDs by the latest data steam received. Therefore, make sure to consider the data stream input *blank* period to avoid any unnecessary data latch.

Figure 13 illustrates the data latch generation timing. This figure shows a 20-MHz data transfer rate (1-bit = 50 ns) and a 3-µs SCK blank input (longer than the typical 40-bit TLC5970 communication). If the rising edge of SCK is not detected, the TLC5970 generates the data latch signal internally, according to the EEPROM setting.

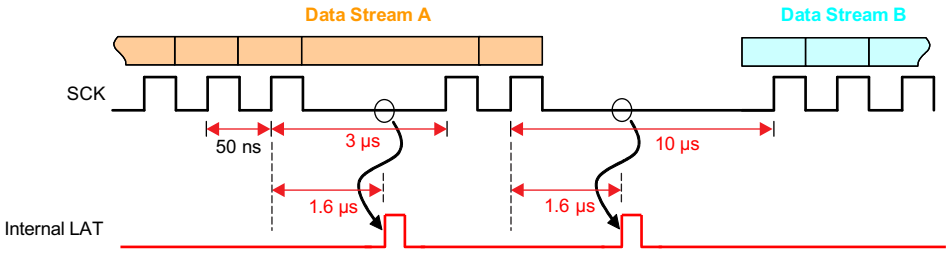


Figure 13. Internal Latch Generation Timing: EEPROM = 02 (1.6 µs Typical)

The TLC5970 data register consists of 40 bits. Therefore, the typical time required for one word is estimated using Equation 10:

$$t_{1WORD} = 40 \times \frac{1}{f_{CLK}} \tag{9}$$

When using a 20-MHz data transfer rate, the TLC5970 typical transfer time for one word (40 bits) equals to 2 µs. The recommended latch generation setting time is this one-word transfer time (to ensure that no communication is initiated from the host). Here, the EEPROM is set to 02h (typical generation time = 1.6 µs, min = 1.3 µs, and max = 2.3 µs) to Table 9 lists the EEPROM settings.

Table 9. TLC5970 Internal Latch Generation Typical Timing by EEPROM DATA Setting

DATA (hex)	Wait Time
0	0.4 µs
1	0.8 µs
2	1.6 µs
3	3.2 µs
4	6.4 µs
5	12.8 µs
6	25.6 µs
7	51.2 µs
8	0.1 ms
9	0.2 ms
A	0.4 ms
B	0.8 ms
C	1.6 ms
D	3.3 ms
E	6.6 ms
F (Default)	13.1 ms

4.4 Register Map

The TLC5970 has four writable registers, two read-only registers, and two writable EEPROM registers. Table 10 describes these registers. The TLC5970 serial interface is based on a 40-bit data steam, including a 4-bit address associated with every register and EEPROM. Figure 14 shows the total register and EEPROM map available in the TLC5970. The portions marked in red are user-configurable bits.

Table 10. TLC5970 Internal EEPROM and Registers Description

Name	Address	R/W	Description
GSData	0	W	Grayscale data latch register. This register stores the PWM grayscale data for each output.
Restart Operation	9	W	This register releases the error status (OVP/SCP) when it is recovered.
SID	10	R	Status information data (SID) read out register. This register stores the error status information.
EEPROM	11	R	EEPROM data readout register. This register accesses the EEPROM value to verify the EEPROM set data.
EEPROM1	12	W	First EEPROM write register. This register stores PH, FB, DSI and LAT delay information.
EEPROM2	13	W	Second EEPROM write register. This register stores dot correction information.
Dot Correction	14	W	Dot correction register data latch. This register overwrites the EEPROM2 value with the setting of the DC bit of the BC and FC register.
BC and FC	15	W	Global brightness control and function control data latch register. This register stores the 7-bit brightness control information and other function-related bits (overwrite dc data, external grayscale clock input mode, auto display repeat, auto data refresh, and display timing reset).

Name	R/W	B 39	B 38	B 37	B 36	B 35	B 34	B 33	B 32	B 31	B 30	B 29	B 28	B 27	B 26	B 25	B 24	B 23	B 22	B 21	B 20	B 19	B 18	B 17	B 16	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B 8	B 7	B 6	B 5	B 4	B 3	B 2	B 1	B 0
GSData	Write	Address				OUT2 Gray Scale Data												OUT1 Gray Scale Data												OUT0 Gray Scale Data											
		0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Restart Operation	Write	Address				N/A																																			
		1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SID	Read	Address				N/A																																	TSD	PTD	OVP	SCP	LOD
		1	0	1	0																																				
EEPROM	Read	Address				TI	LAT Delay			DSI	FB							PH			DCData OUT2									DCData OUT1							DCData OUT0					
		1	0	1	1	0																																			
EEPROM 1	Write	Address				Write Command								N/A																LAT Delay			DSI		FB				PH		
		1	1	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D3	D2	D1	D0	D1	D0	D4	D3	D2	D1	D0	D2	D1	D0
EEPROM 2	Write	Address				Write Command								N/A							DCData OUT2							DCData OUT1							DCData OUT0					
		1	1	0	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	D6	D5	D4	D3	D2	D1	D0	D6	D5	D4	D3	D2	D1	D0	D6	D5	D4	D3	D2	D1	D0
Dot Correction	Write	Address				N/A															DCData OUT2							DCData OUT1							DCData OUT0					
		1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D6	D5	D4	D3	D2	D1	D0	D6	D5	D4	D3	D2	D1	D0	D6	D5	D4	D3	D2	D1	D0
BC / FC	Write	Address				N/A																								DC	Tim	Ext	DSP	Ref	Brightness Control						
		1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0						D6	D5	D4	D3	D2	D1	D0

NOTE: Portions marked in red are user-configurable bits.

Figure 14. TLC5970 Register Map

5 LED Driver Setting

The final task required to initialize the device is to set the driver on the initial configuration flow (see Figure 1). The TLC5970 integrates fast switching with a 150-mA capable, three-channel LED driver. The OUT0, OUT1, and OUT2 output currents are defined by the resistors attached to IREF0, IREF1, and IREF2, respectively. The $IREF_n$ terminals output voltage is typically 1.2 V, and is divided by external resistor R_{IREF} to generate the reference current. The actual LED constant current is 125 times this reference current.

$$I_O = 125 \times \frac{1.2\ V}{R_{IREF}} \tag{10}$$

5.1 Dot Correction (DC)

The TLC5970 is capable of adjusting the constant output current linearly from 0% to 100% in 128 steps. This dot correction function adjusts the brightness difference between the outputs by adjusting the constant current value of each output. Each constant output current is calculated using Equation 11. The result can be stored to EEPROM as an initial value setting. This function can also be used to adjust the component-to-component LED brightness difference by adjusting the constant current value.

$$I_O = 125 \times \frac{1.2\ V}{R_{IREF}} \times \frac{DC\_DATA}{128}$$

Where DC_DATA = decimal value of the dot correction register of the respective output. (11)

5.2 Brightness Control (BC)

Brightness control is a function similar to dot correction; however, the difference is that brightness control adjusts the brightness of all outputs simultaneously (for example, when used for night-and-day brightness adjustment). Dot correction is typically coded in nonvolatile EEPROM in order to store the adjustment of the LED component intrinsic brightness difference. On the other hand, brightness control is used more dynamically; therefore, it is assigned to volatile register FC and BC in the TLC5970 (see Figure 14).

The TLC5970 is capable of adjusting the constant output current linearly with 128 steps from 0% to 100%. The output current is calculated using Equation 12:

$$I_O = 125 \times \frac{1.2\ V}{R_{IREF}} \times \frac{BC\_DATA}{128}$$

Where BC_DATA = decimal value of the brightness control register. (12)

If you use both dot correction and brightness control, the output current setting is multiplied by both of the register settings. For example, if R_{IREF} = 1 kΩ, DC_DATA = 112, and BC_DATA = 64, the output current is calculated as follows:

$$\begin{aligned} I_O &= 125 \times \frac{1.2\ V}{R_{IREF}} \times \frac{DC\_DATA}{128} \times \frac{BC\_DATA}{128} \\ &= 125 \times \frac{1.2\ V}{1k} \times \frac{112}{128} \times \frac{64}{128} \\ &= 65.6\ mA \end{aligned} \tag{13}$$

6 Reference Design Considerations

This section describes in detail how to generate effective designs in various subjects after the initial configuration.

6.1 2-Wire Serial Interface Configuration

If the pixel pitch is less than 2 meters, consider a 2-wire differential interface with common voltage level connections. This configuration reduces the communication interface to 2-wire (SDTA and SCKA) instead of the typical 4-wire (SDTA,SDTB and SCKA,SCKB) connection. The benefit is wire material reduction in connections, and reducing serial interface power consumption. Table 11 summarizes these interface topologies. The lower the frequency, the lower the power consumption value in a 2-wire configuration.

Table 11. 2-Wire and 4-Wire Differential Interface Comparison

Interface	2-Wire	4-Wire
Communication Length	**< 2 m**	**> 30 m**
RL_{DIF}	10 kΩ	100 Ω
I_{FB} at 20 MHz	40 mA	67 mA
I_{FB} at 10 MHz	33 mA	67 mA
I_{FB} at 5 MHz	29 mA	67 mA

Figure 15 shows the recommended schematic. SCKB and SDTB are connected as common level to SCKA and SDTA, respectively. Note that SCKB and SDTB have similar dc levels; almost half of the VREGIF output voltage. However, do *not* connect SCKB and SDTB directly together because it causes CLK-DATA interference during data communication.

NOTE: Do *not* tie SCKB and SDTB directly together in the application because it creates CLK-DATA interference during data communication and degrades the cascading connection capability.

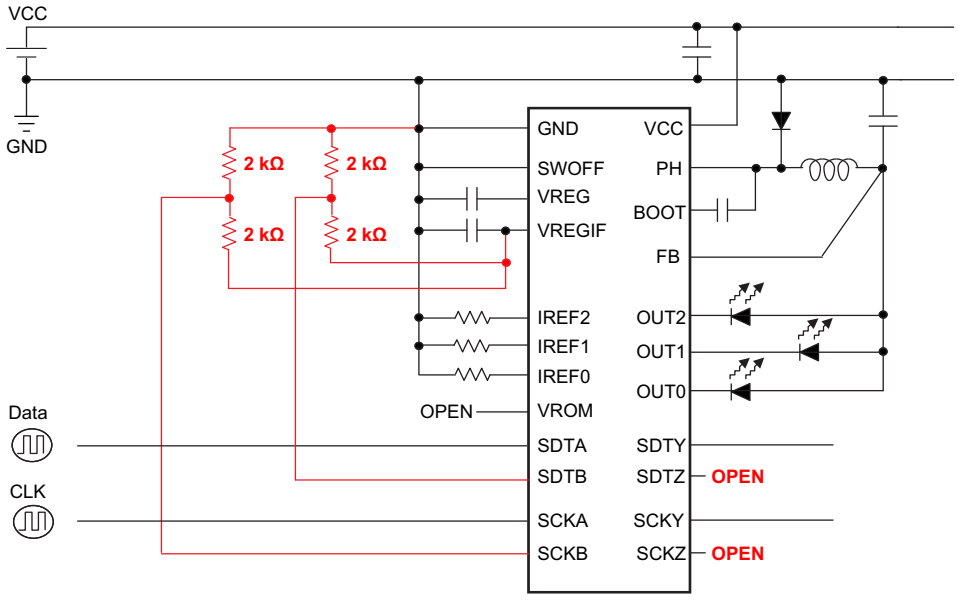


Figure 15. Common 2-Wire Connected Differential Interface

Figure 16 shows the serial interface power consumption, I_{FB}, dependent on the data communication frequency. A comparison is made among 4-wire and 2-wire both with RL_{DIF} = 10 kΩ, and 4-wire with RL_{DIF} = 102 Ω for longer wire communication. The 2-wire configuration power consumption depends on the data communication frequency. With a less than 10 MHz and less than 2 m requirement, the 2-wire configuration consumes only half of the current compared to the 4-wire configuration with RL_{DIF} = 102 Ω.

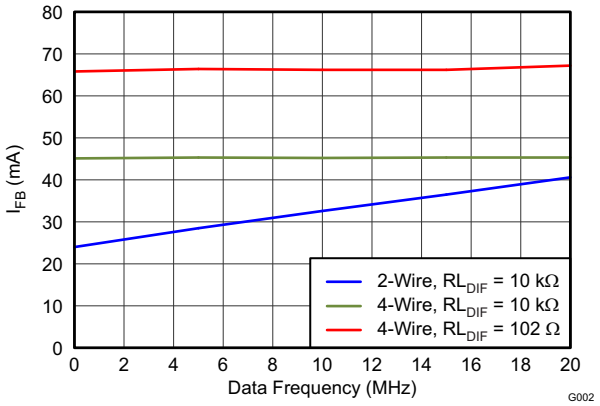


Figure 16. Serial Interface Power Consumption vs Data Communication Frequency

Figure 17 gives the temperature dependency for each configuration. The 4-wire configuration with R_{LDIF} = 102 Ω shows a slight dependency on the temperature.

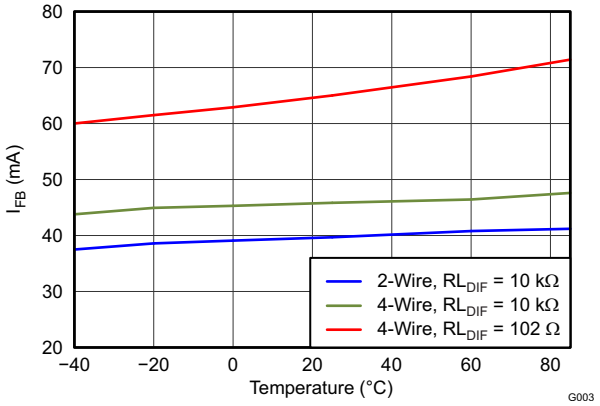


Figure 17. Serial Interface Power Consumption vs Temperature

Figure 18 is the power consumption data per the dc-dc output voltage. No dependency is observed in relation to the dc-dc output voltage.

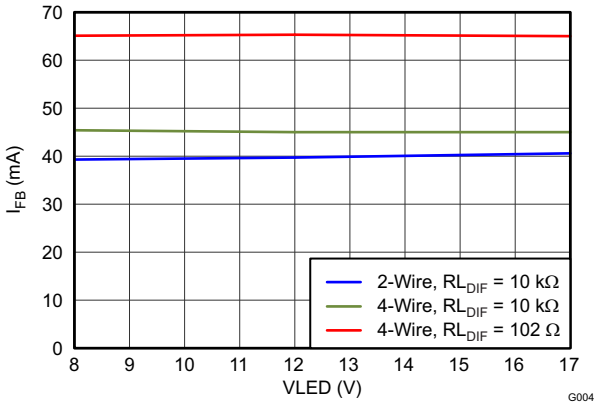


Figure 18. Serial Interface Power Consumption vs VLED

6.2 Appropriate Inductor to Keep Efficiency in Light Load Operation

The TLC5970 dc-dc converter typically operates with 90% efficiency at heavier load conditions, as shown in Table 12.

Table 12. Efficiency of Heavier Load Operation
D = 86%, LED Current = 150 mA/ch

VIN (V)	IVIN (mA)	VLED (V)	$I_{OUT(BUCK)}$ (mA)	Efficiency (%)
24	390	16.6	520	92.3

The TLC5970 PFM topology maintains good efficiency even at light load conditions, which often occur at lower LED currents (≈ 20 mA) and wider VIN input ranges (such as from 22 V to 36 V). In this section, measurement data and considerations in light-load operation are described.

In light-load operation, the peak current increases in proportion to the VIN input voltage. Therefore, the inductor saturation current capability is one of the key parameters that maintains keep good efficiency from lower VIN to higher VIN.

$$I_{LPK} = \frac{(VIN_{Max} - VLED_{Min}) \times t_{ON}}{L} \quad (14)$$

Figure 19 is an efficiency comparison of light-load mode versus VIN dependent on the inductor selection. Coil1 has a small form factor and lower saturation current. Coil2 has a slightly larger form factor and higher saturation current. At lower VIN, the efficiency gap is ≈ 3%; this gap is supposed to come from the dc loss difference of the selected inductors. the gap increases to ≈ 4.5% at higher VIN; this higher gap can be caused by the ac resistance difference.

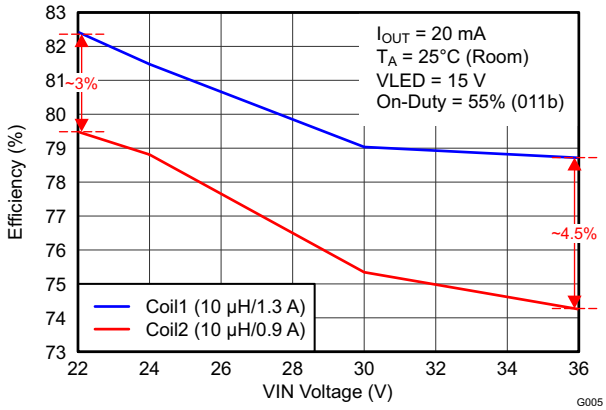


Figure 19. Efficiency Comparison at Light-Load Operation vs VIN,
20 mA/ch × 4 Series-Connected LED, with Inductors = 10 µH / 1.3 A and 10 µH / 0.9 A

Figure 20 shows the TLC5970 switching node waveform (PH) and inductor current waveform (I_L). With coil2, more frequent switching is required than with coil1 because of the lower efficiency. At VIN = 36 V, the peak current of coil2 is slightly higher than the saturation current capability rating (0.9 A).

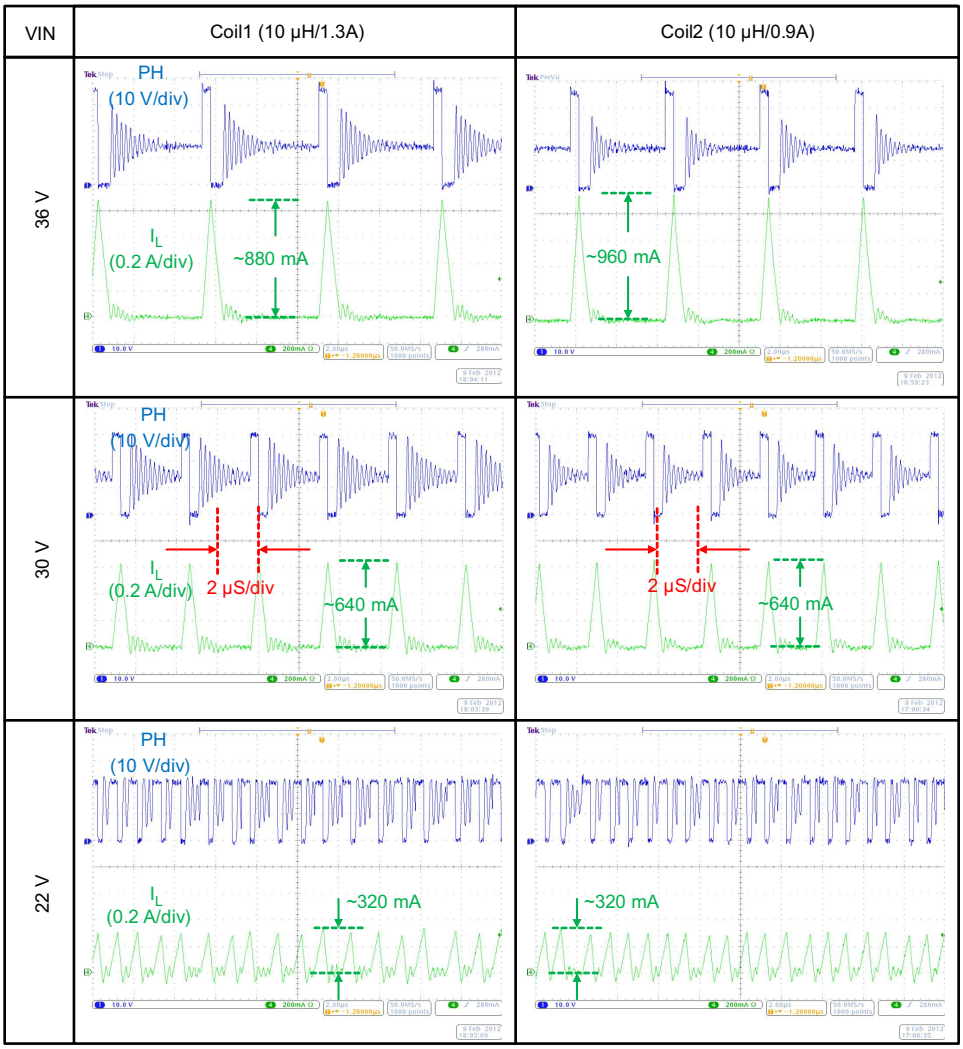


Figure 20. DC-DC Switching Waveform Comparison on Different Inductors

6.3 DC-DC Pins Connection When Unused

Disable the TLC5970 dc-dc converter operation by pulling up the SWOFF pin to the VREG level. This configuration is used to minimize the external dc-dc components for two or three pixels in one PCB . One TLC5970 then supplies the other pixels as well. Figure 21 shows the connection diagram.

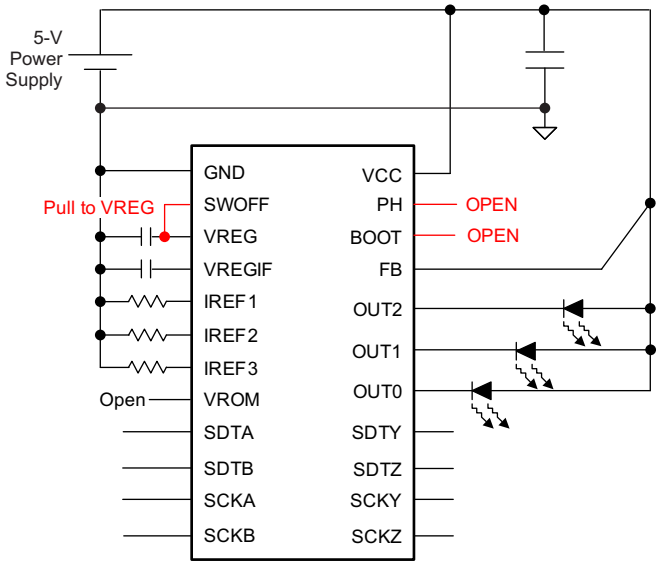


Figure 21. Disable the Buck Converter Operation: SWOFF = High

In this configuration, the dc-dc protection function is also disabled. The available protection is LED open detection and thermal-related protections. Refer to Section 6.4 for protection functions.

6.4 Protection Features

The TLC5970 provides full protection capability. Table 13 summarizes these protection features and the check points when protection activates. LED open detection (LOD) occurs when one LED connection is open. The TLC5970 detects the abnormal lower voltage even when the dc-dc output voltage reaches maximum voltage. If all three LED cathode nodes are detected to be lower, even when the dc-dc output voltage is at its maximum voltage, the TLC5970 detects an overvoltage of the dc-dc output and shuts off the LED strings. In all cases, the TLC5970 serial interface is still activated to maintain daisy-chain data communication.

In case TLC5970 dc-dc operation is forced off by SWOFF = H, the LOD operation has a lower detection voltage of the LED string cathode nodes.

Table 13. Protection Summary

Item	Symbol	Detection Conditions		Protection	Serial Interface
		Normal (SWOFF = L)	DC-DC OFF (SWOFF = H)		
LED open detection	LOD	$V(OUT_m) < 0.9$ V and $V(OUT_n) > 4$ V	$V(OUT_n) < 0.3$ V	Maintain the same dc-dc output	Active
Short-circuit protection	SCP	VLED < 4 V	N/A	DC-DC stops	Active
Overvoltage protection	OVP	VLED Max and $V(OUT_n) < 0.9$ V	N/A	LED driver stops	Active
Prethermal shutdown	PTD	Temp > +138°C		LED driver stops	Active
Thermal shutdown	TSD	Temp > +162°C		Device shutdown	Disabled

6.5 Adjusting Red LED Forward Voltage When Three or More LEDs Are Connected in Series

Adjusting the red LED string forward voltage when considering three or more LEDs connected in series is good design practice in general. Without this consideration, the lower forward voltage of the red LEDs could induce a false LED open detection.

Typically, the forward voltage of red LEDs is lower than that of blue and green LEDs. Figure 22 shows an example of the total LED voltage difference. Because the total LED forward voltage of the red LED string is 4.4 V lower than the green or blue strings, the TLC5970 red string V_{OUT} voltage is as high as 5.4 V. The TLC5970 detects such a voltage difference as an open LED error. Therefore, and typically, strings with three or more LEDs connected in series with different color LEDs require some compensation for the red LED forward voltage.

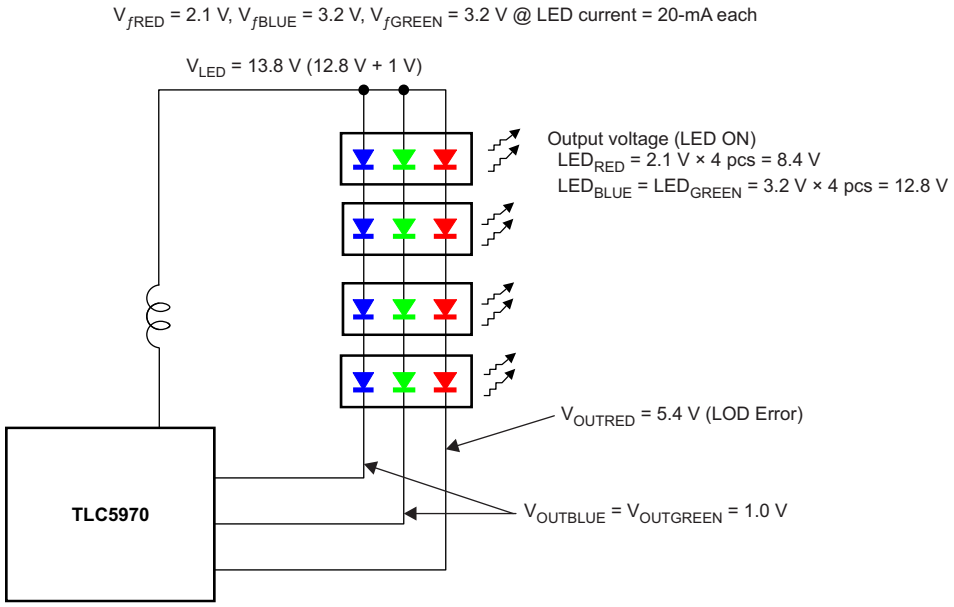


Figure 22. LED Total Voltage Difference Between Blue, Green and Red LED Strings

The most commonly used compensation circuit adds a resistor in series to the red LED string, as shown in Figure 23. In this circuit, the adjustment voltage is calculated with $V_R = I_{LED} \times R$. The circuit works well, as long as the LED current is fixed. If the LED current changes as a result of the dot correction or brightness control functions, the resistor-based compensated voltage also changes the LED current. Make sure to verify that the compensated voltage is appropriately applied for every current level.

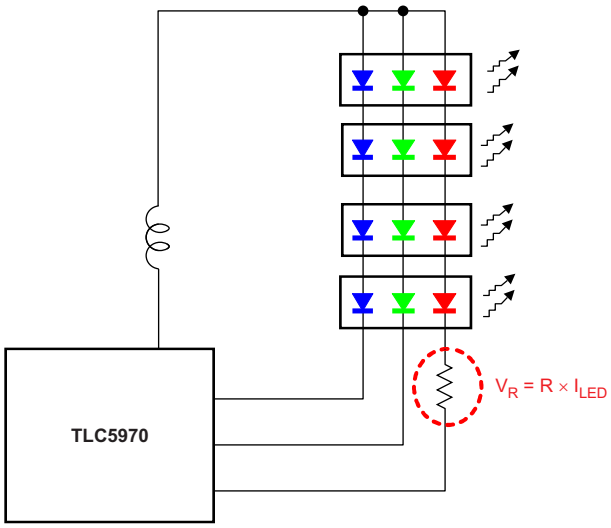


Figure 23. Inserting a Resistor to Adjust the V_f of Red LED

Another recommended compensation circuit is presented in Figure 24. This circuit uses a Zener diode for compensation. Because a Zener diode breakdown voltage is less dependent on the LED current, this circuit can be useful even when the LED current changes with the dot correction or brightness control functions.

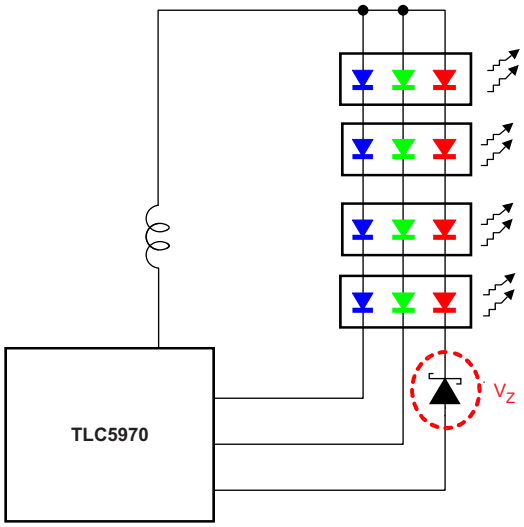


Figure 24. Inserting a Zener Diode to Adjust the V_f of Red LED

Table 14 is a summary of the compensation circuits.

Table 14. Red LED Forward Voltage Compensation Circuits

Configuration	Cost	Benefits
Resistor based (Figure 23)	Lower	Good for fixed LED current
Zener diode based (Figure 24)	Higher	Robust even when LED current changes

6.6 Power Supply and GND Wire Selection for Cascading

Figure 25 shows the power supply wire cascaded scheme. The maximum output current and return-back GND level current is gathered into the output/input terminal of the power supply. The last cascaded module operates between V_{IN_End} and the raised GND level. There are two guidelines for wire diameter selection:

- A large wire diameter is necessary at the initial power terminal to provide full power
- A small wire resistance is necessary to keep enough operation voltage on the last module

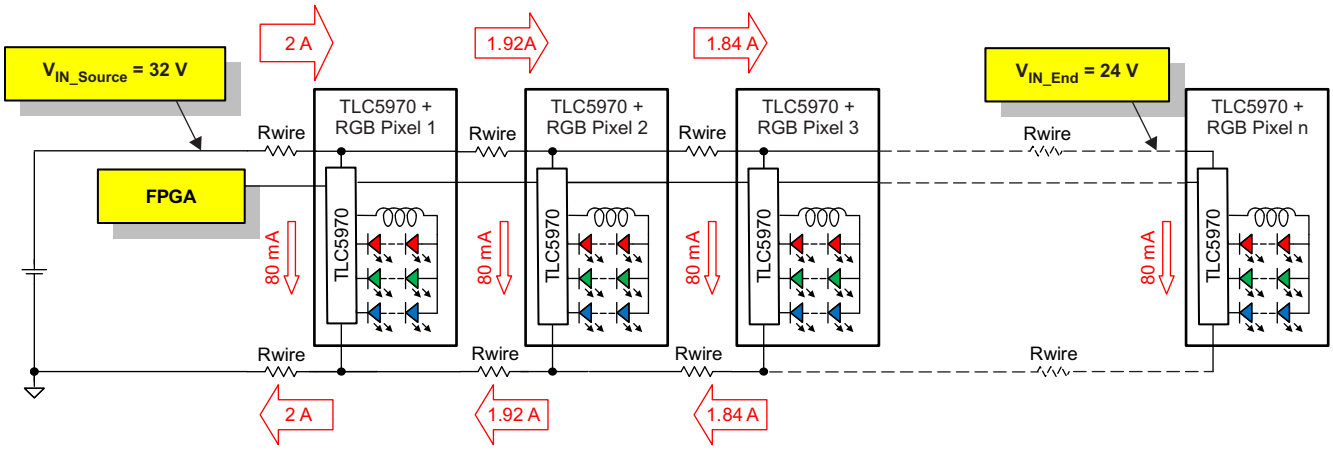


Figure 25. Typical LED Pixels Cascaded Connection

The VIN level and GND level of the *m*th LED pixels is calculated as shown in Equation 15:

$$V_{IN\_mth} = V_{IN\_Source} - \sum_{i=1}^{m} Rwire \times Icc \times (n - i + 1)$$

$$GND_{mth} = GND_{Source} + \sum_{i=1}^{m} Rwire \times Icc \times (n - i + 1) \quad (15)$$

Thus, the condition for correct operation of the last cascaded module #n is:

$$V_{IN\_nth} - GND_{nth} = V_{IN\_Source} - 2 \times \sum_{i=1}^{n} Rwire \times Icc \times (n - i + 1) > \frac{V_f \times LED\_Series\_Count + 1}{M}$$

where M = the voltage conversion ratio of the dc-dc converter.

$$M = \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}}$$

$$K = \frac{2 \times L \times f}{R} = \frac{2 \times L \times f \times I_{OUT(BUCK)}}{VLED} \quad (16)$$

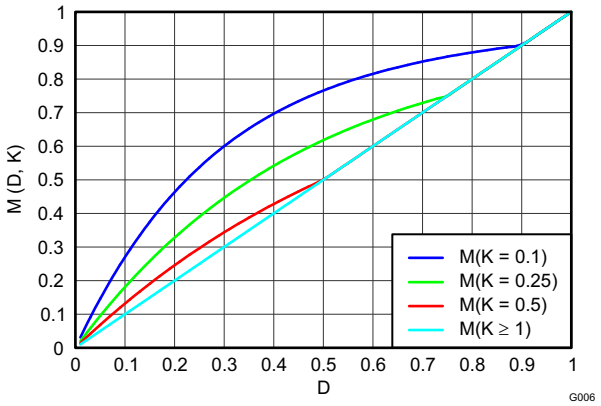


Figure 26. Buck Converter's Voltage Conversion Ratio M

To select appropriate power supply lines, refer to the Table 15 which shows the general AWG gauge versus wire diameter, wire resistance, and maximum current capability.

Table 15. Wire Gauge Table

AWG (Gauge)	Diameter (Inches)	Diameter (mm)	Ohms per 1000 ft	Ohms per km	Maximum Amps for Chassis Wiring	Maximum Amps for Power Transmission
19	0.036	0.91	8.05	26.41	14.0	1.80
20	0.032	0.81	10.15	33.29	11.0	1.50
21	0.029	0.72	12.80	41.98	9.0	1.20
22	0.025	0.65	16.14	52.94	7.0	0.92
23	0.023	0.57	20.36	66.78	4.7	0.73
24	0.020	0.51	25.67	84.20	3.5	0.58
25	0.018	0.45	32.37	106.17	2.7	0.46
26	0.016	0.40	40.81	133.86	2.2	0.36
27	0.014	0.36	51.47	168.82	1.7	0.29
28	0.013	0.32	64.90	212.87	1.4	0.23
29	0.011	0.29	81.83	268.40	1.2	0.18
30	0.010	0.25	103.20	338.50	0.9	0.14
31	0.009	0.23	130.10	426.73	0.7	0.11

6.7 Retrieving Status Information Data(SID)

The TLC5970 stores status information in the Status Information Data (SID) register. Figure 27 shows an application design for retrieving the SID safely with longer communication wire lengths. The SID can be retrieved from the end module through the daisy-chain connection. The key point is to maintain the logic GND level difference between the last TLC5970 device and the controller device.

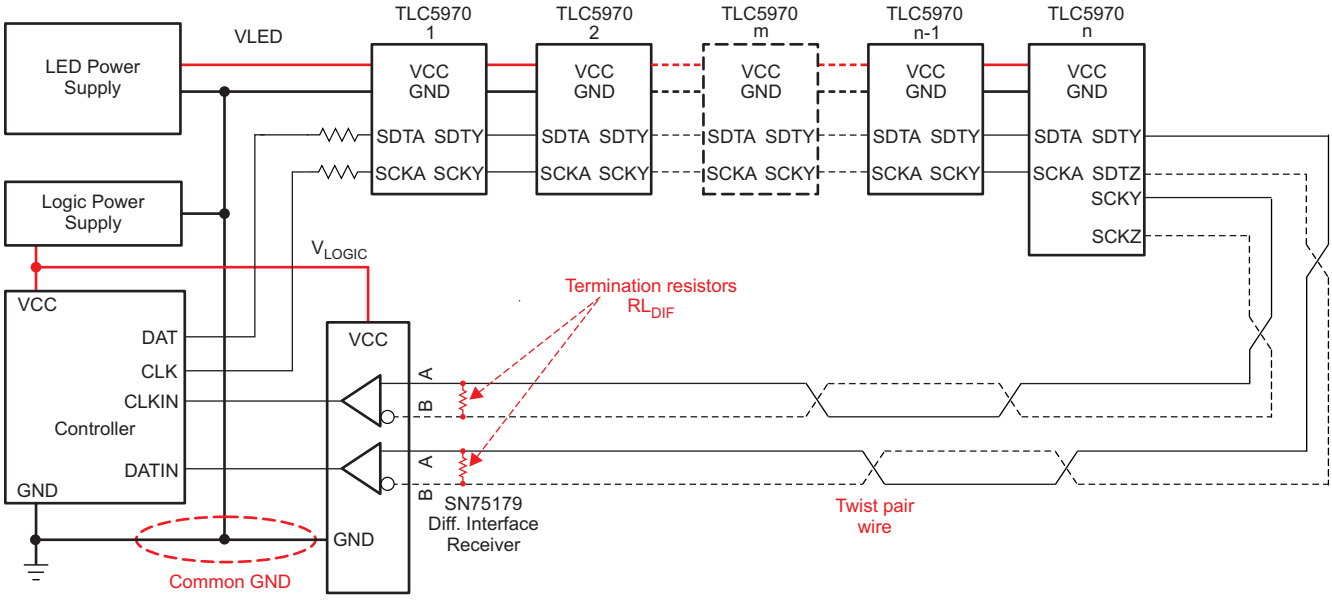


Figure 27. Reading SID Protection Information

As mentioned in Section 6.6, a GND-level shift occurs at the last cascaded TLC5970 from the first TLC5970 as a result of the parasitic resistance of the cable and device power consumption. Therefore, the direct connection of the last TLC5970 differential outputs to the controller device may cause permanent damage to the controller device by exceeding the absolute maximum rating of the controller device, typically defined as 3.3 V for FPGAs or ARM-based processors.

CAUTION

The direct connection of the last TLC5970 differential outputs to the controller device may cause permanent damage to the controller device by exceeding the absolute maximum rating of the controller device, typically defined as 3.3 V for FPGAs or ARM-based processors.

It is recommended to insert buffers for the differential interface to adjust for the GND level difference. By inserting a dedicated differential receiver, the total system is more reliable and robust.

6.8 Layout Guidelines

Figure 28 shows the layout key points. To maximize the performance of the device, layout is always critical; especially for dc-dc converters. A dc-dc converter often switches at high power and at certain high frequencies; therefore, it can be a big noise source to the entire system. The basic noise-reduction strategy is to minimize the switching loops to lower the parasitic impedance and inductance, thus preventing unnecessary noise.

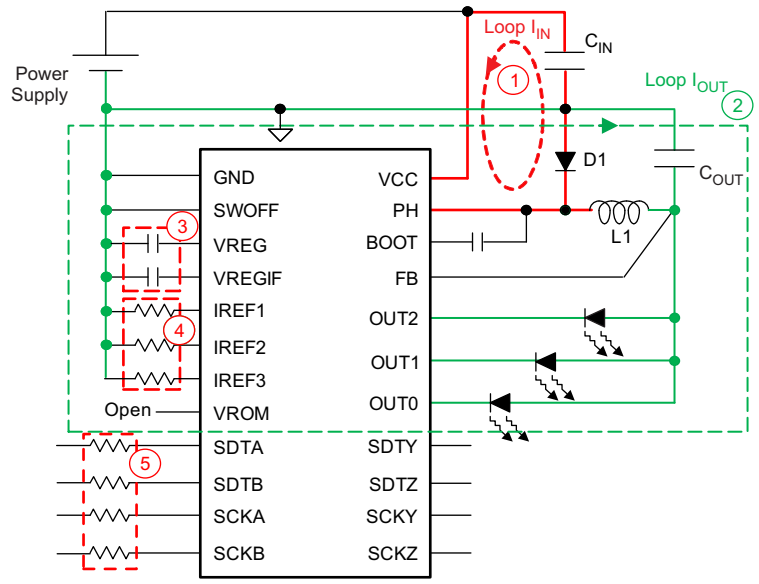


Figure 28. TLC5970 Layout Key Points

The different numbered sections of Figure 28 are:

1. **Loop I_{IN}**
   This portion is the fastest switching loop and needs the most care to prevent noise. The basic strategy is to minimize this loop to minimize the parasitic impedance and inductance. The parasitic inductance ESL of this loop causes voltage level noise ESL × di/dt.
   - Avoid any via hole connections. If you need a via, then place multiple vias in parallel.
   - Place C_{IN} and D1 close to the device.
   - Use wide and short layout power lines.
2. **Loop I_{OUT}**
   This is the output current loop. It has less switching than the input loop, but you must take care of parasitic inductance on C_{OUT}. It also causes spike noise with fast LED current transition.
   - Use a wide and short layout line to L.
   - Avoid via connection from C_{OUT} to GND. If you need a via, consider multiple vias in parallel.
3. **Regulator Output Capacitors**
   These capacitors are used for the TLC5970 integrated low-dropout regulator (LDO).
   - These capacitors must be placed close to the device.
4. **Reference Resistors**
   These resistors are used to set each of the output currents. The GND connection must be stable. If it is unstable, there is an output current oscillation risk.
   - Use the proper width layout GND power line.
5. **Noise Filter Resistors**
   The logic input resistors are often used for noise filtering. Because the TLC5970 integrates high-speeds and long-wire communication, this filtering is recommended.
   - Starting with a lower impedance, such as 100 Ω, is a good idea. Use up to 1-kΩ resistors.

7 Reference Design

This section presents a reference design and experimental results. Table 16 lists the target specifications for a portable demo system with 20-MHz high-speed communication using six series-connected LED strings. The LED pixel pitch is 15 cm, and 30 cascaded TLC5970 modules are evaluated.

Table 16. Reference Design Target Specifications

LED series connected count	6
LED strings forward voltage	20 V
LED maximum current	60 mA
LED typical current	20 mA
LED pixel pitch	15 cm
TLC5970 cascaded count	30
Data transfer speed	20 MHz
Communication interface	2-Wire
V_{IN_Source} (pixel number = 1)	30 V
V_{IN_End} (pixel number = 30)	29 V
Power-supply current	2 A
Inductor	5 µH/1.8 A (10 µH / 0.9 A × 2)
RL_{DIF}	10 kΩ (internal only)

In this system, the TLC5970 initial EEPROM configuration parameter selected is shown in Figure 29. Note that the TLC5970 VLED output range is defined from 5 V to 17 V (see Table 3); therefore, in this reference design, the maximum output voltage setting is boosted up by using a Zener diode in series inserted into the feedback node. For the 20-MHz high-speed interface, DSI mode 2 is selected, and the internal latch generation timing is set to a 1.6-µs typical, 2.3-µs maximum value. The maximum duty cycle is set to 42%.

EEPROM	Operation	Field	Bits
EEPROM 1	Write	Address	1 1 0 0
		Write Command	1 0 1 0 0 1 0 1
		N/A	0 0 0 0 0 0 0 0 0 0 0 0 0 0
		LAT Delay	0 0 1 0
		DSI	1 0
		FB	1 1 1 1 1
		PH	0 1 0
EEPROM 2	Write	Address	1 1 0 1
		Write Command	0 1 0 1 1 0 1 0
		N/A	0 0 0 0 0 0 0
		DCData OUT2	1 1 1 1 1 1 1
		DCData OUT1	1 1 1 1 1 1 1
		DCData OUT0	1 1 1 1 1 1 1

Figure 29. Reference Design EEPROM Initial Configuration

Figure 30 is a picture of a lab experiment with 30 cascaded LEDs in series. The 20-MHz data communication is initiated from the FPGA controller. This FPGA has a USB interface to upload the FPGA program from a personal computer (PC). A 30-V power supply generates the bias power to the LED modules.

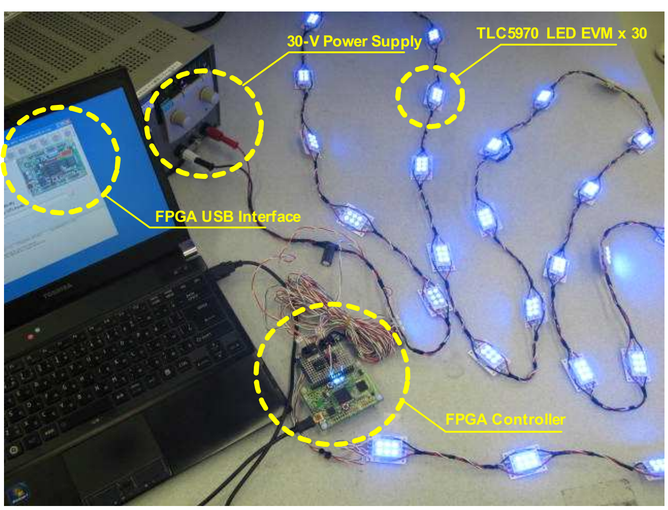
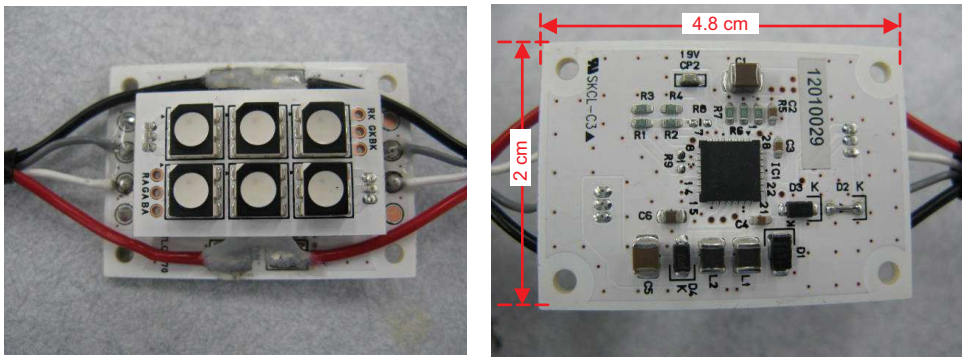


Figure 30. TLC5970 Reference Design Evaluation Environment

Figure 31 shows the top and bottom views of the TLC5970 with six series-connected RGB LEDs on one module. Six RGB LEDs are mounted on a daughter board on the TLC5970 module. The device temperature is measured at less than +70° (shown in Figure 32).



(a) Top View (b) Bottom View

Figure 31. TLC5970 Reference Design Module Picture

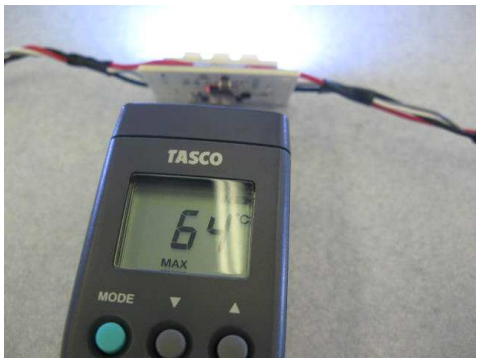


Figure 32. TLC5970 Reference Design Module Temperature Measurement: I_{LED} = 20 mA Each

7.1 Evaluation Results

Here are the power-supply measurement results. At the power supply, V_{IN_Source} is 30.05 V; at the end of the module row, the VLED drops by 320 mV. The power supply current is 1.9 A, while each RGB LED current is 20 mA typical.

Table 17. Reference Design Evaluation for Power Supply

Parameter	Value
V_{IN_Source}	30.05 V
V_{IN_End}	29.73 V
Power supply current	1.9 A

Table 18 shows the measurement results of the R, G, and B forward voltage variance of six series-connected LEDs. Without compensating the forward voltage difference between red, green, and blue, the TLC5970 recognizes this as an error status; see *Section 6.5* for more details. In this case, a 5-V Zener diode effectively works, as shown in Figure 24.

Table 18. Six Series-Connected LEDs Forward Voltage Variance

LED Color	Mean	Standard Deviation
Red	11.5 V	74 mV
Green	18.1 V	243 mV
Blue	17.6 V	94 mV

Next are the data communication line evaluation results of 20 MHz, 30 series-cascaded, 2-wire communication without external RL_{DIF}s (Figure 33). The output waveforms of the module #1 TLC5970 and module #29 TLC5970 are almost identical, as shown in Figure 34. Therefore, in theory, you can connect as many TLC5970s as required.

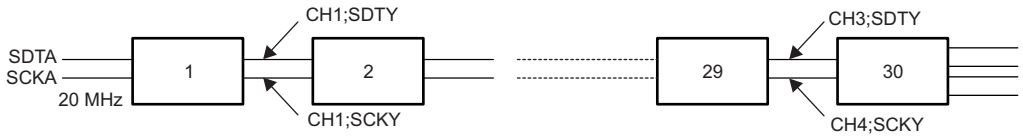


Figure 33. 2-Wire Interface with 20 MHz, 30 Cascading Test

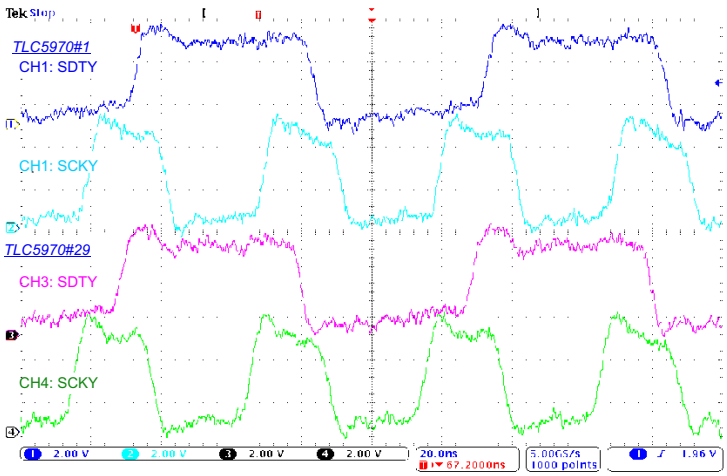


Figure 34. Waveform Comparison #1 Output and #29 Output

7.2 Six Series-Connected LEDs in a 60-mA Reference Design

Figure 35 shows the reference design schematic for the module with six series-connected, 60-mA (maximum) LEDs. This reference design can switch between 2-wire and 4-wire communication. Although the default TLC5970 dc-dc converter maximum output voltage is limited to 17 V, this reference design boosts the FB voltage by adding a Zener diode (D4) to the feedback connection line. Table 19 details the 2-wire and 4-wire data communication settings. You can add 2-kΩ resistors to enable 4-wire data communication.

Table 19. 2-Wire and 4-Wire Communication Settings

Mode	SCKB	SDTB	R1	R2	R3	R4	R8	R9
2-Wire	Open	Open	2 kΩ	2 kΩ	2 kΩ	2 kΩ	Open	Open
4-Wire	$\overline{\text{SCKA}}$	$\overline{\text{SDTA}}$	Open	Open	Open	Open	Reserve	Reserve

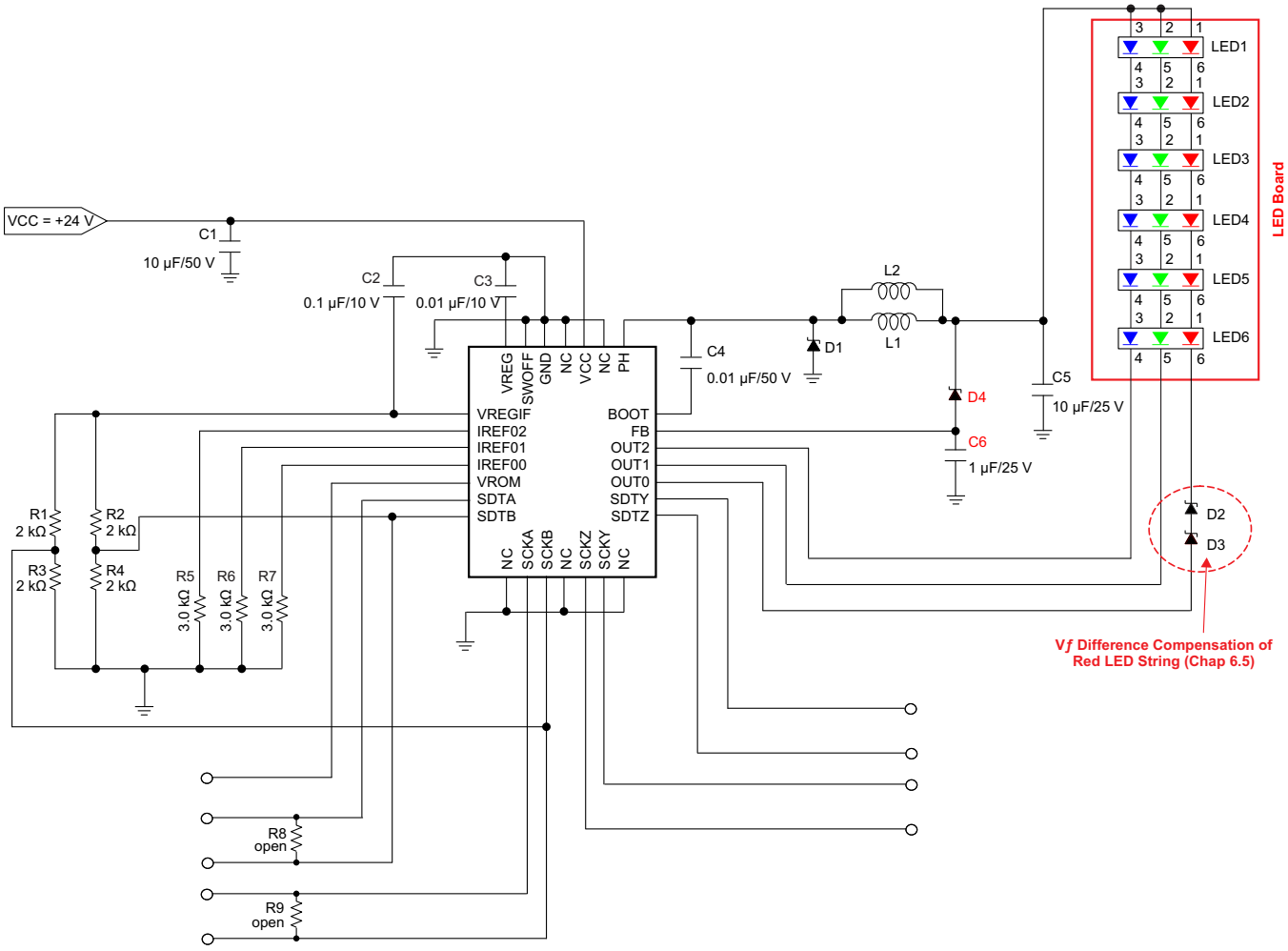


Figure 35. TLC5970 Reference Design: Six Series-Connected LEDs

Table 20 gives the list of required materials.

Table 20. List of Materials

Symbol	Parts No	Spec	Manufacturer	Description	Size
C1	GRM32ER71H106KA12L	10 µF / 50 V	Murata	Chip capacitor	3225(1210)
C2	GRM155R71A104KA01D	0.1 µF / 10 V	Murata	Chip capacitor	1005(0402)
C3	GRM033R71A103KA01D	0.01 µF / 10 V	Murata	Chip capacitor	0603(0201)
C4	C1608X7R1H103K	0.01 µF / 50 V	TDK	Chip capacitor	1608(0603)
C5	GRM32DR71E106KA12L	10 µF / 25 V	Murata	Chip capacitor	3225(1210)
C6	GRM219R71E105KA88D	1 µF / 25 V	Murata	Chip capacitor	2012(0805)
R1, R2, R3, R4	RGC1/16SC202DTH	2.0 kΩ, 0.0625 W, 0.5%	Kamaya	Chip resistor	1005(0402)
R5, R6, R7	CPF0402B3K0E1	3 kΩ, 0.0625 W, 0.1%	TE Connectivity	Chip resistor	1005(0402)
R8, R9	RGC1/16C101DTP	100 Ω, 0.1 W, 0.5%	Kamaya	Chip resistor	1608(0603)
L1	CBC3225T100MR	10 µH / 0.9 A	Taiyo Yuden	INDUCTOR 10 µH 20% 1210 SMD1210 (3225 Metric)	3225(1210)
L2	CBC3225T100MR	↑	↑	↑	↑
D1	SS2P4-E3/84A	2 A / 40 V	Vishay	Schottky diode	SMP 2.2mm x 4.0mm x 1.15mm
D2,3	MMSZ5230BT1G	4.7 V / 0.5 W	ON Semiconductor	Zener diode	SOD-123, 1.6mm x 2.69mm x 1.12mm
D4	MMSZ5230BT1G	4.7 V / 0.5 W	ON Semiconductor	Zener diode	SOD-123, 1.6mm x 2.69mm x 1.12mm
LED1, LED2, LED3, LED4	OVSTRGBB1CR8	Continuous R/G/B = 50 mA, Peak R/G/B = 200/100/100 mA	Optek Technology	Full Color LED(RGB) LED RGB ROUND DIFFUSED 6PLCC	6mm x 5mm x 2.5mm
Header pin	M52-040023V1045	1.27-mm pitch	HARWIN		1.27mm pitch

Appendix A TLC5970 DC-DC Inductance Calculation

In this appendix, a detailed description of the dc-dc inductance calculation is presented; specifically, the inductance values calculation, numerical examples, and an understanding of the dc-dc operational modes. The flowchart for the TLC5970 dc-dc converter settings is shown in Figure 36.

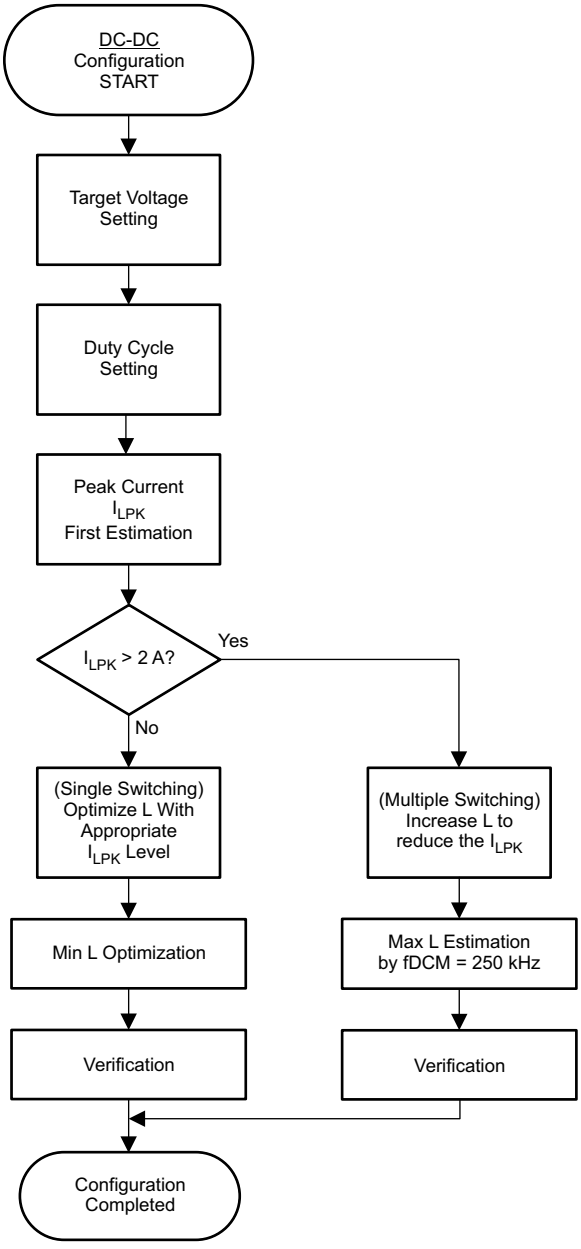


Figure 36. TLC5970 DC-DC Configuration Flowchart

A.1 Duty Cycle Setting

First, calculate the maximum and minimum duty cycle requirement from the given VIN and VLED requirement:

$$D_{Max} = \frac{VLED_{Max}}{VIN_{Min}}$$

$$D_{Min} = \frac{VLED_{Min}}{VIN_{Max}} \quad (17)$$

Set the duty cycle D to be > D_{Max} in the TLC5970 EEPROM code.

Table 21. TLC5970 DC-DC Duty Cycle Setting Code

DATA	Duty Cycle (%)
0(Default)	18
1	30
2	42
3	55
4	67
5	80
6	86
7	86

A.2 Peak Current Calculation

Now you are ready to estimate the maximum peak current of the inductor including 25% margin, as shown in Equation 18:

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{D}{D_{Min}}$$

where

- η = buck converter efficiency. Use 0.9 for reference.
- $I_{OUT(BUCK)}$ = buck converter output current (LED current plus serial interface current). (18)

The calculated inductor peak current value depends heavily on the LED current value requirement. If the LED current is set to a low value (for example, 20 mA/channel), the maximum peak current can be a lower value (for example, less than 0.5 A). For larger currents (for example, 150 mA/channel), the maximum peak current can potentially exceed 2 A. Therefore, there are two recommended policies for dc-dc design with effective inductor usage according to the required current level:

1. For a lower LED current: Use a smaller inductance value to operate the inductor more effectively.
2. For a Higher LED current: Use a larger inductance value to suppress the higher peak current.

A.3 Peak Current Calculation at < 2 A

In this case, the LED current is a lower current setting such as 20 mA. Use as small an inductor as possible within the range of the available peak current of the inductor.

A.3.1 Minimum Inductance Value Estimation

Calculate the minimum inductance value based on the saturation current I_{LPK} setting, as shown in Equation 19:

$$L > \frac{\left(VIN_{Max} - VLED_{Min}\right) \times t_{ON}}{I_{LPK}} = \frac{\left(VIN_{Max} - VLED_{Min}\right) \times D}{I_{LPK} \times f_{Max}}$$

Where f_{Max} = buck converter operating frequency; use 1.5 MHz (maximum). (19)

A.3.2 Peak Current Verification

Confirm that the peak current value is in a stable operating condition with the already estimated inductance value under worst-case conditions using Equation 20:

$$I_{LPK} = \frac{\left(VIN_{Max} - VLED_{Min}\right) \times D}{L \times f}$$

Where f = buck converter operating frequency; use 1.25 MHz (typical). (20)

A.4 Peak Current Calculation at > 2 A

When the peak current calculation results in a value greater than 2 A (for example, in higher load conditions), the operating frequency must be reduced to lower the peak current.

The typical method to reduce the peak current is to use a larger inductor value, which lowers the slope tendency of the inductor current; thus, the peak current value is reduced by as much as 30%.

A.4.1 Maximum Inductance Value Estimation

Calculate the maximum inductance value as shown in Equation 21:

$$L < \frac{D \times (1 - D) \times VIN_{Min}}{2 \times f_{DCM} \times I_{OUT(BUCK)}}$$

$$f_{DCM} = \frac{f}{n}$$

Where f_{DCM} = DCM operating frequency. The buck converter operating frequency divided by n (integer ≥ 1); in this case, use 250 kHz. (21)

A.4.2 Peak Current Verification

The worst-case peak current is estimated in Equation 22:

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{n + 1}{n} \quad (22)$$

Appendix B Inductance Selection versus Operating Modes

Equation 23 shows the calculation for the buck converter critical output current(I_{ocrit}) when the selected inductance value leads to operation in the boundary condition between DCM and CCM:

$$I_{ocrit} = \frac{D \times (1-D) \times VIN_{Min}}{2 \times f_{DCM} \times L} \quad (23)$$

The maximum inductance value (L) for a given output current can be calculated as shown in Equation 24.

$$L < \frac{D \times (1-D) \times VIN_{Min}}{2 \times f_{DCM} \times I_{OUT(BUCK)}} \quad (24)$$

Where f_{DCM} represents the DCM operating frequency. This is calculated as dc-dc operating frequency f divided by n (integer ≥ 1), as shown in Equation 25.

$$f_{DCM} = \frac{f}{n} \quad (25)$$

Figure 37 shows the dc-dc operating mode transitions defined by the required power consumption, $I_{OUT(BUCK)}$, and inductance value L. The red dashed area is denoted as (a), the*Single Pulse Switching DCM* area. This represents lower frequency typical DCM operation for lower LED currents, such as I_{LED} = 20 mA/ch. The green dashed area is denoted as (b), the *Multiple Pulses Switching DCM* area. This area is also analyzed as a DCM region with lower operating frequency, and convenient for high currents, such as I_{LED} = 150 mA/ch. Area (c) is the CCM operating mode. The TLC5970 dc-dc converter does not typically use this area.

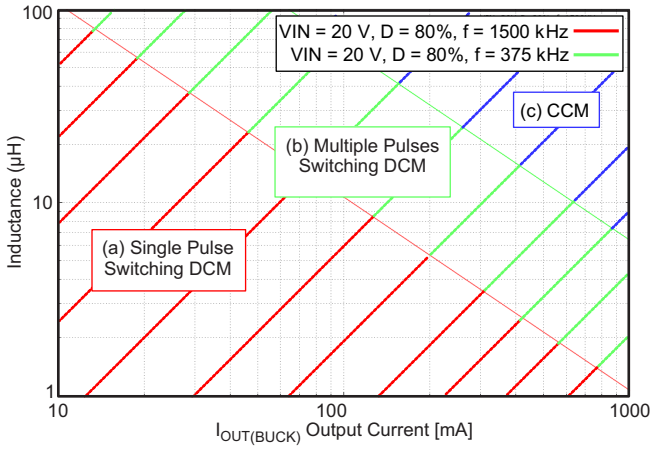
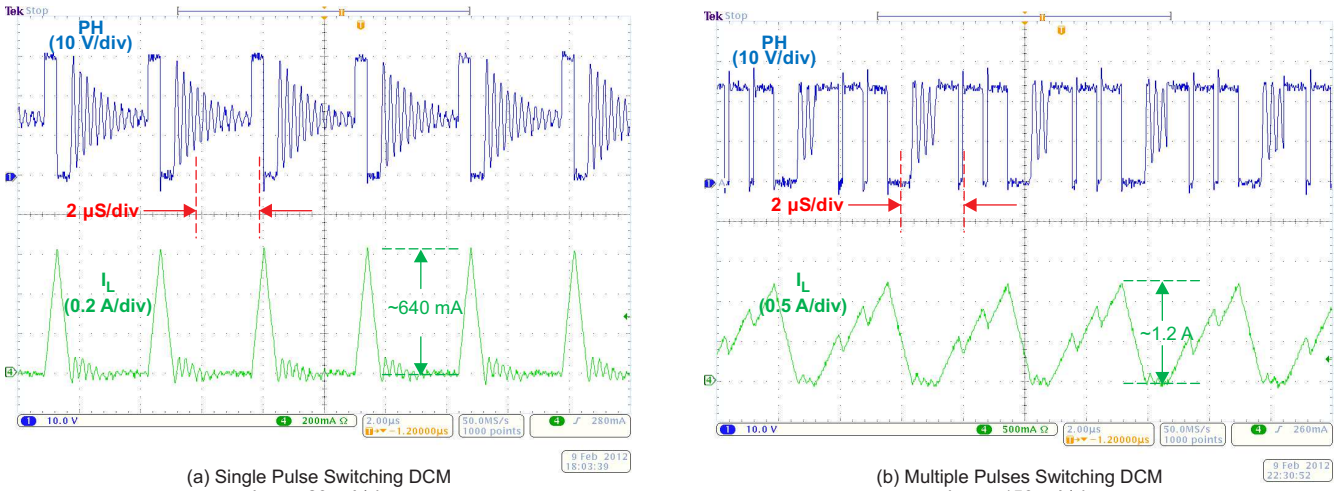


Figure 37. $I_{OUT(BUCK)}$ vs Selected Inductance Value

Figure 38 shows a comparison of these two modes. Table 22 shows the main differences between these two operating modes.



(a) Single Pulse Switching DCM
I_{LED} = 20 mA/ch

(b) Multiple Pulses Switching DCM
I_{LED} = 150 mA/ch

Figure 38. Single Pulse-Switching DCM Mode vs Multiple Pulse-Switching DCM Mode

Table 22. Single and Multiple DCM Comparison (n = integer)

Parameter	(a) Single	(b) Multi
I_{LPK} (in amps)	1.25 × 2 × $I_{OUT(BUCK)}$ / η × D/D_{Min}	1.25 × 2 × $I_{OUT(BUCK)}$ / η × (n + 1)/n
f	1.25 MHz	1.25/n MHz

Appendix C Numerical Examples of Inductance Calculation

C.1 VIN = 24 V, I_O = 150 mA, Four Series-Connected LEDs, 4-Wire Communication

The target setting is given as follows:

VIN_{Max} = 24 V
VIN_{Min} = 20 V
$VLED_{Max}$ = 14 V
$VLED_{Min}$ = 12.6 V

First, calculate the duty cycle, as shown in Equation 26:

$$D_{Max} = \frac{14}{20} = 70.0\%$$

$$D_{Min} = \frac{12.6}{24} = 52.5\%$$

Where D = 80% for this example. (26)

Next, calculate the average current; 150 mA × 3 channels, and assuming 70-mA serial-interface power consumption for 4-wire communication (see Table 11).

$I_{OUT(BUCK)}$ = 3 × 150 + 70 = 520 mA (27)

Assuming a dc-dc converter efficiency of 0.9, the required peak current is shown in Equation 28:

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{D}{D_{Min}} = 2.2 \text{ A} \quad (28)$$

Note that 2.2 A is too large. Therefore, consider using the multiple switching DCM region to lower the peak current value. In this case, *n* = 4 is applied, as shown in Equation 29:

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{n+1}{n} = 1.8 \text{ A} \quad (29)$$

Now the appropriate *L* can be calculated, as shown in Equation 30:

$$L < \frac{D \times (1-D) \times VIN_{Min}}{2 \times f_{DCM} \times I_{OUT(BUCK)}} = 12.3 \text{ µH} \quad (30)$$

Therefore, a good starting point is 10 µH / 2 A peak current value. In this example, f_{DCM} is set to 250 kHz.

C.2 VIN = 36 V, I_O = 20 mA, Six Series-Connected LEDs, and 2-Wire Communication

Here is another example, with the lower LED current condition of the reference design shown in Section 7.

VIN_{Max} = 36 V
VIN_{Min} = 28 V
$VLED_{Max}$ = 21 V
$VLED_{Min}$ = 17 V

First, the duty cycle is calculated, as shown in Equation 31.

$$D_{Max} = \frac{21}{28} = 75.0\%$$

$$D_{Min} = \frac{17}{36} = 47.2\% \quad (31)$$

For this example, select D = 80%.

$$I_{OUT(BUCK)} = 3 \times 20 + 40 = 100 \text{ mA}$$

$$I_{LPK} = 1.25 \times \frac{2 \times I_{OUT(BUCK)}}{\eta} \times \frac{D_{Min}}{D} = 0.47 \text{ A} \quad (32)$$

As the equation shows, the inductor peak current is small enough. If the selected inductor saturation current (L_{Sat}) is large enough, a smaller inductor value can be selected for a smaller form factor. For example, use a maximum peak current setting of I_{LPK} = I_{Sat} = 1.2 A in order to reduce the required inductance value, as shown in Equation 33:

$$L > \frac{(VIN_{Max} - VLED_{Min}) \times D}{I_{LPK} \times f_{MAX}} = 8.4\ \mu H \quad (33)$$

According to Figure 39, with 10 µH and a duty cycle = 80% setting, the peak current of 1.2 A is located between the boundary (denoted as red solid line) of the *Single Switching DCM* and the *Multiple Pulses Switching DCM* operating modes.

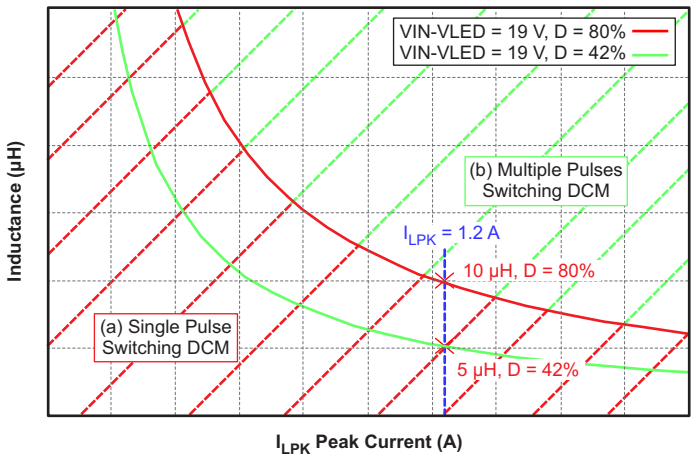


Figure 39. Inductance vs Peak Current Relationship: VIN – VLED = 19 V

Furthermore, in this lower peak current operation, smaller inductance values with lower duty cycles can be used. Figure 39 shows the boundary condition of 5 µH and a 42% duty cycle as the green solid line, and the boundary condition of 10 µH and 80% as the red solid line. These two conditions provide a similar peak current; this is enough peak current to supply the currents to the LED modules. Section 7 takes this approach (5 µH, duty cycle = 42%, L_{Sat} = 1.8 A) to pursue a small footprint design.

Appendix D References

[1] TLC5970 Datasheet http://www.ti.com/product/tlc5970

[2] Texas Instruments Lighting Solutions http://www.ti.com/led

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