Application Report
SCAA060B–February 2003–Revised December 2009

Using the CDC7005 as a 1:5 PECL Buffer With a Programmable Divider Ratio on Each Output

Justo Lapiedra — *ICP-Clock DIstribution Circuits*

ABSTRACT

The CD7005 is a clock synchronizer that can also be used as a simple PECL clock buffer with divide by 1, /2, /4, /8, or /16 option. The divide ratio can be changed independently for each output through the serial port interface (SPI).

This application note shows how to use the CDC7005 as a PECL clock buffer. The document is optimized to simplify design work and understanding of the CDC7005 in this clock buffer application. Therefore, a new pin name assignment is given. The essential features of the CDC7005 when used as a PECL buffer are given in this report, while the unused building blocks of the CDC7005 (e.g., the PLL) are taken out of the documentation.

See the CDC7005 data sheet (SCAS685) for further information.

Contents

List of Figures

1 Feature List and Simplified Package Drawing

- Frequency Range Up to 800 MHz
- Supports Five Differential LVPECL Outputs
- Each Output Frequency Is Selectable by x1, /2, /4, /8, /16
- All Outputs Are Synchronized With Low Output Skew
- SPI Controllable Division Setting
- 3.3-V Power Supply
- High Performance 1:5 PLL Clock Buffer and Divider
- Packaged in 64-Pin BGA (0,8 mm Pitch – ZVA)
- Industrial Temperature Range –40°C to 85°C

ZVA Package
(Top View)

	1	2	3	4	5	6	7	8
A	CTRL_LE	CTRL _CLK	CTRL _DATA	NC	GND	VCC	NC	NC
B	GND	GND	GND	GND	GND	GND	GND	GND
C	NC	GND	VCC	VCC	VCC	VCC	VCC	NC
D	CLK	GND	GND	GND	GND	GND	VCC	NC
E	CLKB	GND	VCC	VCC	VCC	VCC	VCC	VCC
F	Y0	GND	GND	GND	GND	GND	VCC	Y4B
G	Y0B	VCC	VCC	VCC	VCC	VCC	VCC	Y4
H	$\overline{\text{PWRDN}}$	Y1	Y1B	Y2	Y2B	Y3	Y3B	$\overline{\text{RESET}}$

P0022-02

2 Device Description

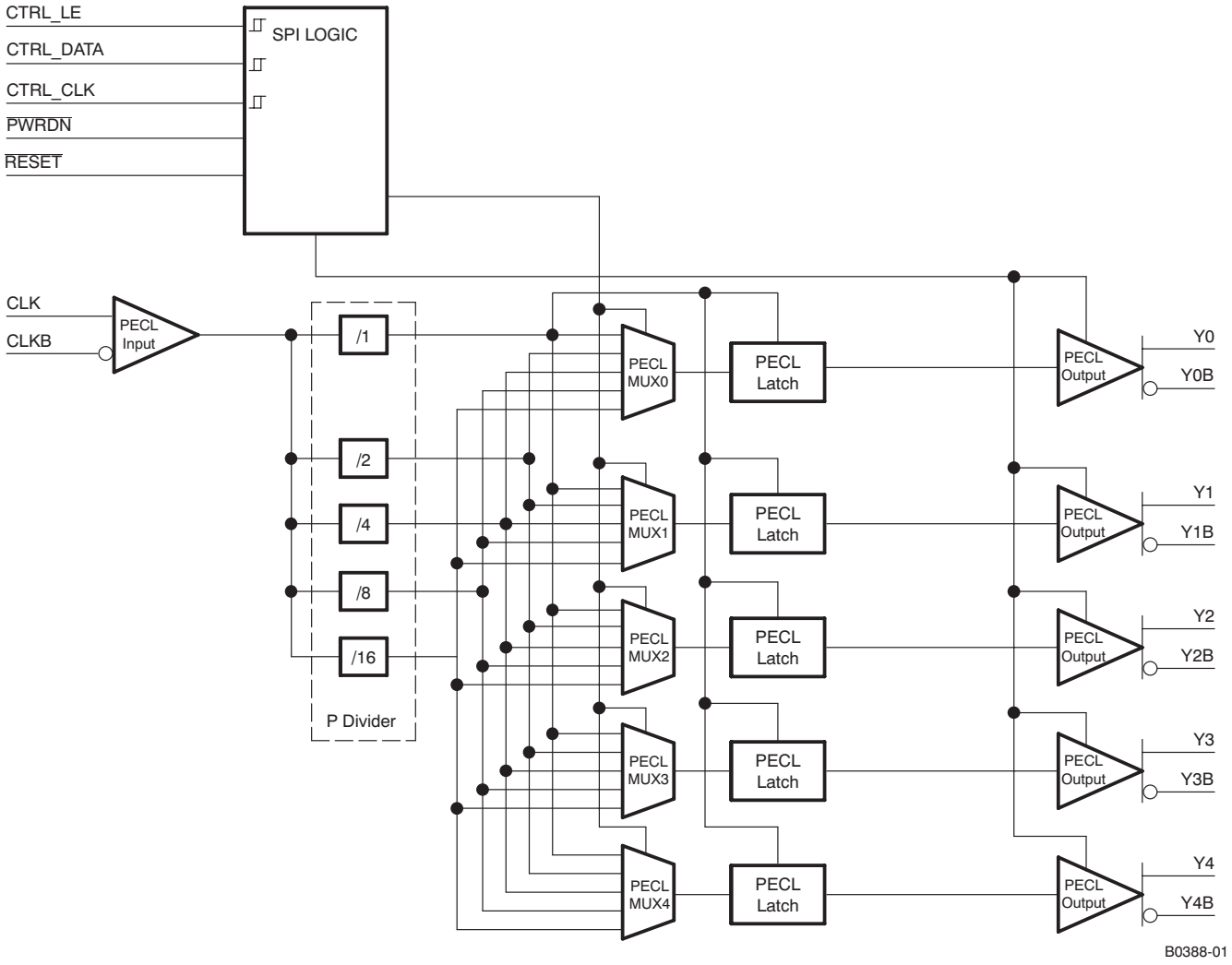
The CDC7005 1:5 PECL buffer is a high-performance, low-phase noise and low skew clock buffer and clock divider. The supported frequency range of operation is up to 800 MHz. Each of the five differential LVPECL outputs is programmable by a serial peripheral interface (SPI). The SPI allows individual control of the frequency and enable/disable state of each output. The device operates in 3.3-V environment. The built-in latches ensure that all outputs are synchronized.

At power up, the configuration of the five outputs is as follows:

Y0 - div1	Y1 - div2	Y2 - div4	Y3 - div8	Y4 - div8

The CDC7005 is characterized for operation from –40°C to 85°C.

3 Functional Block Diagram



4 Pin Description

PIN		TYPE	DESCRIPTION
NAME	NO.		
Y[0:4]	F1, H2, H4, H6, G8	O	LVPECL output
Y[0:4]_B	G1, H3, H5, H7, F8	O	LVPECL output inverted
VCC	D7, E3-E8, F7, G2-G7, A6, C3-C7	Power	3.3-V supply
GND	A5, B1-B8, C2, D2-D6, E2, F2-F6	Ground	Ground
CTRL_LE	A1	I	LVCMOS input, control load enable for serial programmable interface (SPI), with hysteresis
CTRL_CLK	A2	I	LVCMOS input, serial control clock input for SPI, with hysteresis
CTRL_DATA	A3	I	LVCMOS input, serial control data input for SPI, with hysteresis
$\overline{\text{PWRDN}}$	H1	I	LVCMOS input, asynchronous power down (PD) signal active on low. Switches all current sources off, resets all dividers, and 3-states all outputs, has internal 150-kΩ pullup resistor
$\overline{\text{RESET}}$	H8	I	LVCMOS input, asynchronous reset signal active on low. Resets all dividers; has internal 150-kΩ pullup resistor
CLK	D1	I	LVPEC input
CLKB	E1	I	Complementary LVPECL input
NC	A4, A7, A8, C1, C8, D8	O	Not connected: These pins must be left unconnected and are not allowed to be tied to VCC or GND.

5 Programming the SPI Interface

The serial interface of the CDC7005 is a simple SPI-compatible interface for writing to the registers of the device. It consists of three control lines CTRL_CLK, CTRL_DATA, and CTRL_LE. There are three 32 bit wide registers, which can be addressed by the two LSB of a transferred word (bit 0 and bit 1). Every transmitted word must have 32 bits, starting with MSB. Each word can be written separately.

The transfer is initiated with the falling edge of CTRL_LE; as long as CTRL_LE is high, no data can be transferred. During CTRL_LE, low data can be written. The data has to be applied at CTRL_DATA and has to be stable before the rising edge of CTRL_CLK. The transmission is finished by a rising edge of CTRL_LE.

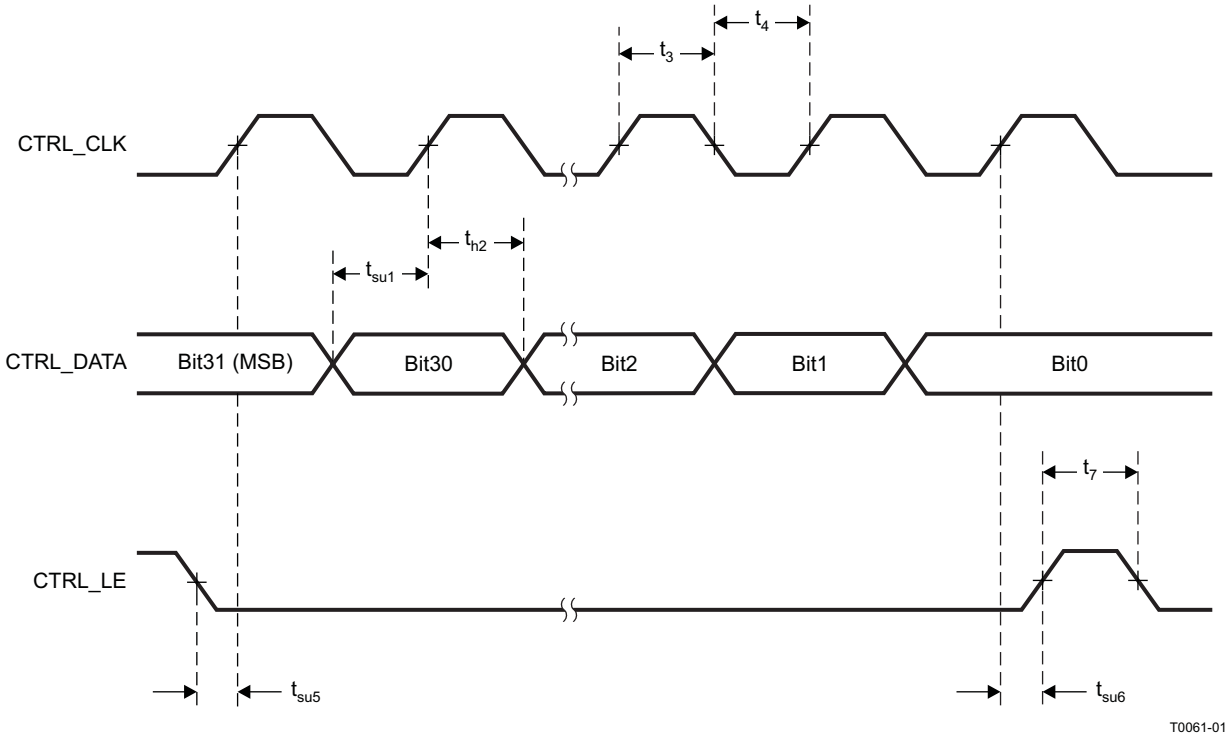


Figure 1. Timing Diagram SPI Control Interface

5.1 Word 0

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER UP CONDITION	PIN AFFECTED
0	Reserved Always write the same bits to these cells as given in the row: power up conditions				0	Reserved
1					0	
2					1	
3					1	
4					1	
5					1	
6					1	
7					1	
8					1	
9					0	
10					0	
11					0	
12					0	
13					0	
14					0	
15					0	
16					0	
17					0	
18					1	
19					0	
20					0	
21					1	
22	Y03St	Output 3-State	Y0 3-state (1 = output enabled)	W	1	F1, G1
23	Y13St		Y1 3-state (1 = output enabled)	W	1	H2, H3
24	Y23St		Y2 3-state (1 = output enabled)	W	1	H4, H5
25	Y33St		Y3 3-state (1 = output enabled)	W	1	H6, H7
26	Y4St		Y4 3-state (1 = output enabled)	W	1	G8, F8
27	Reserved Always write the same bits to these cells as given in the row: power up conditions				1	Reserved
28					0	
29					1	
30					1	
31					0	

5.2 Word 1

BIT	BIT NAME		DESCRIPTION / FUNCTION	TYPE	POWER UP CONDITION	PIN AFFECTED
0	Reserved Always write the same bits to these cells as given in the row: power up conditions				1	Reserved
1					0	
2					1	
3					1	
4					1	
5					1	
6					1	
7					1	
8					1	
9					0	
10					0	
11					0	
12					0	
13					0	
14					0	
15	MUX00	MUX0	MUX0 Select Bit 0	W	0	F1, G1
16	MUX01		MUX0 Select Bit 1	W	0	F1, G1
17	MUX02		MUX0 Select Bit 2	W	0	F1, G1
18	MUX10	MUX1	MUX1 Select Bit 0	W	1	H2, H3
19	MUX11		MUX1 Select Bit 1	W	0	H2, H3
20	MUX12		MUX1 Select Bit 2	W	0	H2, H3
21	MUX20	MUX2	MUX2 Select Bit 0	W	0	H4, H5
22	MUX21		MUX2 Select Bit 1	W	1	H4, H5
23	MUX22		MUX2 Select Bit 2	W	0	H4, H5
24	MUX30	MUX3	MUX3 Select Bit 0	W	1	H6, H7
25	MUX31		MUX3 Select Bit 1	W	1	H6, H7
26	MUX32		MUX3 Select Bit 2	W	0	H6, H7
27	MUX40	MUX4	MUX4 Select Bit 0	W	1	G8, F8
28	MUX41		MUX4 Select Bit 1	W	1	G8, F8
29	MUX42		MUX4 Select Bit 2	W	0	G8, F8
30	Reserved Always write the same bits to these cells as given in the row: power up conditions				1	Reserved
31					0	

5.3 Word 2 and Word 3

SPI word 2 and word 3 are not required to be programmed for using the CDC7005 as a PECL clock divider and/or buffer.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265