LVT-to-LVTH Conversion

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Abstract

Original LVT devices that have bus hold have been redesigned to add the High-Impedance State During Power Up and Power Down feature. Additional devices with and without bus hold have been added to the LVT product line. Design guidelines and issues related to the bus-hold features, switching characteristics, and timing requirements are discussed.

Introduction

In 1992, Texas Instruments (TI^{M}) introduced the LVT low-voltage BiCMOS logic family. All of the devices in the LVT family had bus hold as a feature. In 1996, in response to market demands, redesign of the LVT family began to enhance performance. As part of this redesign, all devices were renamed to LVTH to denote the bus-hold feature explicitly in the device name, and to standardize the bus-hold naming convention used on all TI logic families.

With this redesign, switching performance generally improved, timing requirements changed, and the High-Impedance State During Power Up and Power Down feature was added to all devices in this family. To facilitate the conversion of applications from LVT devices to their LVTH replacements, a device conversion guide, an explanation of the High-Impedance State During Power Up and Power Down feature, changes in bus-hold requirements, and a discussion of the changes to switching and timing requirements are included in this application report.

Conversion Guide

The original LVT devices had the bus-hold feature. The LVTH replacements for these devices not only have bus hold, but also have the High-Impedance State During Power Up and Power Down feature. Table 1 shows the LVTH replacement device for every LVT octal device. Table 2 shows the LVTH replacement device for every LVT Widebus™ device.

LVT OCTAL FUNCTION	REPLACEMENT LVTH OCTAL FUNCTION
LVT125	LVTH125
LVT240	LVTH240
LVT241	LVTH241
LVT244/LVT244A	LVTH244A
LVT245/LVT245A	LVTH245
LVT273	LVTH273
LVT543	LVTH543
LVT573	LVTH573
LVT574	LVTH574
LVT646	LVTH646
LVT652	LVTH652
LVT2952	LVTH2952

	Table 1.	Octal-Function	Conversion
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TI and Widebus are trademarks of Texas Instruments Incorporated.

LVT WIDEBUS FUNCTION	REPLACEMENT LVTH WIDEBUS FUNCTION
LVT16244/LVT16244A	LVTH16244A
LVT162244	LVTH162244
LVT16245/LVT16245A	LVTH16245A
LVT162245	LVTH162245
LVT16373	LVTH16373
LVT16374	LVTH16374
LVT16500	LVTH16500
LVT16501	LVTH16501
LVT16543	LVTH16543
LVT16646	LVTH16646
LVT16835	LVTH16835
LVTH16952	LVTH16952

Table 2. Widebus-Function Conversion

The original LVTZ products had the High-Impedance State During Power Up and Power Down feature. These devices also had bus hold, as did the original LVT devices. The LVTH device is a direct feature-for-feature replacement for LVTZ. Table 3 shows the LVTH replacement device for every LVTZ device.

Table 3. LVTZ-Function Conversion

LVTZ OCTAL FUNCTION	REPLACEMENT LVTH OCTAL FUNCTION
LVTZ240	LVTH240
LVTZ244	LVTH244A
LVTZ245	LVTH245A

Also, 14 devices with bus hold that were not available in the original LVT product line were added in the redesigned LVT product line. These devices are shown in Table 4.

Table 4. New Functions With Bus Hold in the Redesigned LVT Product Line

LVTH2245
LVTH373
LVTH374
LVTH540
LVTH541
LVTH16240
LVTH162240
LVTH16241
LVTH162241
LVTH162373
LVTH162374
LVTH16541
LVTH162541
LVTH16652

Also, three octal functions without bus hold are new to the LVT product line. These devices are shown in Table 5. Care should be taken not to confuse these with the replacements for the original LVT240, LVT244A, and LVT245A devices, which had bus hold and for which LVTH replacements are shown in Table 1.

Table 5.	New Functions	Without Bus	Hold in the	Redesigned L	T Product Line
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LVT240A
LVT244B
LVT245B

High-Impedance State During Power Up and Power Down

High-Impedance State During Power Up and Power Down is one of the features that has been added with the redesign of LVT devices. This feature enables the LVTH replacement devices to better support insertion into or removal from systems that are powered on.

Device capability for supporting live insertion is noted by the specification of output-pin current (I_{OZPU} and I_{OZPD}) while V_{CC} is suboperational. Typically, I_{OZPU} and I_{OZPD} are tested at pin voltages that approximate valid logic low and high levels for that pin (0.5V, 3V). The I_{OZPU} and I_{OZPD} currents at each level are specified in the range of ±50 µA and are tested for V_{CC} in the range below a level at which the circuit is expected to be functionally operational (1.5 V for LVT and LVTH devices).

Figures 1 through 4 demonstrate the effect of the High-Impedance State During Power Up and Power Down feature on the V_{CC} level at which the LVTH device outputs become active, in comparison to the LVT device outputs that lack this feature. In the I_{OZL} plots, the output is pulled to ground through a 500- Ω resistor so that, while the output is in the high-impedance state, the output will be low. The input is biased so that the output will drive to a valid logic-high state when active. In the I_{OZH} plots, the output is pulled to a valid high state through a 500- Ω pullup resistor, so that while the output is in the high-impedance state, the output will be high. The input is biased such that the output will drive to a valid logic-low state when active.

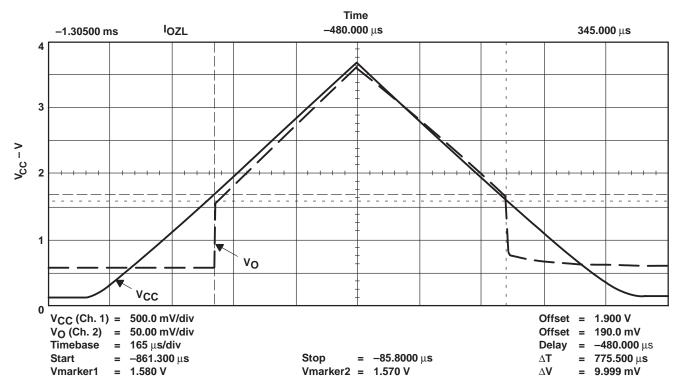


Figure 1. LVT16244A at 85°C With Input Biased to Drive Output High When Active

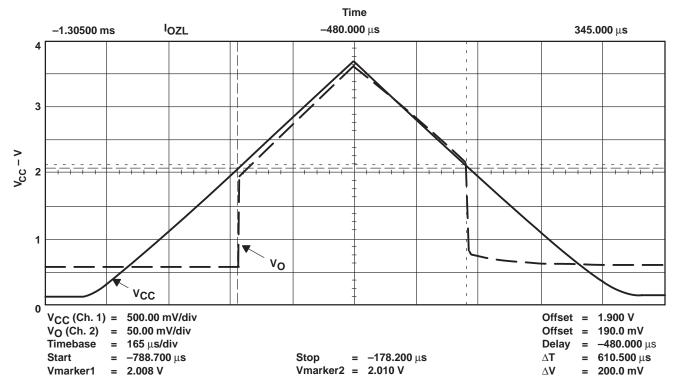


Figure 2. LVTH16244A at 85°C With Input Biased to Drive Output High When Active

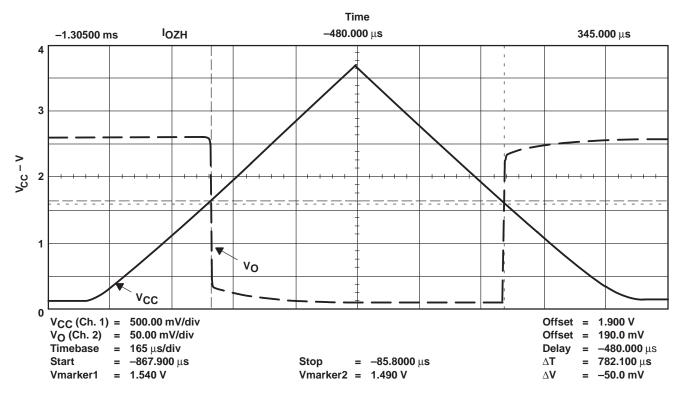


Figure 3. LVT16244A at 85°C With Input Biased to Drive Output Low When Active

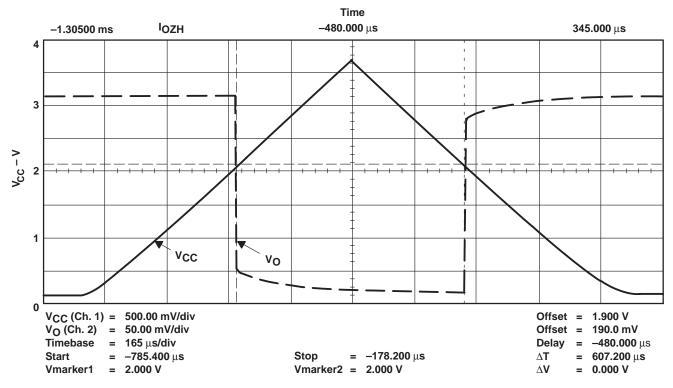


Figure 4. LVTH16244A at 85°C With Input Biased to Drive Output Low When Active

Figures 1 and 3 show that, once the V_{CC} of the LVT16244A exceeds about 1.5 V on power up or that the V_{CC} drops below about 1.5 V on power down, the outputs become active or enter the high-impedance state, respectively. Figures 2 and 4 show that once the V_{CC} of LVTH16244A exceeds about 2 V on power up or that V_{CC} drops below about 2 V on power down, the outputs become active or enter the high-impedance state, respectively.

These figures demonstrate that, while the original LVT devices do exhibit a high-impedance characteristic during the initial phase of power up and final phase of power down, they do so only below V_{CC} levels that are too low to provide adequate margin versus the I_{OZPU} and I_{OZPD} specifications. The new LVTH devices, with the deliberately designed High-Impedance State During Power Up and Power Down feature, do provide adequate margin to the specifications.

Finally, when the device is fully powered, the High-Impedance State During Power Up and Power Down feature does not affect operation or any other specifications of the device. This feature is active and affects device operation only during power up and power down.

Design Guidelines and Issues Concerning the Bus-Hold Feature

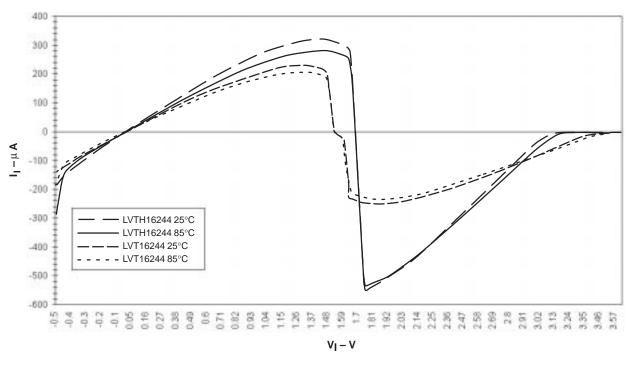
The original LVT product line had the bus-hold feature on all data inputs. When the LVT product line was redesigned, the names were changed to match TI standard naming conventions for bus hold. There have been some issues concerning the bus-hold feature on the replacement LVTH devices versus the original LVT devices. Among the issues are the differences in bus-hold current requirements between some LVTH devices and the LVT devices they replace: overdrive current required to ensure switching of an input from one state to the other and tie-off of bus-hold data inputs.

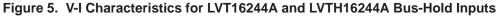
Bus hold is intended to remove the requirement to tie-off unused data inputs. The bus-hold feature is only on the data inputs and data I/O pins of the LVTH devices. Unused control pins still must be tied off to ensure that the input does not float.

LVTH devices in the redesigned product line have one of two versions of the bus-hold circuit. The devices with Type-A circuits have a recommended overdrive current of 750 μ A. The devices with Type-B circuits have a recommended overdrive current of 500 μ A. The original LVT family had a recommended overdrive current of 500 μ A. See Table 6 for a list of LVTH devices that have the Type-A circuit and those that have the Type-B circuit. Overdrive current is the current required to ensure that a bus-hold input is switched from one logic state to the other. Devices with the Type-B circuit are not significantly different from the LVT devices they replace. However, devices with the Type-A circuit must be comprehended when converting an application to use the LVTH device, especially if pullup or pulldown resistors are used at the inputs. Figure 5 shows a comparison of the V-I characteristics of a bus-hold data input on the LVT16244A and the replacement LVTH16244A.

CIRCUIT TYPE	DEVICES
Туре А (750 μА)	LVTH240, LVTH241, LVTH244A, LVTH245A, LVTH2245, LVTH273, LVTH373, LVTH374, LVTH16240, LVTH162240, LVTH16241, LVTH162241, LVTH16244A, LVTH162244, LVTH16245A, LVTH162245, LVTH16373, LVTH162373, LVTH16374, LVTH162374, LVTH162374, LVTH16541, LVTH162541
Туре В (500 μА)	LVTH125, LVTH540, LVTH541, LVTH543, LVTH573, LVTH574, LVTH646, LVTH652, LVTH2952, LVTH16500, LVTH16501, LVTH16543, LVTH16646, LVTH16652, LVTH16835, LVTH16952







Although bus hold eliminates the need to tie-off unused data inputs, there are other situations that require tie-off. When tie-off of inputs is required, the pullup or pulldown mechanism must be able to sink or source the recommended overdrive current to ensure that the input will be pulled to the desired state. See Table 7 for the recommended resistor size for the most common tie-off voltages.

 Table 7. Recommended Resistor Values for Tie-Off

BUS-HOLD			TIE-OFF	OLTAGE		
CIRCUIT TYPE	0 V	2.7 V	3.0 V	3.3 V	3.6 V	5.0 V
Type A (750 uA)	<1.35 kΩ	<1.08 kΩ	<1.48 kΩ	<1.88 kΩ	<2.28 kΩ	<4.15 kΩ
Type B (500 uA)	<2.02 kΩ	<1.62 kΩ	<2.22 kΩ	<2.82 kΩ	<3.42 kΩ	<6.22 kΩ

Another consideration for bus-hold inputs is that multiple bus-hold data inputs on a node increase the overdrive-current requirements for that node. The current requirement is a parallel condition. For example, if the bus-hold inputs of an LVTH244A device and an LVTH574 device were connected on the same node, the node would require 1.25 mA of overdrive current to ensure that the inputs are driven to the correct logic state. This is extensible for three or more devices as well; the total overdrive current for a node is the sum of the individual overdrive currents of each connected device pin.

Switching Characteristics and Timing Requirements

As a result of the redesign of the original LVT product line, switching characteristics and timing requirements of most LVTH replacement devices have changed.

Table 8 shows an example of the switching-characteristics and timing-requirements specification-change summary for all devices that are moving from LVT to LVTH. The specification-change summaries are provided in the Product Change Notifications (PCN) for the devices in question. See Table 8 to determine which PCN has this information for a given original LVT device. Any specifications from the data sheet that are not listed have not changed with the LVTH replacement. In Table 9, for specifications that are listed, only items that are in bold underlined italics are changed from the original LVT device.

PCN NUMBER	DEVICES						
PCN 5287	LVT240, LVT244A, LVTZ244, LVT245A, LVT273, LVT16244A, LVT162244, LVT16373, LVT16374						
PCN 5287A	LVTZ240, LVT241, LVTZ245, LVT543, LVT573, LVT574, LVT646, LVT652, LVT2952, LVT16245A, LVT162245						
PCN 5287B	LVT16543, LVT16646, LVT16952						
PCN 5287C	LVT125						
PCN 5287D	LVT16500, LVT16501, LVT16835						

Table 8. PCN-to-Device Cross-Reference

In the case of the LVT16835 versus LVTH16835, as shown in Table 9, setup times for data before LE, and hold times for data after CLK and data after LE have improved. Also, maximum propagation delays have been improved significantly. However, because all design features are tradeoffs, minimum propagation delays are lower and the setup time of data before CLK has increased slightly. See device data sheets for all specifications and parameter values.

Generally, the switching characteristics and timing requirements have improved. These specification changes should be considered when converting an application from an original LVT device to an LVTH replacement.

			$V_{CC} = 3.3 V \pm 0.3 V$						$V_{CC} = 2.7 V$				
		OLD			NEW			OLD		NEW			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	74LVT16835			74LVTH16835			74LVT16835		74LVTH16835		UNIT
TARAWETER			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII
fclock	Clock frequency		0		150			150	0	125		<u>150</u>	MHz
t _{su}	Data before CLK↑		1.6			<u>2.1</u>			2.1		<u>2.4</u>		ns
t _{su}	Data before LE↑, CLK high		2.6			<u>2.3</u>			1.9		<u>1.5</u>		ns
t _{su}	Data before LE↑, CLK low		2			<u>1.5</u>			1.3		<u>0.5</u>		ns
^t h	Data after CLK↑		2			<u>1.0</u>			2.1		<u>0.0</u>		ns
th	Data after LE↑		0.9			<u>0.8</u>			1.2		<u>0.8</u>		ns
f _{max}			150			150			125		<u>150</u>		MHz
^t PLH	А	Y	1.7	3	5.4	<u>1.3</u>	<u>2.6</u>	<u>3.7</u>		6.8		<u>4</u>	ns
^t PHL	А	Y	1.6	3.2	5.9	<u>1.3</u>	<u>2.4</u>	<u>3.7</u>		7.7		<u>4</u>	ns
^t PLH	LE	Y	2.3	4	7	<u>1.5</u>	<u>3.2</u>	<u>5.1</u>		8.5		<u>5.7</u>	ns
^t PHL	LE	Y	2.7	4.3	7.9	<u>1.5</u>	<u>3.3</u>	<u>5.1</u>		9.7		<u>5.7</u>	ns
^t PLH	CLK	Y	2.5	4.1	7.9	<u>1.5</u>	<u>3.5</u>	<u>5.1</u>		9.2		<u>5.7</u>	ns
^t PHL	CLK	Y	3.5	5.4	8.9	<u>1.5</u>	<u>3.4</u>	<u>5.1</u>		10.4		<u>5.7</u>	ns
^t PZH	ŌĒ	Y	1.2	3	5	<u>1.3</u>	<u>2.9</u>	<u>4.6</u>		5.9		<u>5.5</u>	ns
^t PZL	ŌE	Y	1.5	3	5.8	<u>1.3</u>	3	<u>4.6</u>		6.9		<u>5.5</u>	ns
^t PHZ	ŌE	Y	2.7	4.6	7.4	<u>1.7</u>	<u>4.2</u>	<u>5.8</u>		8.3		<u>6.3</u>	ns
tpLZ	ŌE	Y	2.8	4.7	6.7	<u>1.7</u>	<u>3.7</u>	<u>5.8</u>		7.2		<u>6.3</u>	ns

Table 9. Comparison of LVT16835 and LVTH16835 Timing Requirements and Propagation Delays

Summary

The LVTH devices are offered as replacements for the original LVT devices. The LVTH devices, with enhanced performance and added High-Impedance State during Power Up and Power Down feature, are drop-in replacements for the original LVT devices if the changes in bus hold, switching characteristics, and timing requirements are addressed.

Acknowledgment

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References

LVT Logic Low-Voltage Technology Data Book, 1998, literature number SCBD154.

The following Product Change Notifications are available on the TI web page at http://www.ti.com/sc/docs/asl/pcns.htm.

PCN5287 PCN5287A PCN5287B PCN5287C PCN5287D