- Single Down/Up Count-Control Line
- Look-Ahead Circuitry Enhances Speed of Cascaded Counters
- Fully Synchronous in Count Modes
- Asynchronously Presettable With Load Control
- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

**SN54ALS191A . . . J PACKAGE**
**SN74ALS191A . . . D OR N PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| B | 1 | 16 | $V_{CC}$ |
| $Q_B$ | 2 | 15 | A |
| $Q_A$ | 3 | 14 | CLK |
| $\overline{CTEN}$ | 4 | 13 | RCO |
| D/$\overline{U}$ | 5 | 12 | MAX/MIN |
| $Q_C$ | 6 | 11 | $\overline{LOAD}$ |
| $Q_D$ | 7 | 10 | C |
| GND | 8 | 9 | D |

**SN54ALS191A . . . FK PACKAGE**
**(TOP VIEW)**

Pins (top, left to right): $Q_B$ (3), B (2), NC (1), $V_{CC}$ (20), A (19)

Left side: $Q_A$ (4), $\overline{CTEN}$ (5), NC (6), D/$\overline{U}$ (7), $Q_C$ (8)

Right side: CLK (18), RCO (17), NC (16), MAX/MIN (15), $\overline{LOAD}$ (14)

Bottom: $Q_D$ (9), GND (10), NC (11), D (12), C (13)

NC – No internal connection

## description

The 'ALS191A are synchronous 4-bit reversible up/down binary counters. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.
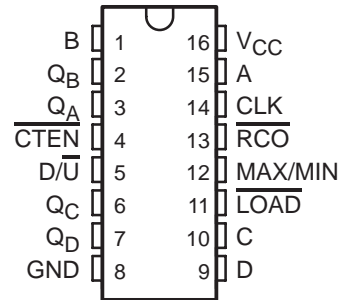
The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock (CLK) input if the count enable ($\overline{CTEN}$) input is low. A high at $\overline{CTEN}$ inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up, and when D/$\overline{U}$ is high, the counter counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($\overline{CTEN}$ and D/$\overline{U}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter is dictated solely by the conditions meeting the stable setup and hold times.
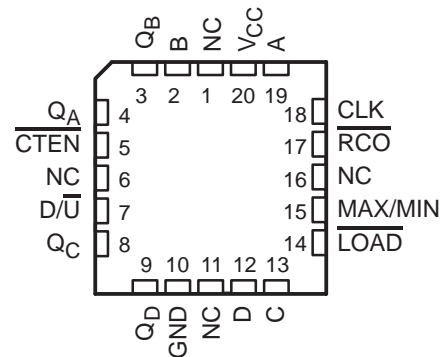
These counters are fully programmable. Each output can be preset to either level by placing a low on the $\overline{LOAD}$ input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

CLK, D/$\overline{U}$, and $\overline{LOAD}$ are buffered to lower the drive requirement, which significantly reduces the loading on (current required by) clock drivers, for long parallel words.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TEXAS INSTRUMENTS**

## description (continued)

Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is minimum (0) counting down or maximum (15) counting up. The ripple-clock output ($\overline{RCO}$) produces a low-level output pulse under those same conditions, but only while the clock input is low. The counter easily can be cascaded by feeding the ripple-clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count (MAX/MIN) output can be used to accomplish look ahead for high-speed operation.

The SN54ALS191A is characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74ALS191A is characterized for operation from $0°C$ to $70°C$.

## logic symbol†
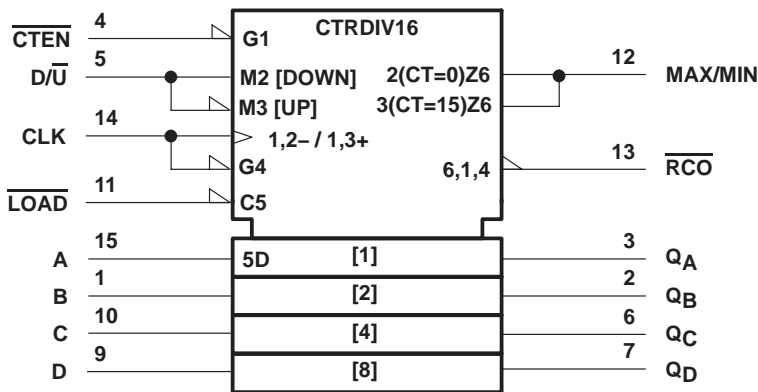


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

## logic diagram (positive logic)
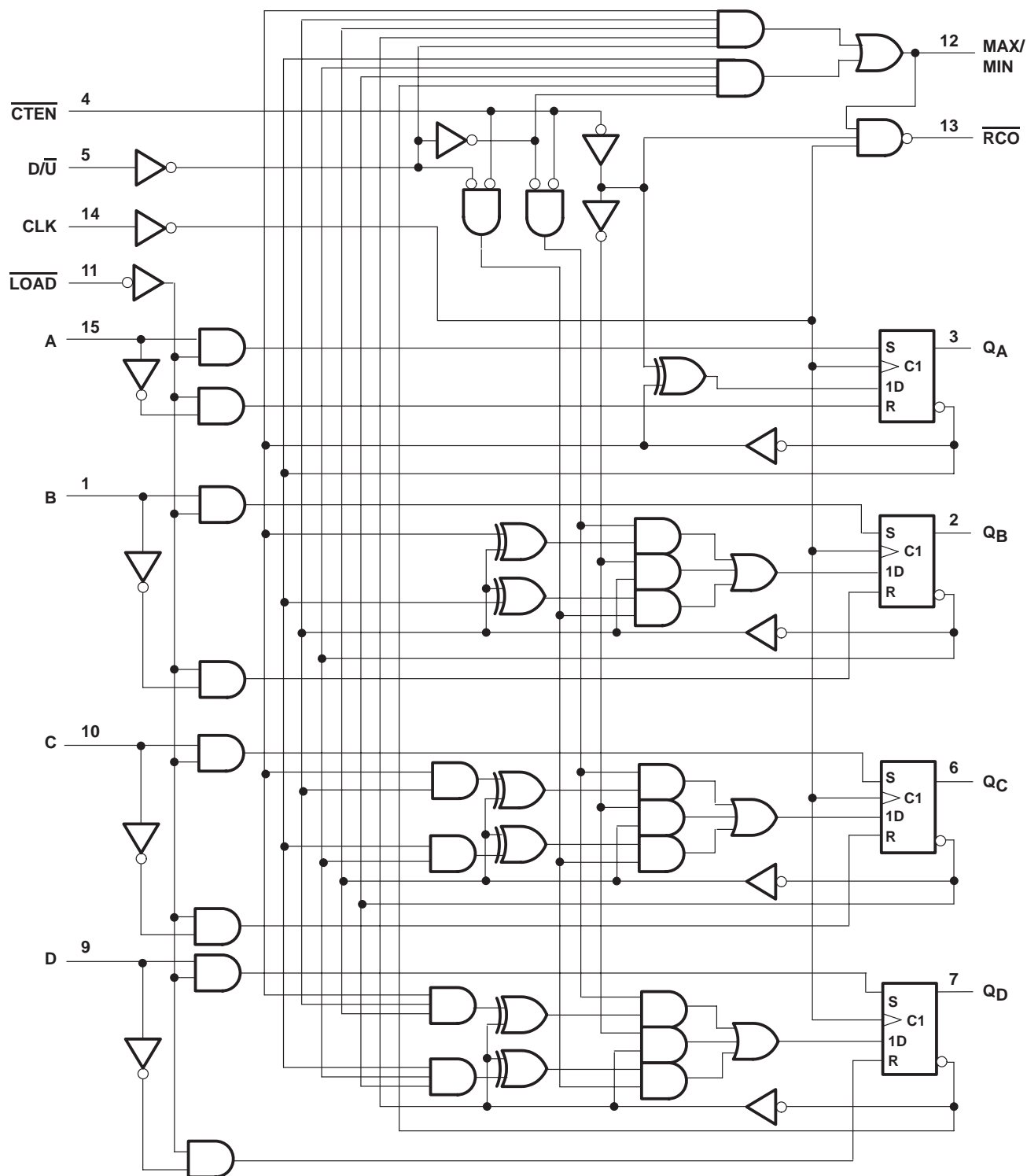


Pin numbers shown are for the D, J, and N packages.

## typical load, count, and inhibit sequences

The following sequence is illustrated below:

1. Load (preset) to binary 13

2. Count up to 14, 15 (maximum), 0, 1, and 2

3. Inhibit

4. Count down to 1, 0 (minimum), 15, 14, and 13
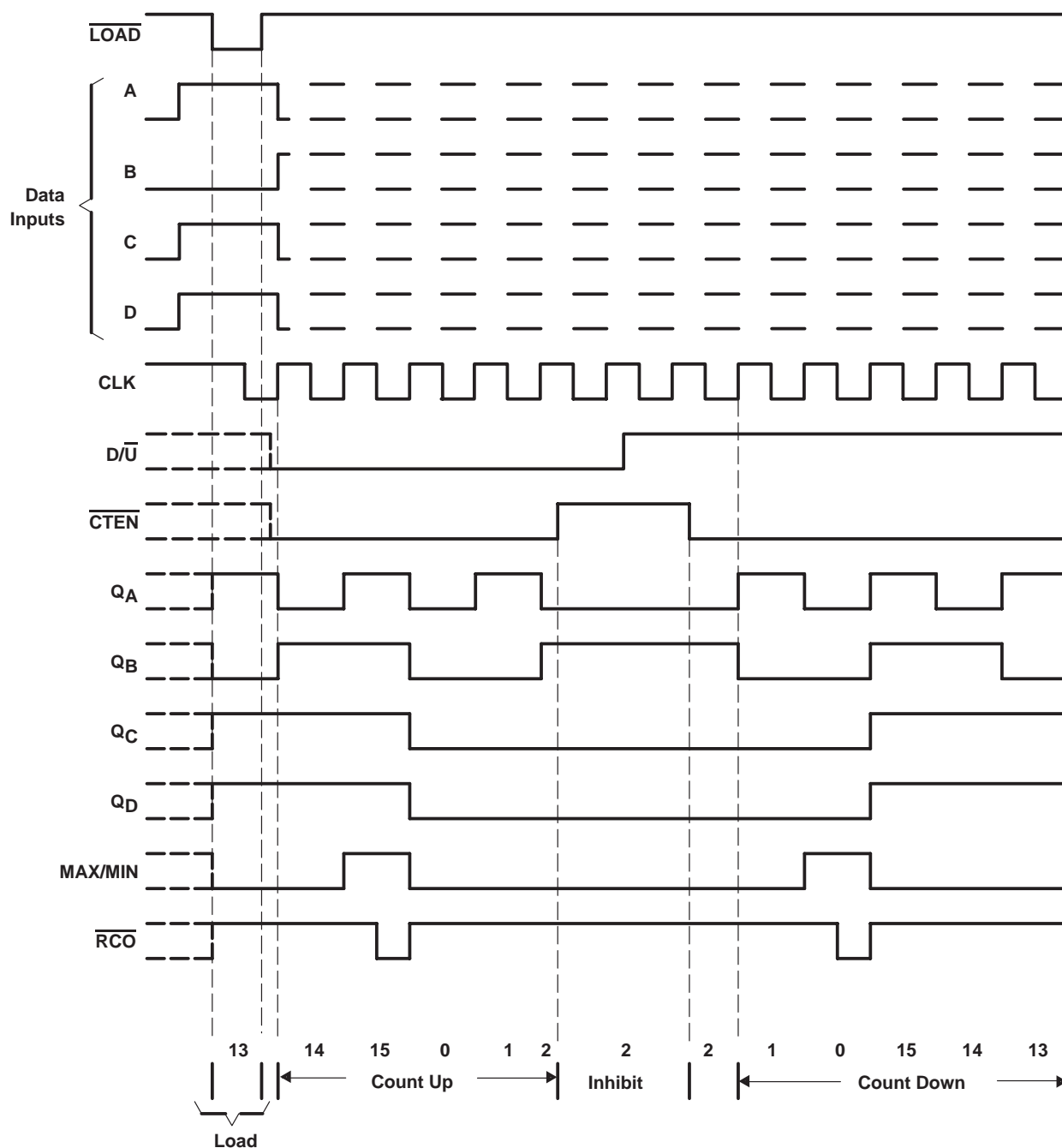
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265
POST OFFICE BOX 1443 ● HOUSTON, TEXAS 77251–1443

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ ........................................................................ 7 V
Input voltage, $V_I$ ........................................................................ 7 V
Operating free-air temperature range, $T_A$: SN54ALS191A ............................. −55°C to 125°C
$\quad\quad$ SN74ALS191A ............................. 0°C to 70°C
Storage temperature range, $T_{stg}$ ................................................. −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | SN54ALS191A | | | SN74ALS191A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 20 | 0 | | 30 | MHz |
| $t_w$ | Pulse duration | CLK high or low | 20 | | | 16.5 | | | ns |
| | | $\overline{LOAD}$ low | 25 | | | 20 | | | |
| $t_{su}$ | Setup time | Data before $\overline{LOAD}\uparrow$ | 25 | | | 20 | | | ns |
| | | $\overline{CTEN}$ before CLK$\uparrow$ | 45 | | | 20 | | | |
| | | D/$\overline{U}$ before CLK$\uparrow$ | 30 | | | 20 | | | |
| | | $\overline{LOAD}$ inactive before CLK$\uparrow$ | 20 | | | 20 | | | |
| $t_h$ | Hold time | Data after $\overline{LOAD}\uparrow$ | 5 | | | 5 | | | ns |
| | | $\overline{CTEN}$ after CLK$\uparrow$ | 0 | | | 0 | | | |
| | | D/$\overline{U}$ after CLK$\uparrow$ | 0 | | | 0 | | | |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS191A | | | SN74ALS191A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC} = 4.5$ V, | $I_I = -18$ mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC} = 4.5$ V to 5.5 V, | $I_{OH} = -0.4$ mA | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | | |
| $V_{OL}$ | | $V_{CC} = 4.5$ V | $I_{OL} = 4$ mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8$ mA | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC} = 5.5$ V, | $V_I = 7$ V | | | 0.2 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC} = 5.5$ V, | $V_I = 2.7$ V | | | 20 | | | 20 | µA |
| $I_{IL}$ | CTEN or CLK | $V_{CC} = 5.5$ V, | $V_I = 0.4$ V | | | −0.2 | | | −0.2 | mA |
| | All others | | | | | −0.2 | | | −0.1 | |
| $I_O$‡ | | $V_{CC} = 5.5$ V, | $V_O = 2.25$ V | −20 | | −112 | −30 | | −112 | mA |
| $I_{CC}$ | | $V_{CC} = 5.5$ V, | All inputs at 0 | | 12 | 22 | | 12 | 22 | mA |

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (OUTPUT) | TO (OUTPUT) | $V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R_L = 500$ Ω, $T_A =$ MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS191A | | SN74ALS191A | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 20 | | 30 | | MHz |
| $t_{PLH}$ | LOAD | Any Q | 7 | 37 | 7 | 30 | ns |
| $t_{PHL}$ | | | 8 | 34 | 8 | 30 | |
| $t_{PLH}$ | A, B, C, D | Any Q | 3 | 25 | 3 | 21 | ns |
| $t_{PHL}$ | | | 4 | 25 | 4 | 21 | |
| $t_{PLH}$ | CLK | RCO | 5 | 24 | 5 | 20 | ns |
| $t_{PHL}$ | | | 5 | 25 | 5 | 20 | |
| $t_{PLH}$ | CLK | Any Q | 3 | 26 | 3 | 18 | ns |
| $t_{PHL}$ | | | 3 | 22 | 3 | 18 | |
| $t_{PLH}$ | CLK | MAX/MIN | 8 | 37 | 8 | 31 | ns |
| $t_{PHL}$ | | | 8 | 34 | 8 | 31 | |
| $t_{PLH}$ | D/$\overline{U}$ | RCO | 8 | 45 | 8 | 37 | ns |
| $t_{PHL}$ | | | 10 | 36 | 10 | 28 | |
| $t_{PLH}$ | D/$\overline{U}$ | MAX/MIN | 8 | 35 | 8 | 25 | ns |
| $t_{PHL}$ | | | 8 | 30 | 8 | 25 | |
| $t_{PLH}$ | CTEN | RCO | 4 | 21 | 4 | 18 | ns |
| $t_{PHL}$ | | | 4 | 23 | 4 | 18 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

**LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT FOR 3-STATE OUTPUTS**

$R_L = R1 = R2$

**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS PULSE DURATIONS**

**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**
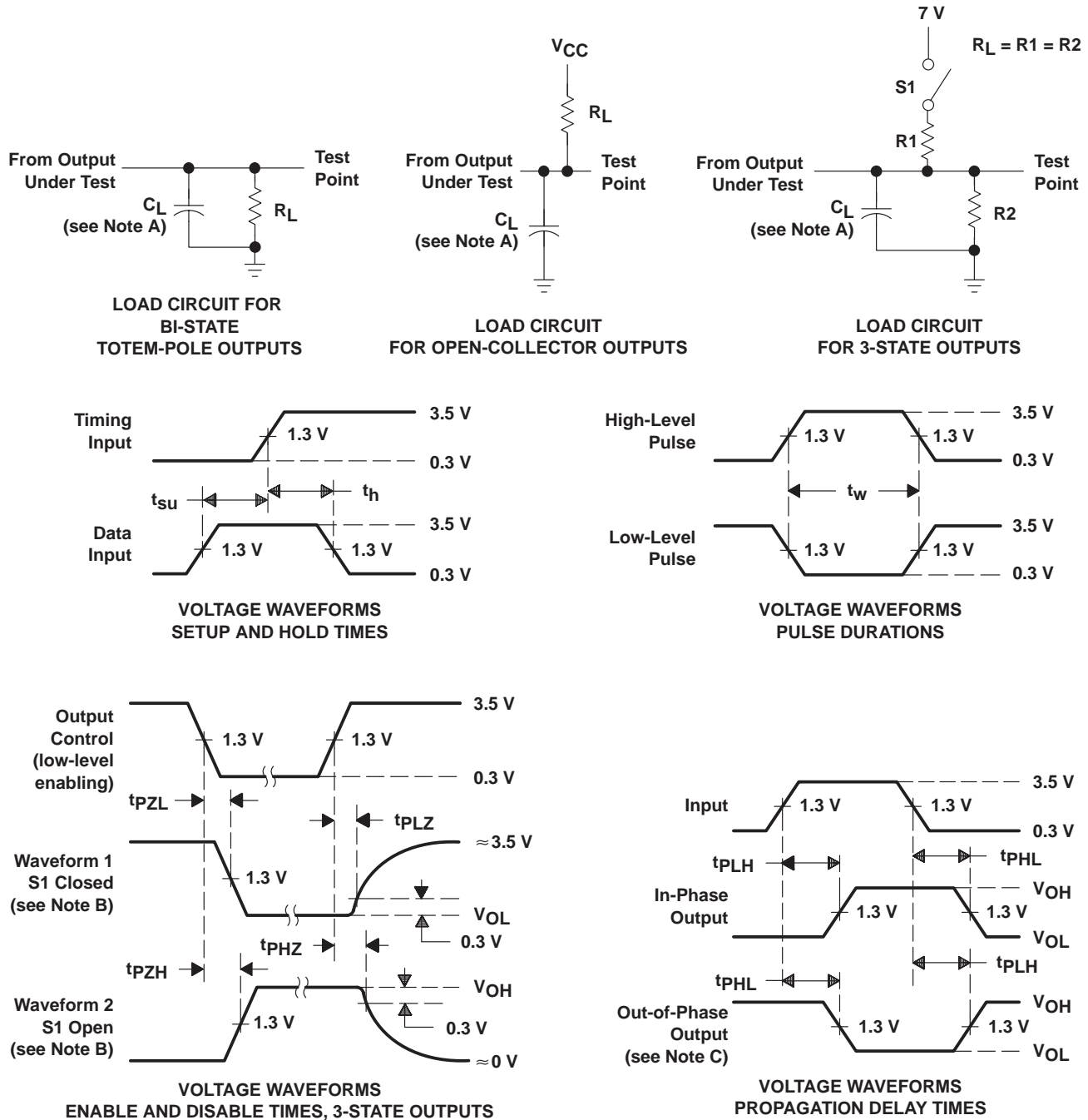
NOTES: A. $C_L$ includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
  D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
  E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable part number (1) | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-86840012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-86840012A SNJ54ALS 191AFK |
| 5962-8684001EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001EA SNJ54ALS191AJ |
| 5962-8684001FA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001FA SNJ54ALS191AW |
| SN74ALS191AD | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | ALS191A |
| SN74ALS191ADR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS191A |
| SN74ALS191ADR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS191A |
| SN74ALS191AN | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS191AN |
| SN74ALS191AN.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS191AN |
| SNJ54ALS191AFK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-86840012A SNJ54ALS 191AFK |
| SNJ54ALS191AFK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-86840012A SNJ54ALS 191AFK |
| SNJ54ALS191AJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001EA SNJ54ALS191AJ |
| SNJ54ALS191AJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001EA SNJ54ALS191AJ |
| SNJ54ALS191AW | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001FA SNJ54ALS191AW |
| SNJ54ALS191AW.A | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8684001FA SNJ54ALS191AW |

(1) **Status:** For more details on status, see our product life cycle.

**(2)** **Material type:**  When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3)** **RoHS values:**  Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4)** **Lead finish/Ball material:**  Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5)** **MSL rating/Peak reflow:**  The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6)** **Part marking:**  There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54ALS191A, SN74ALS191A :**

- Catalog : SN74ALS191A

- Military : SN54ALS191A

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

| Q1 | Q2 | Q1 | Q2 |
| Q3 | Q4 | Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS191ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| SN74ALS191ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

## TUBE



**T - Tube height**

**L - Tube length**

**W - Tube width**

**B - Alignment groove width**

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-86840012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8684001FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74ALS191AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS191AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS191AN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS191AN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS191AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS191AFK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS191AW | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54ALS191AW.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

D (R−PDSO−G16)                                    PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16                          9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1                           8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES:    A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
        ⚠C   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
        ⚠D   Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AC.

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W (R−GDFP−F16)                    CERAMIC DUAL FLATPACK

Base and Seating Plane

$\frac{0.285 \ (7,24)}{0.245 \ (6,22)}$

$\frac{0.045 \ (1,14)}{0.026 \ (0,66)}$

$\frac{0.008 \ (0,20)}{0.004 \ (0,10)}$

$\frac{0.080 \ (2,03)}{0.055 \ (1,40)}$

0.305 (7,75) MAX

1                    16

$\frac{0.019 \ (0,48)}{0.015 \ (0,38)}$

$\frac{0.430 \ (10,92)}{0.370 \ (9,40)}$

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8                    9

$\frac{0.360 \ (9,14)}{0.250 \ (6,35)}$            $\frac{0.360 \ (9,14)}{0.250 \ (6,35)}$

4040180−3/F   04/14

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
        C.  This package can be hermetically sealed with a ceramic lid using glass frit.
        D.  Index point is provided on cap for terminal identification only.
        E.  Falls within MIL STD 1835 GDFP2−F16

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R−GDIP−T**)  
14 LEADS SHOWN

CERAMIC DUAL IN−LINE PACKAGE

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | —— | —— | —— | —— |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14        8

1        7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

## N (R−PDIP−T**)                    PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

| PINS ** DIM | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A   MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A   MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | AA | BB | AC | AD |

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

$\oplus$ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E  12/2002

NOTES:    A.  All linear dimensions are in inches (millimeters).
          B.  This drawing is subject to change without notice.
          C.  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
          D.  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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