

# TCAN1048AV-Q1 Functional Safety FIT Rate, FMD and Pin FMA



## Table of Contents

1 Overview.....	2
2 Functional Safety Failure In Time (FIT) Rates.....	4
3 Failure Mode Distribution (FMD).....	5
4 Pin Failure Mode Analysis (Pin FMA).....	6
5 Revision History.....	9

## List of Figures

Figure 1-1. TCAN1048AV-Q1 Functional Block Diagram.....	3
Figure 4-1. TCAN1048AV-Q1 SOIC Pin Diagram.....	6
Figure 4-2. TCAN1048AV-Q1 VSON Pin Diagram.....	6

## List of Tables

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11.....	4
Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2.....	4
Table 3-1. Die Failure Modes and Distribution.....	5
Table 4-1. TI Classification of Failure Effects.....	6
Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground.....	7
Table 4-3. Pin FMA for Device Pins Open-Circuited.....	7
Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin.....	7
Table 4-5. Pin FMA for Device Pins Short-Circuited to $V_{CC}$ .....	8
Table 4-6. PIN FMA for Device Pins Short-Circuited to $V_{IO}$ .....	8
Table 4-7. Pin FMA for Device Pins Short-Circuited to $V_{BAT}$ .....	9

## Trademarks

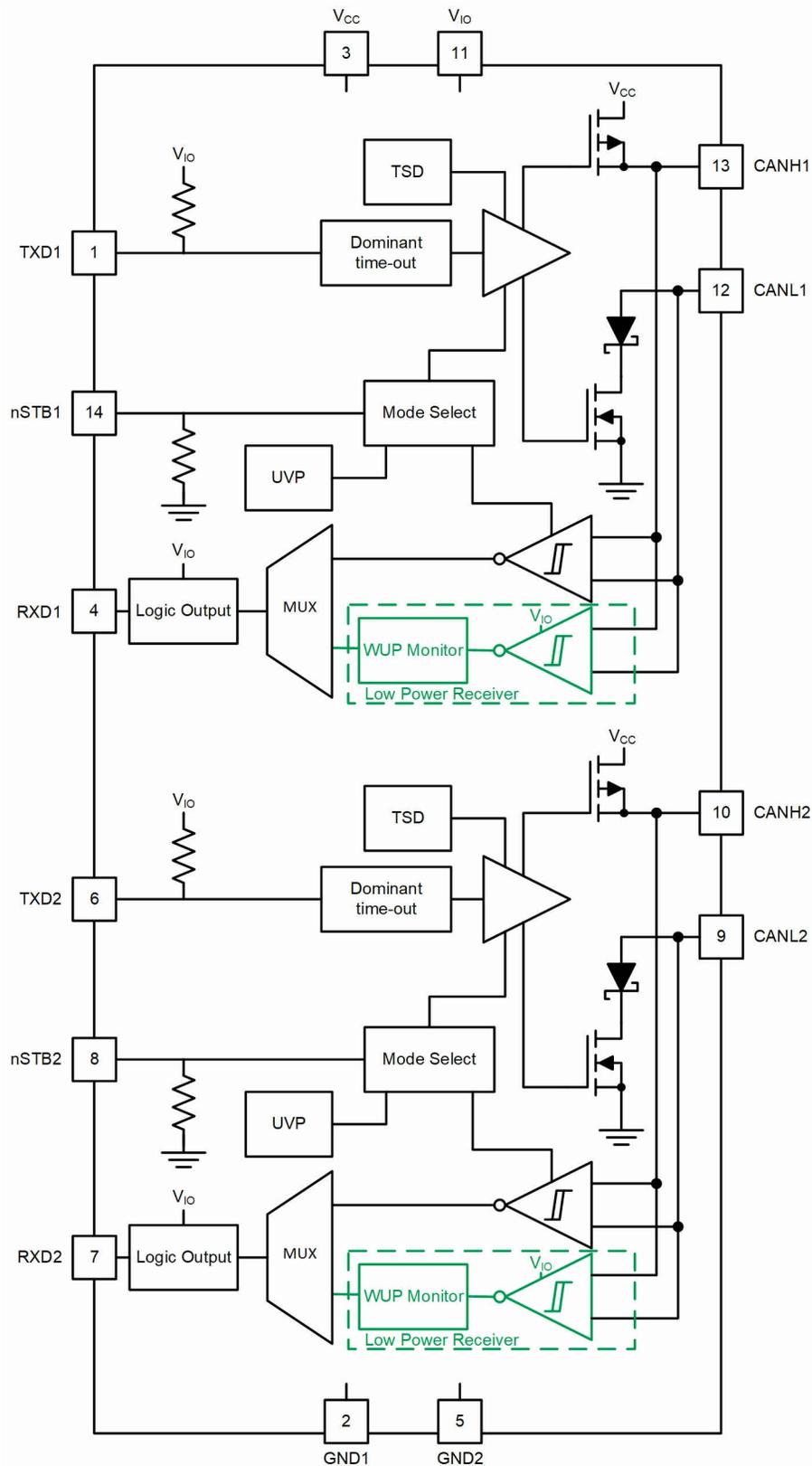
All trademarks are the property of their respective owners.

## 1 Overview

This document contains information for TCAN1048AV-Q1 (VSON package and SOIC package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

[Figure 1-1](#) shows the TCAN1048AV-Q1 functional block diagram for reference.



**Figure 1-1. TCAN1048AV-Q1 Functional Block Diagram**

TCAN1048AV-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

## 2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TCAN1048AV-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 <sup>9</sup> Hours) 14-pin VSON (DMT)	FIT (Failures Per 10 <sup>9</sup> Hours) 14-pin SOIC (D)
Total Component FIT Rate	9	18
Die FIT Rate	3	3
Package FIT Rate	6	15

The failure rate and mission profile information in [Table 2-1](#) comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 250 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

Table	Category	Reference FIT Rate	Reference Virtual T <sub>J</sub>
5	CMOS, BICMOS digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T<sub>J</sub> (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

### 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TCAN1048AV-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

Die Failure Modes	Failure Mode Distribution (%)
Receiver Fail	45%
Transmitter Fail	45%
CANH or CANL driver stuck dominant	5%
Short circuit any two pins	5%

## 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TCAN1048AV-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

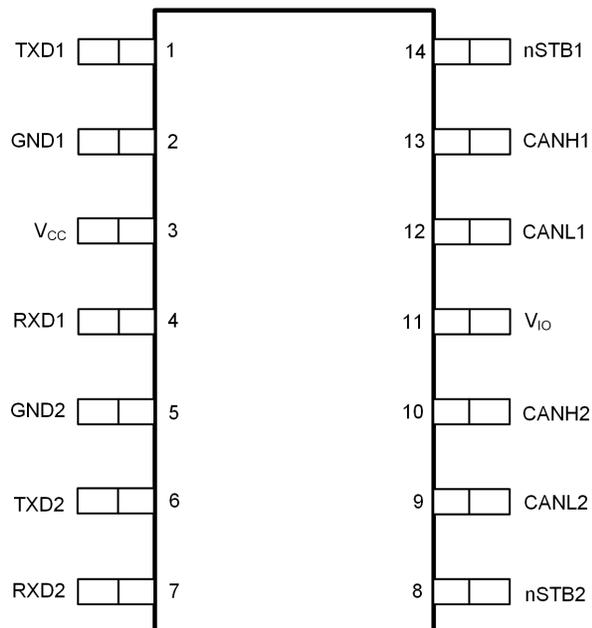
- Pin short-circuited to Ground (see [Table 4-2](#))
- Pin open-circuited (see [Table 4-3](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#))
- Pin short-circuited to  $V_{CC}$  (see [Table 4-5](#))
- Pin short-circuited to  $V_{IO}$  (see [Table 4-6](#))
- Pin short-circuited to  $V_{BAT}$  (see [Table 4-7](#))

[Table 4-2](#) through [Table 4-7](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

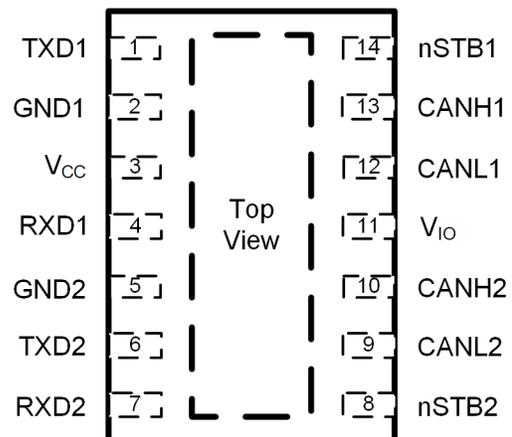
**Table 4-1. TI Classification of Failure Effects**

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

[Figure 4-1](#) shows the TCAN1048AV-Q1 SOIC package pin diagram. [Figure 4-2](#) shows the TCAN1048AV-Q1 VSON package pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TCAN1048AV-Q1 data sheet.



**Figure 4-1. TCAN1048AV-Q1 SOIC Pin Diagram**



**Figure 4-2. TCAN1048AV-Q1 VSON Pin Diagram**

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- $V_{CC} = 4.5$  to  $5.5$  V
- $V_{BAT} = 6$  to  $24$  V
- $V_{IO}$  (if applicable) =  $1.7$  to  $5.5$  V

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	CAN1 enters dominant time out mode. Unable to transmit data to the CAN1 bus.	B
GND1	2	None	D
V <sub>CC</sub>	3	Device unpowered, high I <sub>CC</sub> current.	B
RXD1	4	RXD default is high side FET ON, with pin short to ground, it forms direct path between supply and ground causing high current	A
TXD2	6	CAN2 will enter dominant time out mode. Unable to transmit data to the CAN2 bus.	B
GND2	5	None	D
RXD2	7	RXD default is high side FET ON, with pin short to ground, it forms direct path between supply and ground causing high current	A
CANL2	9	V <sub>O(REC)</sub> spec violated. Degraded EMC performance on CAN2 bus.	C
CANH2	10	Device cannot drive dominant to CAN2 bus, no communication possible.	B
nSTB2	8	nSTB2 stuck low, CAN2 transceiver always in standby mode	B
V <sub>IO</sub>	11	Device will be in protected mode. Transceiver passive on both CAN1 and CAN2 bus.	B
CANL1	12	V <sub>O(REC)</sub> spec violated. Degraded EMC performance on CAN1 bus.	C
CANH1	13	Device cannot drive dominant to CAN1 bus, no communication possible.	B
nSTB1	14	nSTB1 stuck low, CAN1 transceiver always in standby mode.	B
Thermal Pad	-	None	D

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	TXD1 pin defaults high, CAN1 bus state always recessive and unable to transmit data to CAN1 bus.	B
GND1	2	CAN1 unpowered.	B
V <sub>CC</sub>	3	Device unpowered.	B
RXD1	4	No RXD1 output, unable to receive data from CAN1 bus.	B
TXD2	6	TXD2 pin defaults high, CAN2 bus state always recessive and unable to transmit data to CAN2 bus.	B
GND2	5	CAN2 unpowered.	B
RXD2	7	No RXD2 output, unable to receive data from CAN2 bus.	B
CANL2	9	Device cannot drive dominant on CAN2 bus, unable to communicate.	B
CANH2	10	Device cannot drive dominant on CAN2 bus, unable to communicate.	B
nSTB2	8	nSTB2 pin defaults low, CAN2 portion stuck in low-power mode.	B
V <sub>IO</sub>	11	Device will be in protected mode, Transceiver passive on both CAN1 and CAN2 bus.	B
CANL1	12	Device cannot drive dominant on CAN1 bus, unable to communicate.	B
CANH1	13	Device cannot drive dominant on CAN1 bus, unable to communicate.	B
nSTB1	14	nSTB1 pin defaults low, CAN1 portion stuck in low-power mode.	B
Thermal Pad	-	None	D

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	GND1	CAN1 bus will enter dominant time out mode. Unable to transmit data to CAN1 bus.	B
GND1	2	V <sub>CC</sub>	Device unpowered, high I <sub>CC</sub> current.	B
V <sub>CC</sub>	3	RXD1	RXD1 output stuck high, unable to receive data from CAN1 bus.	B

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)**

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	4	GND2	RXD default is high side FET ON, with pin short to ground, it forms direct path between supply and ground causing high current	A
GND2	5	TXD2	CAN2 bus will enter dominant time out mode. Unable to transmit data to CAN2 bus.	B
TXD2	6	RXD2	RXD2 output reflects the input to TXD2, and while this is the same transceiver, due to loop delay, the communication will be corrupted. Information from CAN2 bus will not be received correctly.	B
nSTB2	8	CANL2	CAN2 driver and receiver turn off when a dominant is driven. May not enter normal mode.	B
CANL2	9	CANH2	CAN2 bus stuck recessive, no communication possible. I <sub>OS</sub> current may be reached.	B
CANH2	10	V <sub>IO</sub>	CAN2 bus stuck dominant, no communication possible.	B
V <sub>IO</sub>	11	CANL1	CAN1 bus stuck recessive, no communication possible. I <sub>OS</sub> current may be reached on CANL1.	B
CANL1	12	CANH1	CAN1 bus stuck recessive, no communication possible I <sub>OS</sub> current may be reached.	B
CANH1	13	nSTB1	CAN1 driver and receiver may turn off when the CAN1 bus is recessive. May not enter normal mode.	B

**Note**

The VSON package includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

**Table 4-5. Pin FMA for Device Pins Short-Circuited to V<sub>CC</sub>**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	TXD1 pin stuck high, unable to transmit data to CAN1 bus.	B
GND1	2	CAN1 transceiver unpowered, high I <sub>CC</sub> current.	B
V <sub>CC</sub>	3	None	D
RXD1	4	RXD1 pin stuck high, unable to receive data from CAN1 bus.	B
TXD2	6	TXD2 pin stuck high, unable to transmit data to CAN2 bus.	B
GND2	5	CAN2 transceiver unpowered, high I <sub>CC</sub> current.	B
RXD2	7	RXD2 pin stuck high, unable to receive data for CAN2 bus.	B
CANL2	9	CAN2 bus always recessive, no communication possible. I <sub>OS</sub> current may be reached.	B
CANH2	10	V <sub>O(REC)</sub> spec violated, degraded EMC performance on CAN2 bus.	C
nSTB2	8	nSTB2 stuck high, CAN2 transceiver unable to enter low power mode	B
V <sub>IO</sub>	11	IO pins will operate as 5V input/output. Microcontroller may be damaged if V <sub>CC</sub> > V <sub>IO</sub> .	C
CANL1	12	CAN1 bus always recessive, no communication possible. I <sub>OS</sub> current may be reached.	B
CANH1	13	V <sub>O(REC)</sub> spec violated, degraded EMC performance on CAN1 bus.	C
nSTB1	14	nSTB1 stuck high, CAN1 transceiver unable to enter low power mode	B

**Table 4-6. PIN FMA for Device Pins Short-Circuited to V<sub>IO</sub>**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	TXD1 stuck high, unable to transmit data to CAN1 bus.	B
GND1	2	CAN1 unpowered, high I <sub>IO</sub> current.	B
V <sub>CC</sub>	3	IO pins will operate as 5V input/output. Microcontroller may be damaged if V <sub>CC</sub> > V <sub>IO</sub> .	C

**Table 4-6. PIN FMA for Device Pins Short-Circuited to  $V_{IO}$  (continued)**

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
RXD1	4	RXD1 pin stuck high, unable to receive data from CAN1 bus.	B
GND2	5	CAN2 unpowered, high $I_{IO}$ current.	B
TXD2	6	TXD2 stuck high, unable to transmit data to CAN2 bus.	B
RXD2	7	RXD2 pin stuck high, unable to receive data from CAN2 bus.	B
nSTB2	8	nSTB2 stuck high, CAN2 transceiver unable to enter low power mode.	B
CANL2	9	CAN2 bus always recessive, no communication possible. $I_{OS}$ current may be reached if $V_{IO} \geq 3.3V$ .	B
CANH2	10	$V_{O(REC)}$ spec violated if $V_{IO} \geq 3.3V$ , degraded EMC performance on CAN2 bus.	C
$V_{IO}$	11	None	D
CANL1	12	CAN1 bus always recessive, no communication possible. $I_{OS}$ current may be reached if $V_{IO} \geq 3.3V$ .	B
CANH1	13	$V_{O(REC)}$ spec violated if $V_{IO} \geq 3.3V$ , degraded EMC performance on CAN1 bus.	C
nSTB1	14	nSTB1 stuck high, CAN1 transceiver unable to enter low power mode.	B

**Table 4-7. Pin FMA for Device Pins Short-Circuited to  $V_{BAT}$** 

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
TXD1	1	Absolute maximum violation, transceiver may be damaged. Unable to transmit data to CAN1 bus.	A
GND1	2	Device unpowered, high $I_{BAT}$ current.	B
$V_{CC}$	3	Absolute maximum violation, transceiver may be damaged. CAN bus may be unable to communicate.	A
RXD1	4	Absolute maximum violation, transceiver may be damaged. Unable to receive data from CAN1 bus.	A
TXD2	6	Absolute maximum violation, transceiver may be damaged. Unable to transmit data to CAN2 bus.	A
GND2	5	Device unpowered, high $I_{BAT}$ current.	B
RXD2	7	Absolute maximum violation, transceiver may be damaged. Unable to receive data from CAN2 bus.	B
CANL2	9	CAN2 bus always recessive, no communication possible. $I_{OS}$ current may be reached.	B
CANH2	10	$V_{O(REC)}$ spec violated, degraded EMC performance on CAN2 bus.	C
nSTB2	8	Absolute maximum violation, transceiver may be damaged. CAN2 transceiver stuck in standby mode.	A
$V_{IO}$	11	Absolute maximum violation, transceiver may be damaged.	A
CANL1	12	CAN1 bus always recessive, no communication possible. $I_{OS}$ current may be reached.	B
CANH1	13	$V_{O(REC)}$ spec violated, degraded EMC performance on CAN1 bus.	B
nSTB1	14	Absolute maximum violation, transceiver may be damaged. CAN1 transceiver stuck in standby mode.	A

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2021	*	Initial Release

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated