Functional Safety Information

CDCE913-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for CDCE913-Q1 (TSSOP-14 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

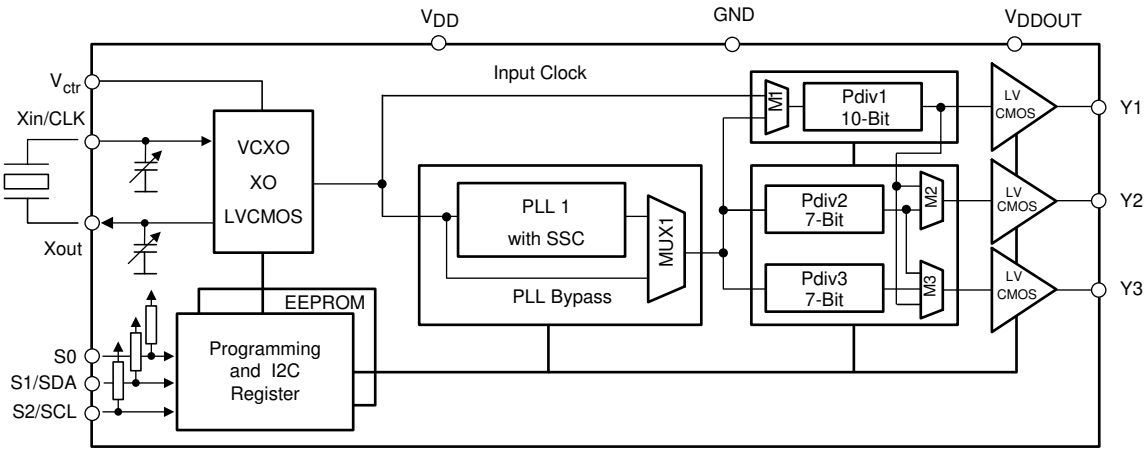

Figure 1-1. Functional Block Diagram

CDCE913-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for CDCE913-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	11
Die FIT Rate	3
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed ≤ 50V supply	60 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for CDCE913-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Performance degradation of output clocks	45%
Incorrect output frequencies, poor timing accuracy	40%
Part in undefined state due to incorrect startup/power-on reset	10%
Loss of I2C communication	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the CDCE913-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the CDCE913-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the CDCE913-Q1 data sheet.

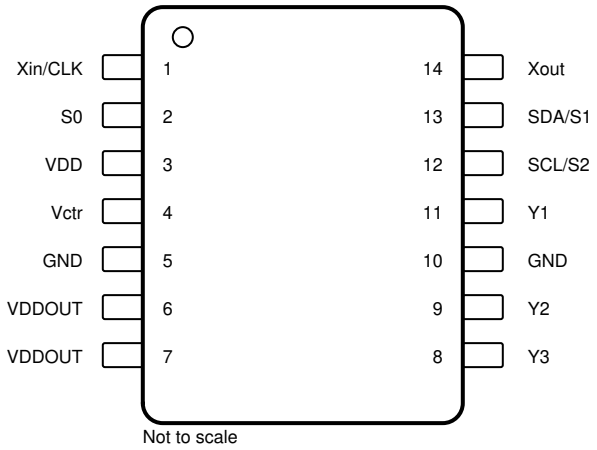

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Output frequencies set to 27 MHz, 54 MHz and 108 MHz.
- 27 MHz Crystal is used as input.
- VCTR pin is connected to an programmable analog voltage from a microcontroller.
- PLL1 is configured to 108 MHz.
- VDD is connected to a 1.8-V supply.
- VDDOUT is connected to a 3.3-V supply.
- S0 is driven high from a microcontroller.
- S1 and S2 are connected to a I2C controller.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Xin/CLK	1	Xin pin pulled low. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	B
S0	2	S0 pulled low. Outputs disabled.	B
VDD	3	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCTR	4	Crystal input frequency pulled to lowest frequency possible. Output frequencies pulled by the same relative offset. Loss of frequency control.	B/C
GND	5	No effect. Normal operation.	D
VDDOUT	6	Outputs not functional.	B
VDDOUT	7	Outputs not functional.	B
Y3	8	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Y2	9	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
GND	10	No effect. Normal operation.	D
Y1	11	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
S2/SCL	12	SCL stuck low. Loss of I2C communication.	B
S1/SDA	13	SDA stuck low. Loss of I2C communication.	B
Xout	14	Xout pin pulled low. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Xin/CLK	1	Xin pin open. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	C
S0	2	S0 pulled high. Outputs enabled. Normal operation.	D
VDD	3	Device unpowered. Device not functional.	B
VCTR	4	VCTR state undetermined. Noise on pin can effect output frequency accuracy and performance.	C
GND	5	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
VDDOUT	6	Device outputs unpowered. Outputs not functional.	B
VDDOUT	7	Device outputs unpowered. Outputs not functional.	B
Y3	8	No output.	B
Y2	9	No output.	B
GND	10	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
Y1	11	No output.	B
S2/SCL	12	SCL stuck high. Loss of I2C communication.	B
S1/SDA	13	SDA stuck high. Loss of I2C communication.	B
Xout	14	Xout pin open. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
Xin/CLK	1	S0	Xin pin pulled high. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	B
S0	2	VDD	S0 pulled high. Outputs enabled. Normal operation.	D
VDD	3	VCTR	Crystal input frequency pulled to highest frequency possible. Output frequencies pulled by the same relative offset. Loss of frequency control.	B/C
VCTR	4	GND	Crystal input frequency pulled to lowest frequency possible. Output frequencies pulled by the same relative offset. Loss of frequency control.	B/C
GND	5	VDDOUT	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VDDOUT	6	VDDOUT	No effect. Normal operation.	D
VDDOUT	7	Y3	Not considered. Corner pin.	D
Y3	8	Y2	No or distorted output clock.	B
Y2	9	GND	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
GND	10	Y1	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Y1	11	S2/SCL	Output pulled low. No output clock. I2C communication corrupted. Loss of I2C communication.	B
S2/SCL	12	S1/SDA	I2C communication corrupted. Loss of I2C communication.	B
S1/SDA	13	Xout	Xout pin pulled high with I2C bus pullups. Crystal oscillation stops. PLL does not lock. Incorrect output frequency. I2C communication corrupted. Loss of I2C communication.	B/C
Xout	14	Xin/CLK	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
Xin/CLK	1	Xin pin pulled high. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	B
S0	2	Outputs enabled.	D
VDD	3	No effect. Normal operation.	D
VCTR	4	Crystal input frequency pulled to highest frequency possible. Output frequencies pulled by the same relative offset. Loss of frequency control.	B/C
GND	5	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
VDDOUT	6	Supply voltage not in recommended operating range. Output swing lower. Output performance degraded. VDD may be pulled to VDDOUT and device damage may be plausible.	A
VDDOUT	7	Supply voltage not in recommended operating range. Output swing lower. Output performance degraded. VDD may be pulled to VDDOUT and device damage may be plausible.	A
Y3	8	Output pulled to VDD. No output clock.	B
Y2	9	Output pulled to VDD. No output clock.	B
GND	10	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
Y1	11	Output pulled high. No output clock.	B
S2/SCL	12	SCL stuck high. Loss of I2C communication.	B
S1/SDA	13	SDA stuck high. Loss of I2C communication.	B
Xout	14	Xout pin pulled high. Crystal oscillation stops. PLL does not lock. Incorrect output frequency.	B

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