1394b OHCI-Lynx Controller

FEATURES

- **Single 3.3-V supply (1.8-V internal core voltage with regulator)**
- **3.3-V and 5-V PCI signaling environments**
- **Serial bus data rates of 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s**
- **Physical write posting of up to three outstanding transactions**
- **Serial ROM or boot ROM interface supports 2-wire serial EEPROM devices**
- **33-MHz/64-bit and 33-MHz/32-bit selectable PCI interface**
- **Multifunction terminal (MFUNC terminal 1):**
  - **$\overline{\text{PCI\_CLKRUN}}$ protocol per the *PCI Mobile Design Guide***
  - **General-purpose I/O**
  - **CYCLEIN/CYCLEOUT for external cycle timer control for customized synchronization**
- **PCI burst transfers and deep FIFOs to tolerate large host latency:**
  - **Transmit FIFO—5K asynchronous**
  - **Transmit FIFO—2K isochronous**
  - **Receive FIFO—2K asynchronous**
  - **Receive FIFO—2K isochronous**
- **D0, D1, D2, and D3 power states and $\overline{\text{PME}}$ events per the *PCI Bus Power Management Interface Specification***
- **Programmable asynchronous transmit threshold**
- **Isochronous receive dual-buffer mode**
- **Out-of-order pipelining for asynchronous transmit requests**
- **Register access fail interrupt when the PHY SYSCLK is not active**
- **Initial bandwidth available and initial channels available registers**
- **Digital video and audio performance enhancements**
- **Fabricated in advanced low-power CMOS process**
- **Packaged in 144-terminal LQFP (PGE) or 176-ball MicroStar BGA (GGW)**

DESCRIPTION

The TSB82AA2 OHCI-Lynx is a discrete 1394b link-layer device, which has been designed to meet the demanding requirements of today's 1394 bus designs. The TSB82AA2 device is capable of exceptional 800M bits/s performance; thus, providing the throughput and bandwidth to move data efficiently and quickly between the PCI and 1394 buses. The TSB82AA2 device also provides outstanding ultra-low power operation and intelligent power management capabilities. The device provides the IEEE 1394 link function and is compatible with 100M bits/s, 200M bits/s, 400M bits/s, and 800M bits/s serial bus data rates.

The TSB82AA2 improved throughput and increased bandwidth make it ideal for today's high-end PCs and open the door for the development of S800 RAID- and SAN-based peripherals.

The TSB82AA2 OHCI-Lynx operates as the interface between a 33-MHz/64-bit or 33-MHz/32-bit PCI local bus and a compatible 1394b PHY-layer device (such as the TSB81BA3 device) that is capable of supporting serial data rates at 98.304M, 196.608M, 393.216M, or 786.432M bits/s (referred to as S100, S200, S400, or S800 speeds, respectively). When acting as a PCI bus master, the TSB82AA2 device is capable of multiple cacheline bursts of data, which can transfer at 264M bytes/s for 64-bit transfers or 132M bytes/s for 32-bit transfers after connecting to the memory controller.

Due to the high throughput potential of the TSB82AA2 device, it possible to encounter large PCI and legacy 1394 bus latencies, which can cause the 1394 data to be overrun. To overcome this potential problem, the TSB82AA2 implements deep transmit and receive FIFOs to buffer the 1394 data, thus preventing possible problems due to bus latency. This also ensures that the device can transmit and receive sustained maximum size isochronous or asynchronous data payloads at S800.

The TSB82AA2 device implements other performance enhancements to improve overall performance of the device, such as: a highly tuned physical data path for enhanced SBP-2 performance, physical post writing buffers, multiple isochronous contexts, and advanced internal arbitration.

The TSB82AA2 device also implements hardware enhancements to better support digital video (DV) and MPEG data stream reception and transmission. These enhancements are enabled through the isochronous receive digital video enhancements register at TI extension offset A80h. These enhancements include automatic time stamp insertion for transmitted DV and MPEG-formatted streams and common isochronous packet (CIP) header stripping for received DV streams.

The CIP format is defined by the IEC 61883-1:1998 specification. The enhancements to the isochronous data contexts are implemented as hardware support for the synchronization timestamp for both DV and audio/video CIP formats. The TSB82AA2 device supports modification of the synchronization timestamp field to ensure that the value inserted via software is not stale—that is, less than the current cycle timer when the packet is transmitted.

The TSB82AA2 performance and enhanced throughput make it an excellent choice for today's 1394 PC market; however, the portable, mobile, and even today's desktop PCs power management schemes continue to require devices to use less and less power, and Texas Instrument's 1394 OHCI-Lynx product line has continued to raise the bar by providing the lowest power 1394 link-layers in the industry. The TSB82AA2 device represents the next evolution of Texas Instruments commitment to meet the challenge of power-sensitive applications. The TSB82AA2 device has ultra-low operational power requirements and intelligent power management capabilities that allow it to autonomously conserve power based on the device usage.

One of the key elements for reducing the TSB82AA2 operational power requirements is Texas Instrument's advanced CMOS process and the implementation of an internal 1.8-V core, which is supplied by an improved integrated 3.3-V to 1.8-V voltage regulator. The TSB82AA2 device implements a next generation voltage regulator which is more efficient than its predecessors, thus providing an overall reduction in the device's operational power requirements especially when operating in $D3_{cold}$ using auxiliary power. In fact, the TSB82AA2 device fully supports D0, D1, D2, and $D3_{hot/cold}$ power states as specified in the *PC 2001 Design Guide* requirements and the *PCI Power Management Specification*. PME wake event support is subject to operating system support and implementation.

As required by the *1394 Open Host Controller Interface Specification* (OHCI) and IEEE Std 1394a–2000, internal control registers are memory-mapped and nonprefetchable. The PCI configuration header is accessed through configuration cycles as specified by the *PCI Local Bus Specification*, and provides plug-and-play (PnP) compatibility. Furthermore, the TSB82AA2 device is fully compliant with the latest *PCI Local Bus Specification*, *PCI Bus Power Management Interface Specification*, IEEE Draft Std 1394b, IEEE Std 1394a–2000, and *1394 Open Host Controller Interface Specification*.

NOTE:

This product is for high-volume PC applications only. For a complete datasheet or more information contact support@ti.com.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB82AA2PGE	Obsolete	Production	LQFP (PGE) | 144	-	-	Call TI	Call TI	0 to 70	TSB82AA2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TSB82AA2 :

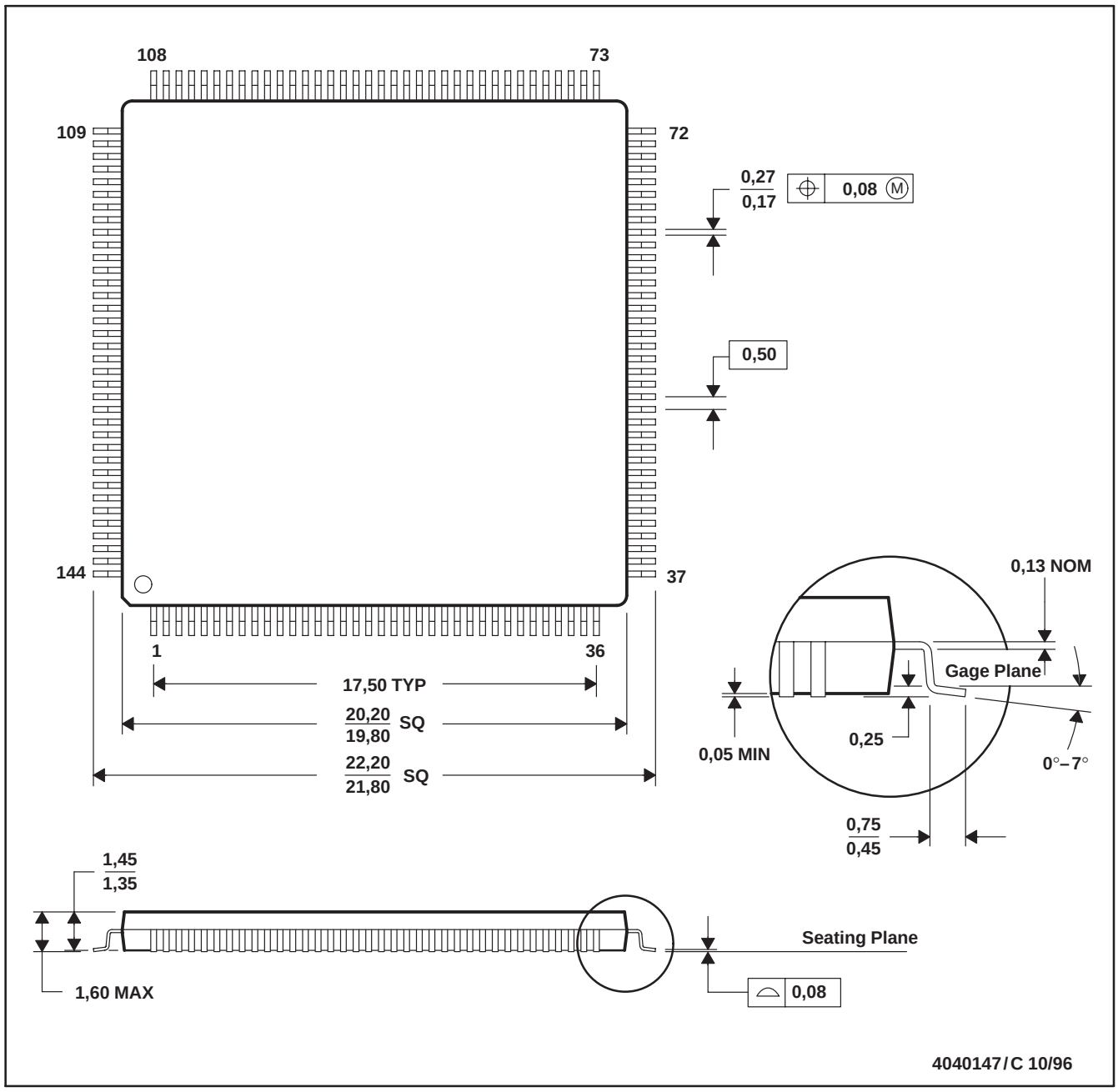
- Enhanced Product : TSB82AA2-EP

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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