TI Mobile and Embedded Sandy Bridge CPU Power Solution

Mobile and Embedded Sandy Bridge Platform Power Solutions

Includes 5V/3.3V Integrated FET Options



Intel Mobile/Embedded Sandy Bridge PWR Solution

CPU + GPU core controller
CPU + GPU core MOSFET Driver
2012 GPU
CPU/GPU NexFET Power Block
System
CPU and PCH PLL
PCH and ME Core
PCH and ME Core
PCH and ME Core (AMT)
System Agent (SA)
DDR3 Core and Termination

TPS51640 1-Phase/1-Phase TPS51601 for GPU TPS51640 2-Phase CSD86350Q5D TPS51123/25A TPS53312 TPS51219/51513 TPS53312 TPS51217/51461 TPS59116/216 TPS51640 2-phase/1-Phase TPS51601 for GPU TPS51640 2-phase CSD86350Q5D TPS51123/25A TPS53312 TPS51219/51513 TPS53312 TPS51217/51461 TPS59116/216

IMVP7

SV 35W

Quad Core 45W

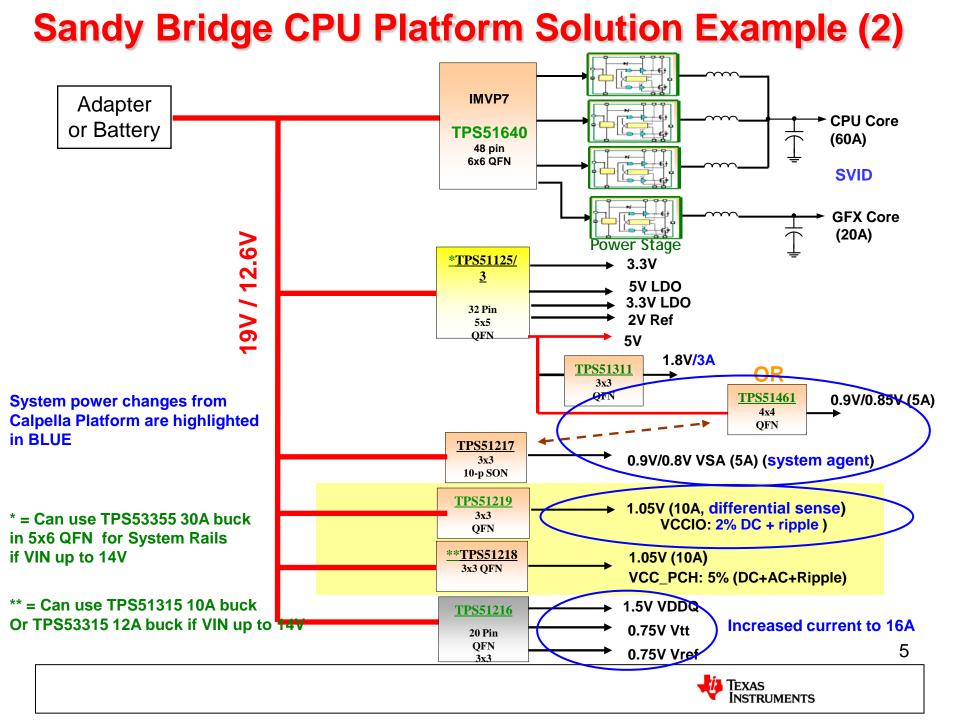
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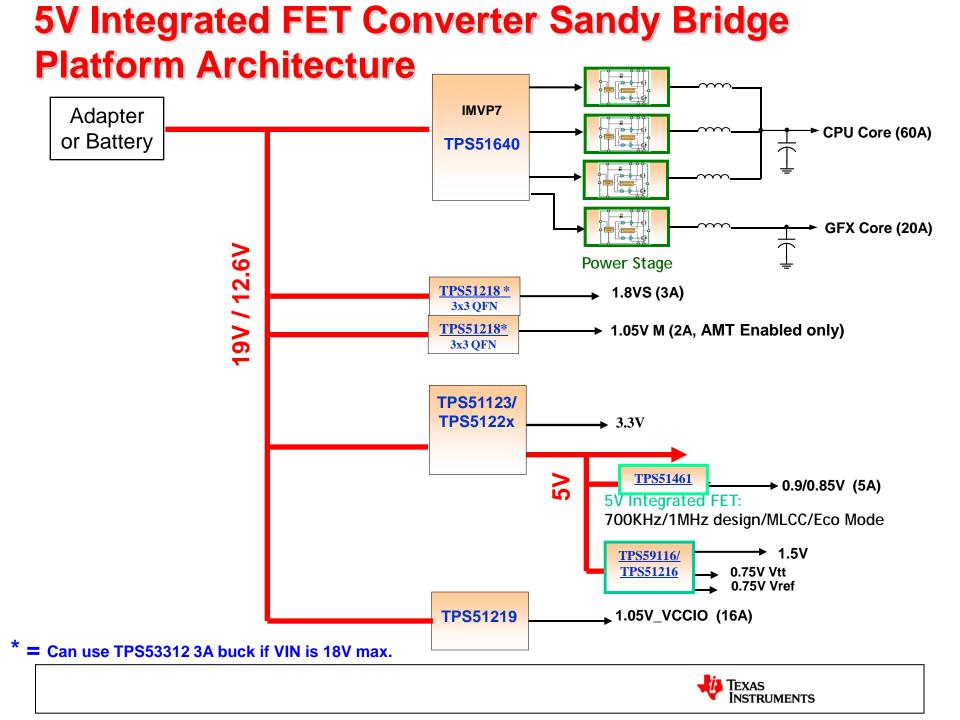
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TPS51640 3-phase/1-Phase TPS51601 for CPU/GPU TPS51640 2-Phase CSD86350Q5D TPS51123/25A TPS53312 TPS51219/51513 TPS53312 TPS51217/51461 TPS59116/216

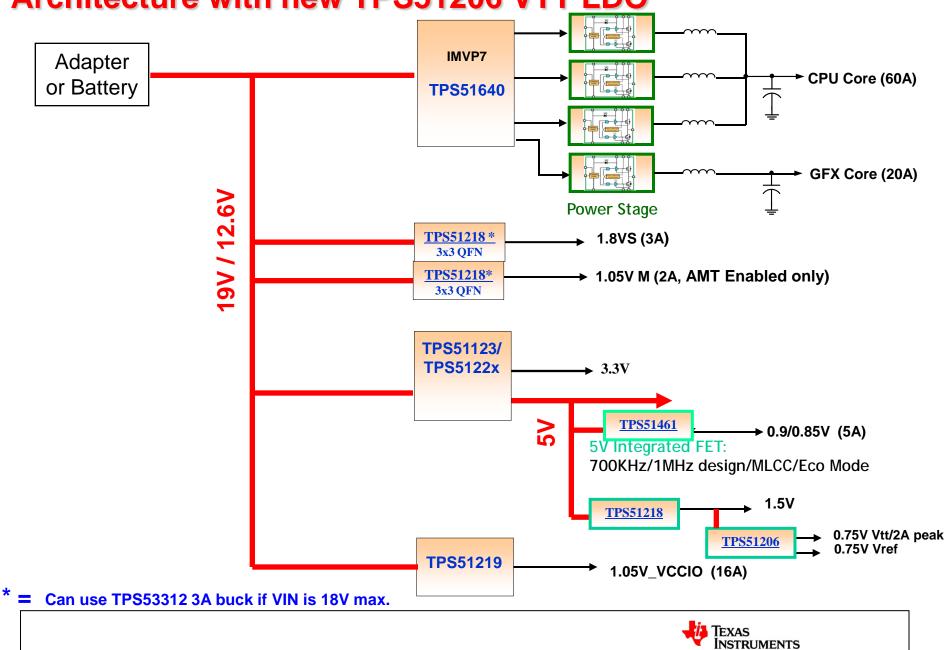


Sandy Bridge CPU Platform Solution Example (1) **IMVP7** Adapter **CPU Core TPS51640** (60A) 48 pin **BO24725** 6x6 QFN 3.5x3.5 **SVID OFN GFX Core** Batterv (20A) 19V / 12.6V **Power Stage** * TPS51125/3 3.3V **5V LDO** 32 Pin **3.3V LDO** 5x5 2V Ref **OFN 5V** 1.8V/3A **TPS53311 OR 3x3 System power changes from **TPS51461** 0.9V/0.8V (5A) Calpella Platform are highlighted 4x4 in **BLUE OFN TPS51217** 0.9V/0.8V VSA (5A) (system agent) 10-p SON * = Can use TPS53355 30A buck **TPS51219** 1.05V (20A, differential sense) in 5x6 QFN for System Rails **QFN** VCCIO: 2% DC+ripple, VCC PCH: 5% if VIN up to 14V **1.5V VDDQ TPS51216 Increased current to 16A** 20 Pin 0.75V Vtt ** = Can use TPS53312 3A **QFN** buck if VIN is >5V 0.75V Vref 3x3 **TPS51217** Discrete GFX (1 or 2 bit VID) 4 3x3SON **TEXAS** Instruments





5V Integrated FET Converter Sandy Bridge Platform Architecture with new TPS51206 VTT LDO



Sandy Bridge TPS51640 + TPS51219 + TPS51216 POWER EVM **Main Power** Switch (On/Off) 30V TI NexFETs **Connections** for CSD17xxx electronic loads OCL, FSW, **CPU Core** OSR jumpers GND 7 **TPS51640** CPU/GPU **TPS51219** controller **VCCIO/PCH GPU** controller **CORE Intel SVID Sandy Bridge GUI** input **CPU** socket and 5V jumper to 12 Texas Instruments **TPS51216 DDR3** use 5V from core controller **USB** with integrated



Vtt LDO

Sandy Bridge TPS51640 + TPS51219 + TPS51216 Power EVM with CSD86350Q5D Power Blocks **Main Power** Switch (On/Off) CSD86350Q5D **Connections 5x6 Power Blocks** for electronid loads OCL, FSW, **CPU** OSR Core jumpers **TPS51640 TPS51219 GPU** VCCIO CORE **Intel SVID** Sandy **GUI** input **Bridge CPU** and 5V socket jumper to **TPS51216** use 5V DDR3 core from USB and Vtt ia Texas INSTRUMENTS

Sandy Bridge CPU Power System Reference Designs available

1 / 26A peak

1 / 33A peak

0 - No GPU used

CSD17303Q5

CSD86350Q5D

CSD86350Q5D

CSD17302Q5A x1 CSD17303Q5 x2 for

CPU/GPU

CSD17302Q5A x1

CSD17303Q5 x1 for DDR3

core and PCH core

CSD17302Q5A

CSD17303Q5

CSD96370Q5M power stage

x 4

CSD86350Q5D for CPU

phases 1-2, CSD96370Q5M

for CPU phase 3, GPU

CSD17302Q5A

CSD17303Q5

TEXAS

INSTRUMENTS

TPS51601 x2

TPS51640

TPS51601

TPS51640 TPS51601 x2

(2" x 2" PCB area)

TPS51640

TPS51601 x2

TPS51219

TPS51216

TPS51640

TPS51640

TPS51640

TPS51640

Carray Briage of o revier cyclem reference Beergine available						
Reference Design	CPU Phases/CPU Current	GPU Phases/GPU Current	Power Train per phase	TI PWM / Drivers		
3+1 CPU/GPU core	3 / 94A peak	1 / 33A peak	CSD86350Q5D	TPS51640 TPS51601 x		
3 + 1 CPU/GPU core	3 / 66A peak	1 / 26A peak	CSD17302Q5A	TPS51640		

2 / 50A peak

3 / 94A peak

3 / 94A peak

2 / 53A peak

3 / 94A peak

3 / 94A peak

2 / 53A peak

2 + 1 CPU/GPU core

3 + 1 CPU/GPU core

PR989E2 IMVP7 power

system EVM

2 + 1 CPU/GPU core

3 + 1 CPU/GPU core

3 + 1 CPU/GPU core

2 + 0 CPU/GPU core

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