

BQ77905 Design Considerations in High-Current Applications

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ABSTRACT

The BQ77905 is a 3-5S low-power protector for lithium-ion batteries that controls the charge and discharge FETs for current control. In some cases, the charge and discharge current path is required to handle a continuous high-current that causes heat and component problems. This document provides an example of the BQ77905 with a 50-A current path for charge and discharge. The design considerations presented in this document help designers build a high-current charge and discharge path with the BQ77905.

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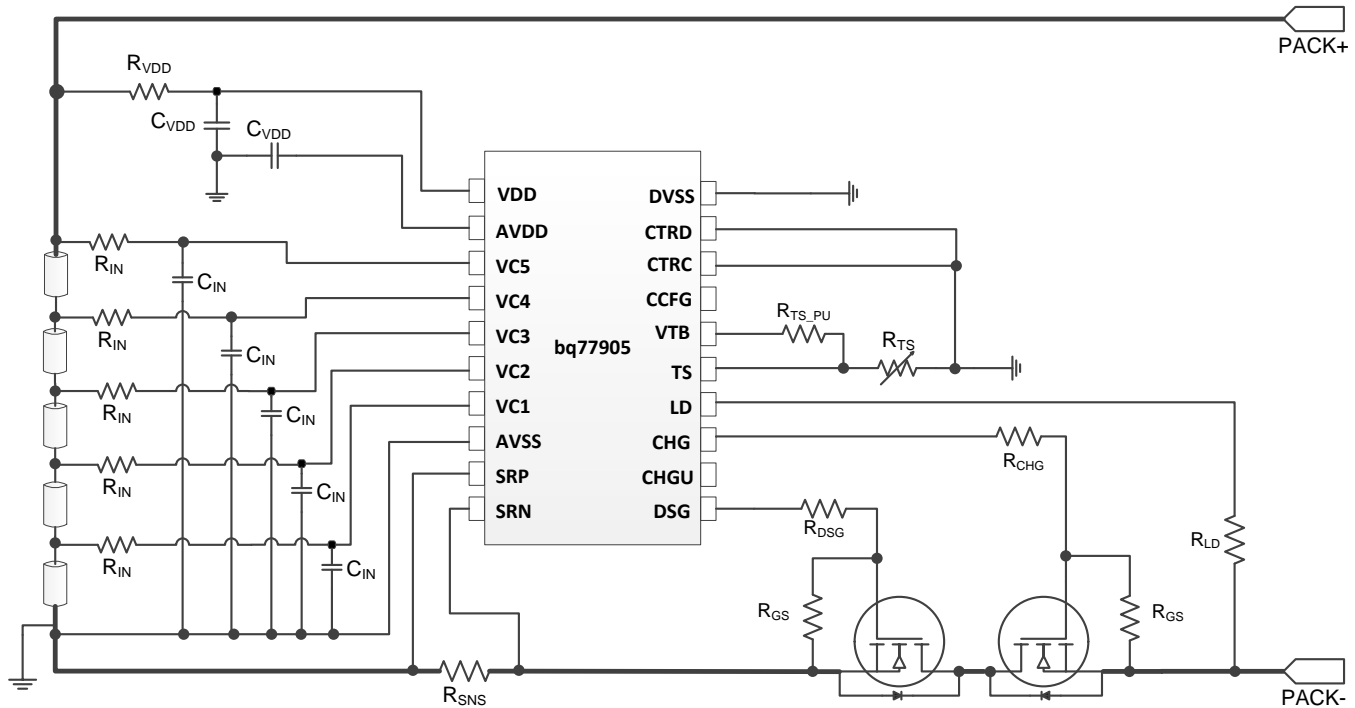
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1 Introduction

The BQ77905 is a 3-5S low-power protector that provides voltage, current, and temperature protection without a microcontroller (MCU) control. The BQ77905 is an easy-to-use protector that can handle high-power systems, such as power tools, while consuming low power. When designing a battery system with a 50-A charge and discharge path, power dissipation and sizing of the sense resistor are issues. Due to these issues TI recommends several strong design considerations regarding the layout and component selection.

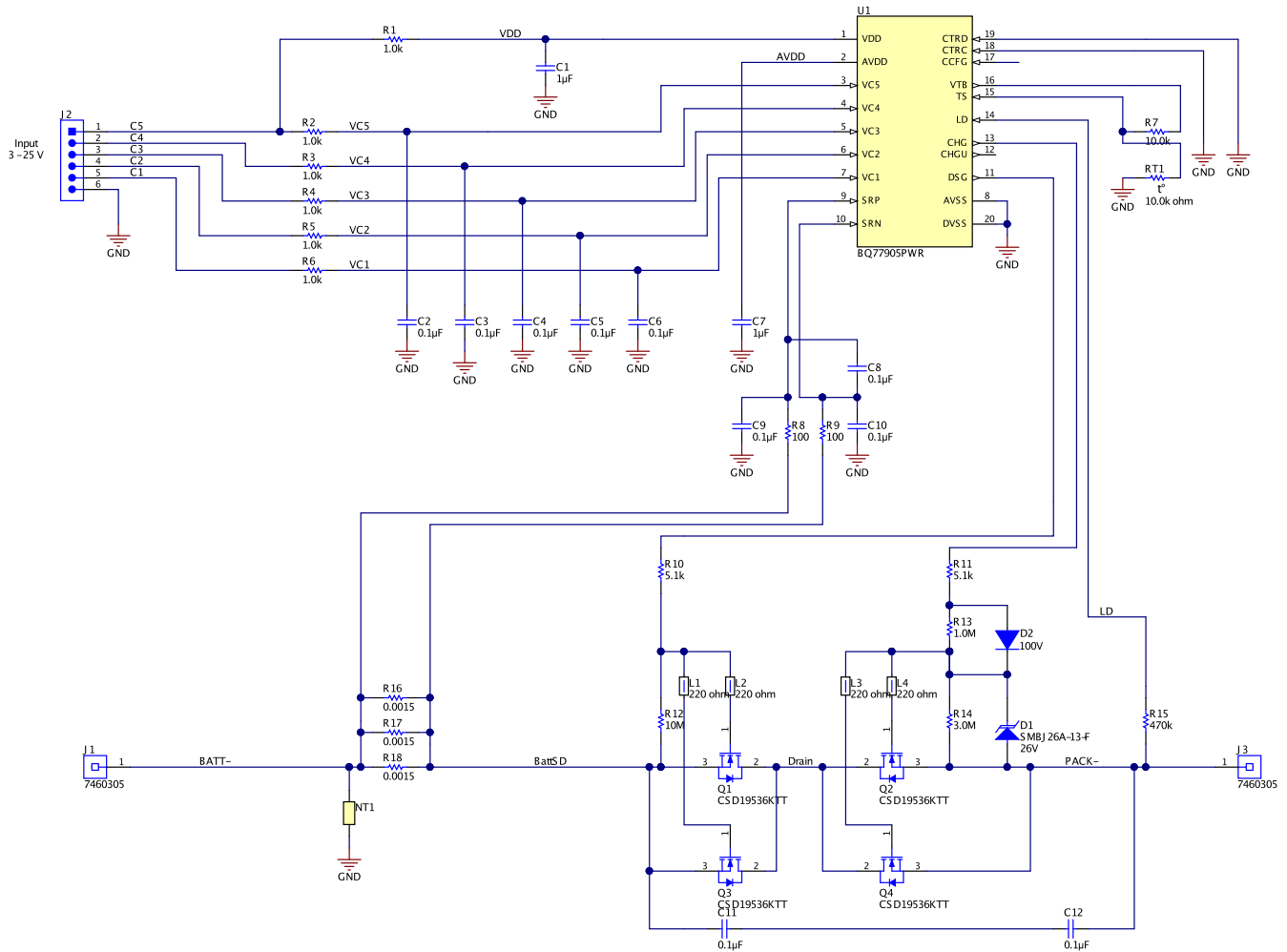


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Figure 1. Common Implementation

2 High-Current Path

When working with a high-current path it is very important to control the temperature along the charge and discharge trace to prevent physical malfunction of the board. Examples of physical malfunctions that can occur are delamination of the traces and footprint, as well as component damage. To improve the thermal performance of the board, several layout guidelines help reduce heat concentration. An example of these guidelines is the implementation of battery protection using the BQ77905, shown in Figure 2, and the layout of the BQ77905, shown in Figure 3, which can handle 50-A of continuous current.



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Figure 2. BQ77905 High-Current Schematic

The high-current path in this board is from PACK- to BATT-. This path consists of the CHG and DSG FETs Q1, Q2, Q3, Q4, and the current sense resistors R_{SNS} . In this path, it is important to increase the area that the current travels. The more area the current gets to travel through, the less resistance there is in the path. In this layout, the current path consists of wide traces (> 600-mil wide) using two layers of 1 oz copper. Figure 4 shows the heat concentration on this board during a test that consisted of running a continuous 50-A current for 2 minutes during normal bq77905 operation. With the heat spread across the top and bottom layers, the highest recorded heat value was 76°C at the source pin Q3, depicted by the arrow in Figure 4. This high-heat concentration occurs due to the amount of current entering the board from Q3, because of uneven distribution of current across the DSG FETs Q1 and Q3. By comparing the layout of Q2 and Q4 with Q1 and Q3 for high-current applications, the layout symmetry of Q2 and Q4 from PACK- to the DRAIN net is beneficial. Q2 and Q4 have no overlap in their current paths while the current for Q1 must pass through Q3, causing the uneven distribution in current and resulting in an increase in temperature at Q3. This occurrence is visible in Figure 4 due to Q4 having a higher temperature and also the temperature on the heat sink over Q4.

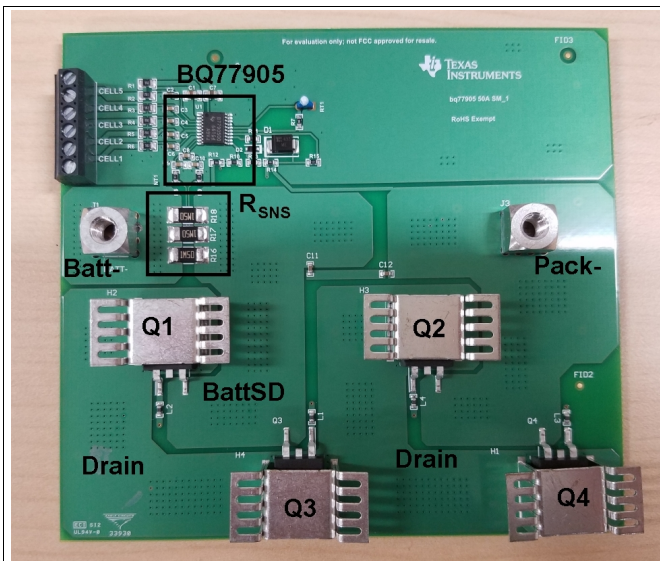


Figure 3. Layout of the BQ77905 High-Current Schematic

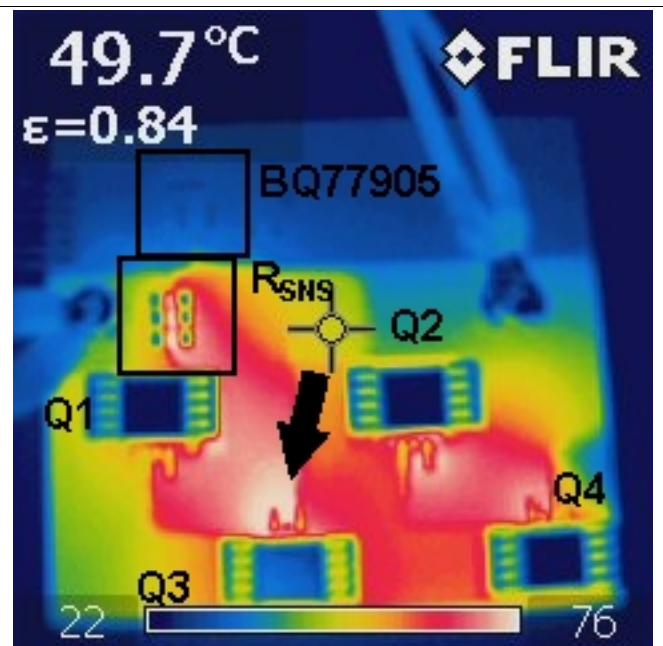
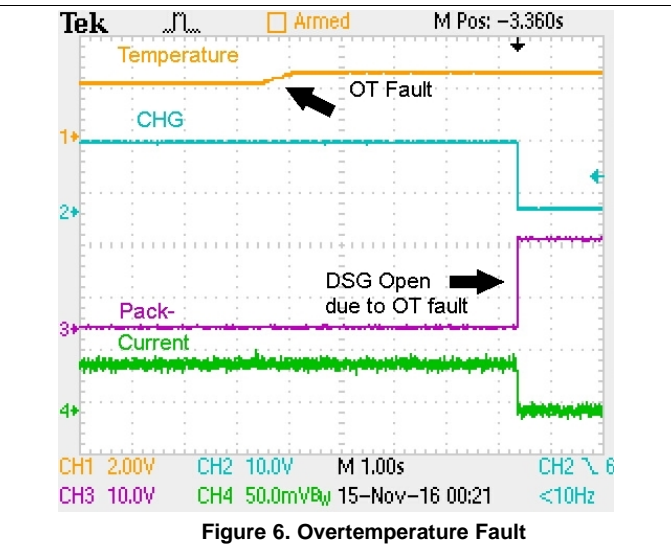
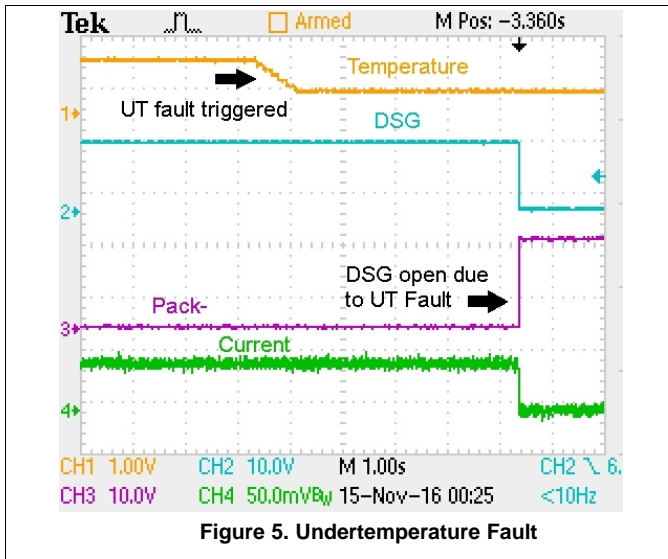


Figure 4. Thermal Image After Two Minutes With a 50-A Current

For more space-constrained layouts, the width of the traces can be reduced by using thicker copper layers. In this example board, 1-oz copper was used to create visible heat distinction, but TI recommends using a minimum of 2-oz copper. The design uses CSD19536KTT FETs, which are surface mount FETs (TO-263 package) that take advantage of the wider traces due to the exposed drain on the backside of the package, but also dissipate heat into the board, therefore heat sinks are used to draw heat away from the board surface. More about FET packages is discussed in [Section 4](#).

Due to the high temperature under the continuous high current, it may be necessary to add an additional temperature sensor around the FETs for switching if the FETs ever reach their thermal limits. [Figure 5](#) shows BQ77905 protecting the battery for undertemperature (UT) conditions and [Figure 6](#) shows battery protection for overtemperature (OT) conditions.



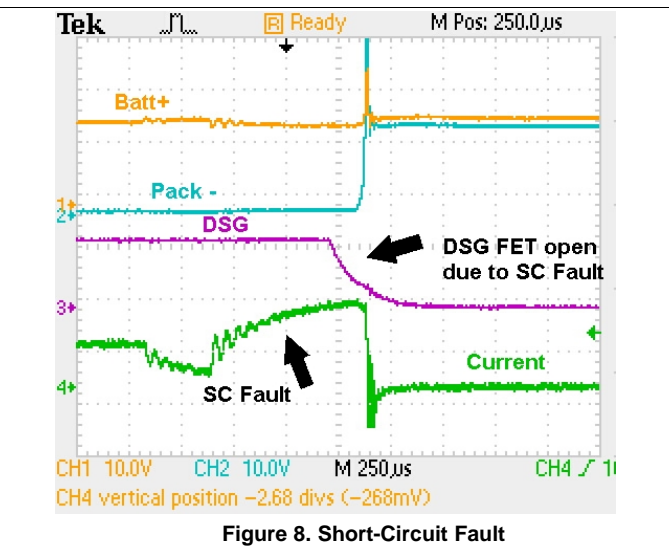
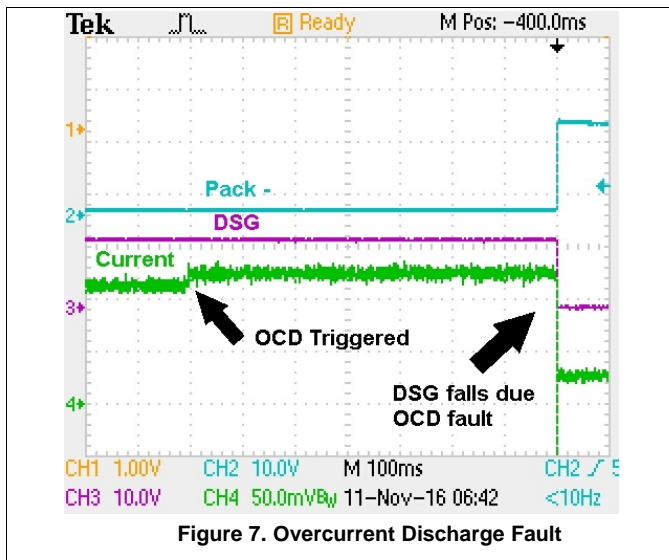
3 Current Sense

When working with a 50-A current path, is it necessary to adjust the R_{SNS} resistor for accurate overcurrent discharge (OCD) fault and short circuit discharge (SCD) fault handling. In the bq77905 the R_{SNS} is adjusted based on the factory programmed device configuration and the OCD thresholds desired (see Equation 1). In this design, the desired value of the OCD is 60 A, and the programmed OCD threshold is 30 mV, therefore the calculated value of R_{SNS} is 0.5 m Ω (see Equation 2). The same calculation was performed for the SC threshold.

$$R_{SNS} = \frac{OCD1\ Threshold\ (V)}{I_{OCD}(A)} \tag{1}$$

$$R_{SNS} = \frac{0.03\ mV}{60\ A} = 0.5\ m\Omega \tag{2}$$

While this value can be realized by a single-sense resistor, TI recommends using several resistors in parallel so the path across the R_{SNS} is larger, to accommodate the high current. Figure 3 shows an example of this because the resistors R16, R17, and R18 are in parallel with a large package size to ensure that the current is split across three paths and the current has more area when it converges on each resistor. Figure 7 and Figure 8 show the BQ77905 performing as expected over the OCD and SC faults. The temperature across R_{SNS} resistors is very high, as seen in Figure 4, even with resistors in parallel due to the amount of current that has concentrated across the junction points. In some applications it may be more beneficial to add more resistors in parallel than the three that were used here. When using a multiple layer trace on both sides of the board, it is important to add resistors to both sides so all the current does not have to rush onto a single side.



4 FET Selection

The protection FETs disable current flow in the event of charge or discharge faults. When choosing FETs for a design at this current level it is necessary to consider the voltage, current, and thermal handling from the package.

The voltage capability of the FETs must meet the requirement of the total battery voltage and any voltage transients. A conservative value is double the battery voltage. For this application, 20 V is the reference voltage and therefore the FETs need a V_{DS} minimum of 40-V as a requirement.

The current going through the FET and the $R_{DS(on)}$ largely determines the power consumed by the FET. When choosing a FET, it is desirable to have the lowest possible $R_{DS(on)}$ available, but at times this conflicts with the physical characteristics of the FET. In Figure 9 the $R_{DS(on)}$ limits the amount of current in low V_{DS} states. For example, a CSD19536KTT being driven by the BQ77905 has a minimum V_{GS} of 10 V which lowers the $R_{DS(on)}$ of the FET to 3.5 m Ω .

$$V_{DS} = I_{DS} * R_{DS(on)} = 50A * 3.5m\Omega = 175mV \tag{3}$$

Passing 50 A through a CSD19536KTT causes the V_{DS} to be 175 mV, which results in a value above the $R_{DS(on)}$ limit line as denoted by the black dot in Figure 9. Due to physics, the FET adapts to this situation and moves to the nearest point on the right, following the 50-A line denoted by the blue dot, which results in a higher V_{DS} than expected. This increase in V_{DS} means the FET is running inefficiently, more heat is dissipated into the board, and there is a larger voltage drop across the FETs, which is undesirable.

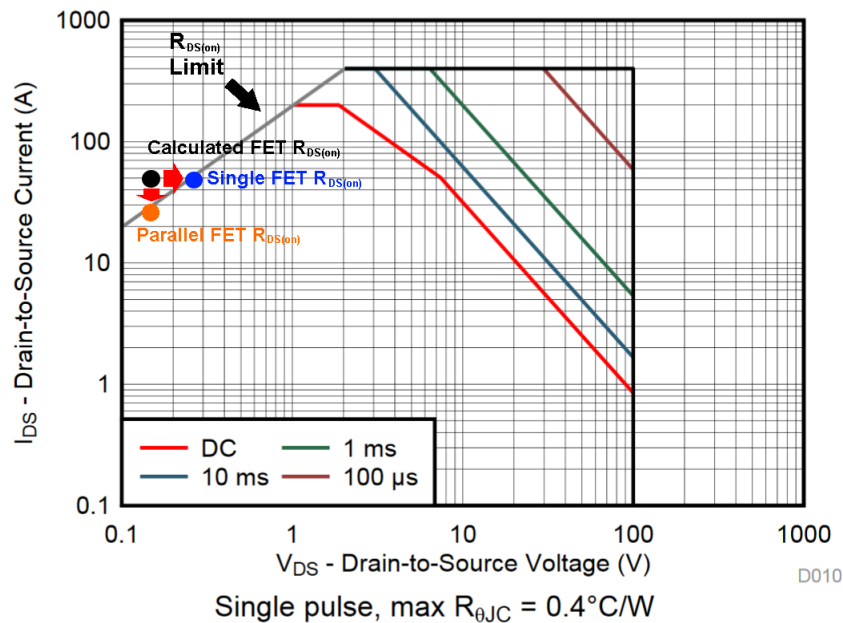


Figure 9. SOA Curve for CDS19536KTT

To lower the current through the FETs, this design uses two FETs in parallel for the charge and discharge gate functions. This layout lowers the current going into each FET by half and brings the current back below the $R_{DS(on)}$ line into the SOA safe region for each individual FET, as denoted by the orange dot. This effectively makes each FET consume half the power over a larger area. It is important to remember that when using FETs in parallel the capacitance increases and this effects the charge and discharge rate of the FET.

Figure 10 and Figure 11 show the BQ77905 reacting to overvoltage (OV) and undervoltage (UV) faults using parallel FETs.

Packaging also impacts thermal performance of the board. For example, in Figure 3 the board uses CDS19536KTT FETs with heat sinks attached to the board to dissipate heat. The CDS19536KTT FETs are SMT which dissipate heat into the board as the drain of the CDS19536KTT is soldered onto the board. If the FET has a low $R_{DS(ON)}$, the voltage drop across the FET is minimized, which results in less heat transferred into the PCB, but by using a different package the heat can be directly dissipated out of the FET. For example, the CSD18536KCS FET uses a TO-220 package that exposes the drain of the FET to air which allows it to be directly connection to a heat sink. The benefit of this FET package is that heat bypasses the board and directly dissipates into the air due to the larger surface area. Having a heat sink directly connected to the CSD18536KCS helps reduce heat in the PCB more than the SMT alternative at the cost of an increased height requirement.

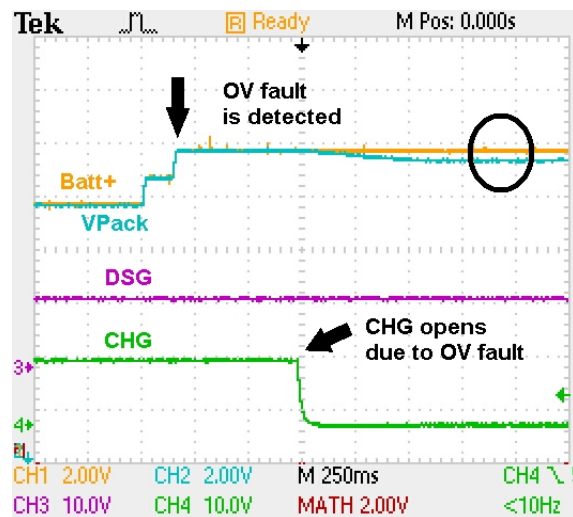


Figure 10. Overvoltage Fault

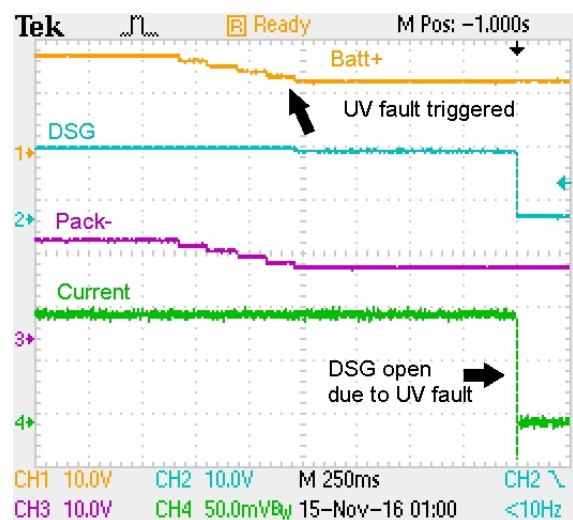


Figure 11. Undervoltage Fault

5 References

For additional information, refer to the following documents, available at www.ti.com.

- *BQ77904 / BQ77905: 3-5S Low Power Protector* , Data Sheet ([SLUSCM3](#))
- *BQ77905 EVM User's Guide* ([SLVUAN2](#))
- *BQ77905 Using Multiple FETs* , Application Report ([SLUA773](#))
- *AN-558 Introduction to Power MOSFETs and Their Applications*, Application Note ([SNVA008](#))
- *CSD19536KTT 100-V N-Channel NexFET™ Power MOSFET*, Data Sheet ([SLPS540](#))

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