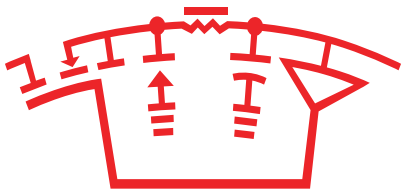

Power Supply Design Seminar

Creating a Primary-Side Regulation Flyback Converter Using a Conventional Boost Controller

Texas Instruments

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Topic 6
Jiri Panacek
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Primary-side regulation (PSR) eliminates the need for optocoupler-based feedback by sensing the voltage across the primary or auxiliary winding, an approach that reduces system costs and enhances reliability. Flyback controllers featuring integrated advanced feedback circuitry specifically designed for primary-side sensing are broadly available, but it is also possible to achieve PSR-type feedback using standard boost controllers. Despite its apparent simplicity, this implementation has its own caveats. This topic explains these caveats and identifies areas where trade-offs become necessary, including a design example.

Flyback Converters

Flyback converters are popular solutions for low-cost isolated DC/DC converters. The topology uses only one switch that controls the current flow through the primary winding.

Figure 1 is a simplified circuit diagram of a flyback converter. **Figure 2** shows selected waveforms for the flyback converter operating in discontinuous conduction mode (DCM). The operating cycle breaks down into two phases: turnon and turnoff.

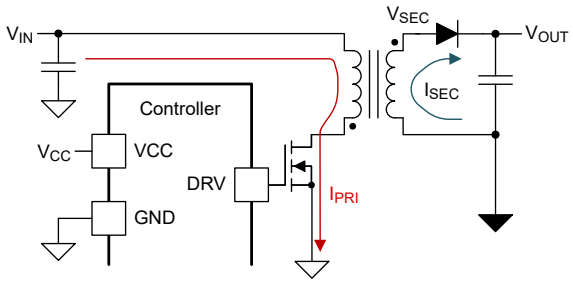


Figure 1. *Simplified flyback converter.*

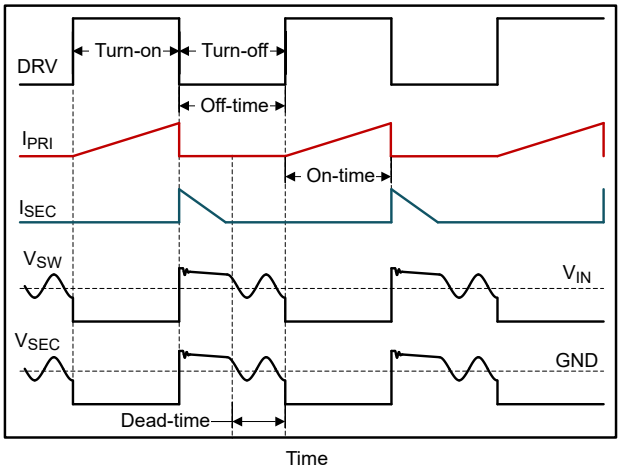


Figure 2. *Flyback converter waveforms.*

During turnon, the switch conducts. The current (I_{PRI}) through the primary winding rises linearly. A diode on the secondary side is reverse-polarized and blocks the secondary winding current (I_{SEC}). Only the output capacitor energizes the load. This phase stores energy in the coupled inductor (transformer).

During turnoff, the switch opens and I_{PRI} drops to zero. The energy that the coupled inductor accumulated during the turnon phase causes the secondary winding to change the polarity. With the polarity change, the secondary-side diode conducts. The current I_{SEC} linearly decreases and demagnetizes the inductor. This current recharges the output capacitor and supplies the load.

The dead-time interval starts when the inductor becomes completely demagnetized and I_{SEC} drops to zero. During this interval, resonant ringing between the primary inductance and output capacitance of the switch occurs. This is characteristic for flyback converters operating in DCM. The ringing is visible across all windings.

By carefully balancing the turnon and turnoff durations, the converter maintains the output voltage (V_{OUT}) within the regulated levels. Flyback converters and controllers typically sense I_{PRI} and V_{OUT} to maintain regulation with quick transient response. Sensing I_{PRI} is simple. The controller is on the primary side and the information does not need to cross the isolation barrier. Sensing V_{OUT} is more challenging because the information must cross the isolation barrier. There are two possible techniques to address this challenge: secondary-side regulation (SSR) and PSR (see **Figure 3**).

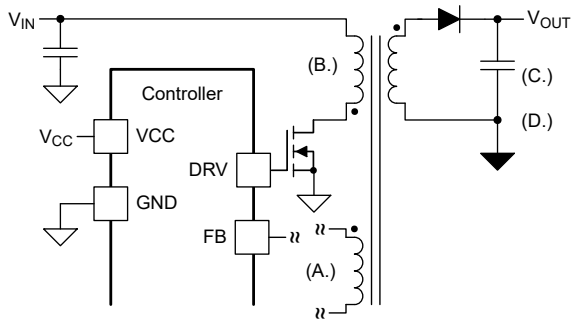


Figure 3. *Flyback voltage feedback locations.*

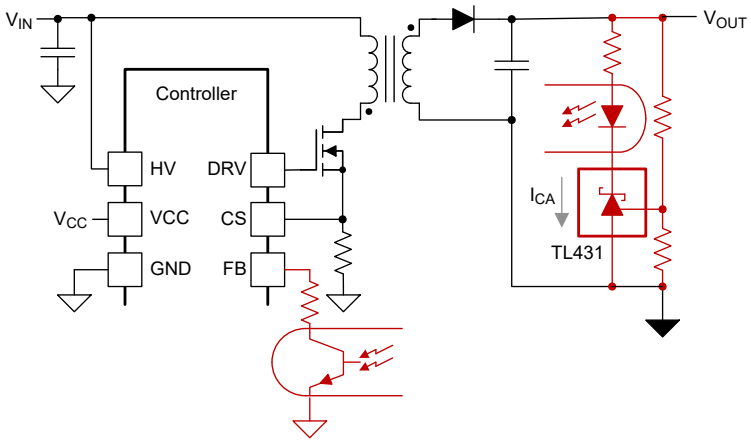
SSR measures V_{OUT} directly on the output of the DC/DC converter (C and D in **Figure 3**). In converters, where galvanic isolation is not a concern (for example, in DC/DC converters with a high voltage output), a simple resistor divider scales V_{OUT} down to match the feedback (FB) pin input voltage range. In most applications, however, galvanic isolation is important. In this case, SSR uses an analog isolator (an optocoupler) that transfers information across the isolation barrier.

PSR measures V_{OUT} indirectly by sensing the reflected voltage on the primary winding during the turnoff phase. This method uses either an additional auxiliary winding (A in **Figure 3**) or measures the switch-node voltage (V_{SW}) on the switch node (B in **Figure 3**).

SSR

Figure 4 shows a simplified circuit diagram of a flyback converter with SSR. The feedback network uses a resistor divider, shunt voltage reference and optocoupler. The voltage reference (a TL431 or similar device) compares V_{OUT} against its internal voltage reference and adjusts the cathode-anode current (I_{CA}) accordingly. The optocoupler transistor current is proportional to the current transfer ratio (CTR).

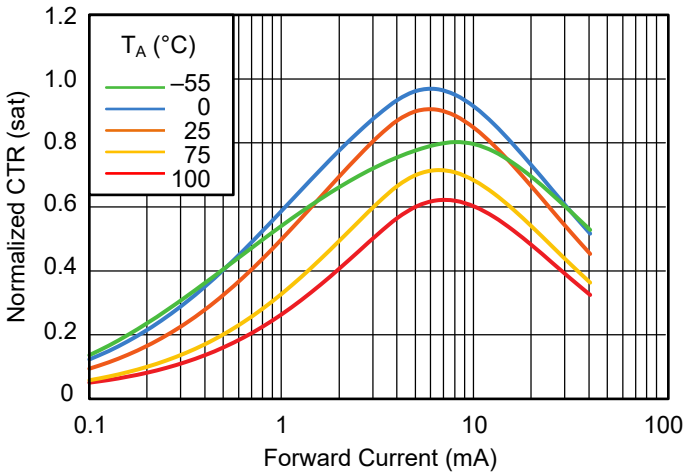
The flyback controller relies on the voltage reference that indirectly reports if V_{OUT} is less or more than intended. In reality, this circuit requires additional passive components for proper compensation in order to ensure the stability of the control loop.



Feedback network simplified.

Figure 4. *Flyback converter with SSR using an optocoupler.*

The CTR of a common optocoupler is highly nonlinear and depends on several factors. **Figure 5** shows how the CTR varies with temperature and forward current. Additionally, the CTR exhibits degradation over time. A reliable flyback converter design has to accommodate the worst-case scenario, including the product lifetime and operating temperature.



Source: Vishay, Application Note 45 V_{CE} = 0.4 V

Normalized to:

I_F = 5 mA V_{CE} = 5 V T_A = 25°C

Figure 5. *CTR vs. forward current and temperature.*

PSR

Figure 6 is a simplified schematic of a PSR flyback. In this example, the controller senses V_{OUT} indirectly by sensing the auxiliary winding. The auxiliary winding shares the ground reference with the controller. The winding polarity is the same as the secondary winding.

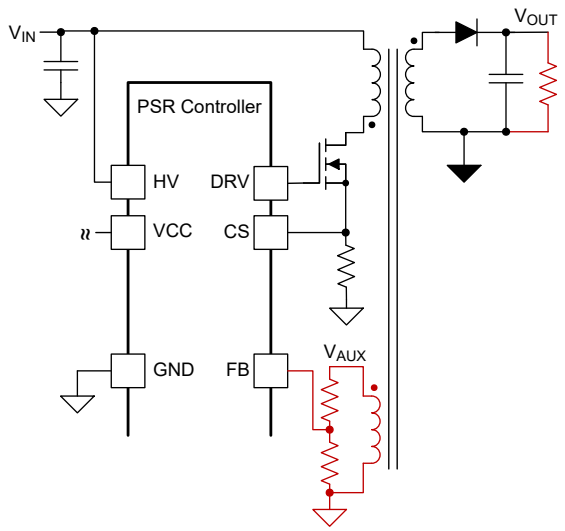


Figure 6. *Flyback converter with PSR using an auxiliary winding.*

Figure 7 shows PSR flyback waveforms. The waveform present on the auxiliary winding is important. During the turnon phase, the auxiliary voltage (V_{AUX}) is negative and corresponds to V_{IN} scaled by the turns ratio between the primary and auxiliary windings.

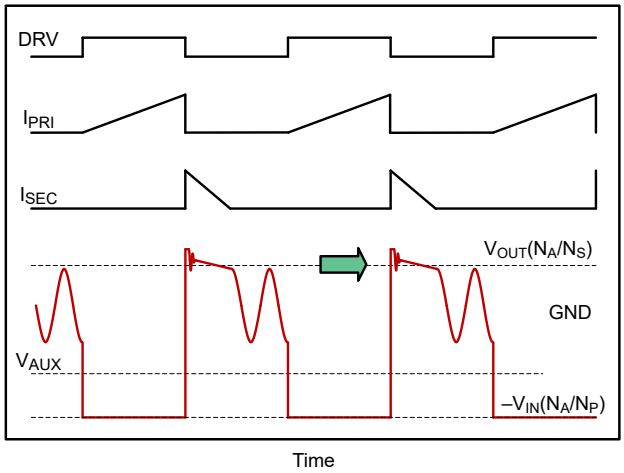


Figure 7. *PSR flyback waveforms.*

During the turnoff phase, and before the dead time, V_{AUX} is positive. The amplitude corresponds to V_{OUT} scaled by the turns ratio between the secondary and auxiliary windings. The controller measures V_{OUT} once per switching cycle by sampling V_{AUX} when the dead time starts. Continuous switching of PSR flybacks is crucial, as it ensures that V_{AUX} accurately represents the output.

Table 1 compares SSR and PSR.

Parameter	SSR with an optocoupler	PSR
Light-load behavior	Good light-load regulation	Requires minimal load
Feedback	Complex feedback network using a TL431 regulator and optocoupler	Sampled reflected V_{OUT}
Initial V_{OUT} accuracy	Excellent	Average
Load regulation	Very good load regulation (<1%)	Average load regulation (>1%)
Reliability	Optocoupler aging affects reliability	Excellent
Transient response	Limited by optocoupler bandwidth	Mostly limited by the switching frequency (f_{SW})
Cost	Average	Improved because of the optocoupler removal
Self-biasing	Requires auxiliary winding	Leverages auxiliary winding for both the bias and feedback

Table 1. *SSR vs. PSR.*

Detailed Look at the Auxiliary Winding Waveforms

Figure 8 shows PSR flyback feedback, including additional parameters that affect the shape of the auxiliary winding waveform. As I noted earlier, the turnon phase is not important for the regulation because the auxiliary winding does not carry any useful information during this phase. As soon as the converter enters the turnoff phase, V_{AUX} suddenly changes polarity.

The parasitic leakage inductance of the coupled inductor causes high-frequency ringing. After damping the ringing, the V_{AUX} waveform enters the phase when it remains nearly constant. In reality, the voltage slightly decreases over time. The forward voltage of the diode (V_F) and the equivalent series resistance of the secondary winding (R_S) are the reasons why V_{AUX} changes as I_{SEC} linearly decreases during the inductor demagnetization process. Green arrows in **Figure 9** mark the ideal moment when V_{AUX} indirectly – but accurately – represents V_{OUT}. This moment is right at the time when I_{SEC} drops to zero; therefore, voltage drops across the diode and series resistance are negligible. After this moment, resonant ringing occurs. This ringing does not carry any useful information for the control loop. It is beneficial, however, for quasi-resonant operation when the controller waits for the valley (when the voltage on V_{SW} is low) to start a new switching cycle. This technique improves the efficiency of the flyback converter.

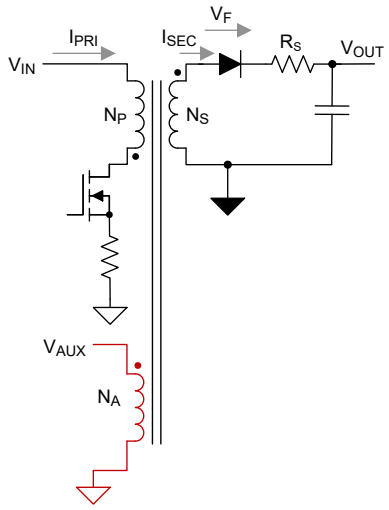


Figure 8. *Auxiliary winding in a PSR flyback.*

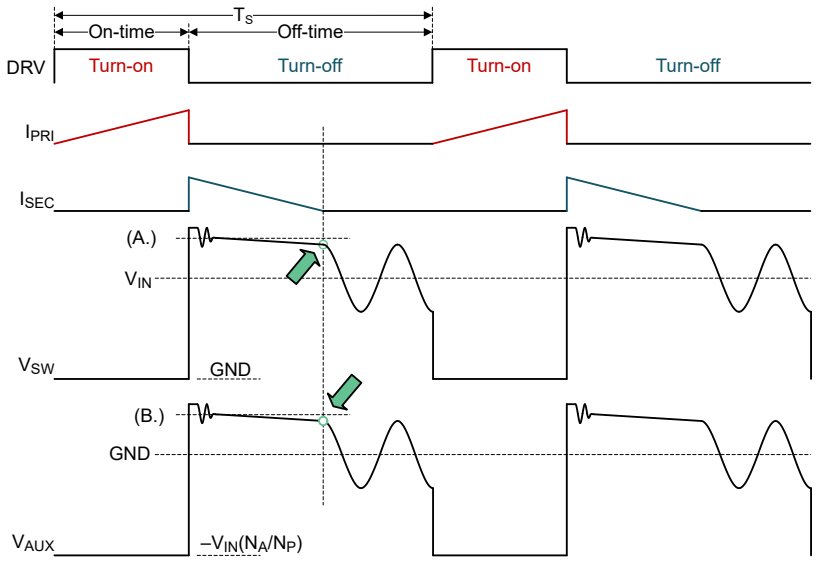


Figure 9. *Detailed PSR flyback waveforms.*

A. **Equation 1** defines the voltage level for the switch node waveform (V_SW) at the point (A.).

$$\frac{N_P}{N_S} \times (V_{OUT} + V_F + (I_S \times R_S) + V_{IN}) \quad (1)$$

B. **Equation 2** defines the voltage level for the auxiliary winding waveform (V_AUX) at the point (B.)

$$\frac{N_A}{N_S} \times (V_{OUT} + V_F + (I_S \times R_S)) \quad (2)$$

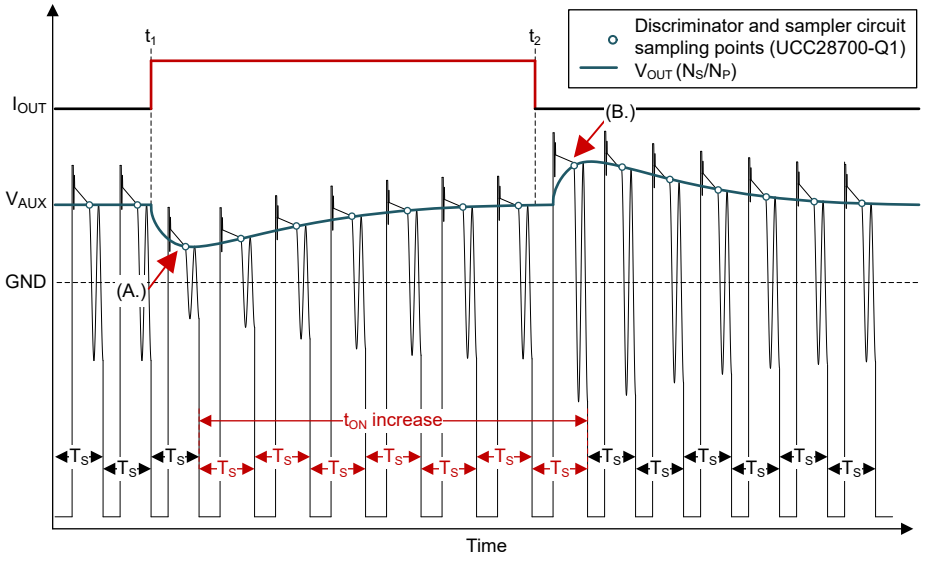
Equation 1 defines the voltage level for the switch node waveform (V_SW) at the point (A.). **Equation 2** defines the voltage level for the auxiliary winding waveform (V_AUX) at the point (B.)

Auxiliary Winding Waveforms During a Load Transient

Figure 10 shows the V_{AUX} waveform during a load transient. At time t_1, the output current increases and V_{OUT} drops. This event scales V_{AUX} accordingly. The controller responds to the current demand increase within one switching cycle (T_S). As a result, the controller increases the on-time (t_{ON}). The controller decreases f_{SW} to maintain DCM and quasi-resonant operation. After several cycles, V_{OUT} returns to the intended level. At time t_2, the process repeats with inverse logic.

The controller responds to the current demand increase (A.) within one switching cycle (TS).

At time t2, the process repeats with inverse logic (B.).



Waveforms are not in scale

Figure 10. *Auxiliary winding waveform during a load transient.*

Three Different Flavors of PSR

Multiple solutions allow for PSR in flyback converters. **Figure 11** shows the UCC28730-Q1 high-voltage PSR controller from Texas Instruments. These controllers integrate a special sampler circuit that samples the auxiliary winding "at the right time." The feedback divider senses the auxiliary winding directly without any additional filtering. The auxiliary winding biases the controller during operation. During flyback startup, the controller takes energy from the HV pin. After startup, the controller internally disconnects the HV pin and uses the rectified V_{AUX} for the bias. This improves the efficiency of the flyback converter.

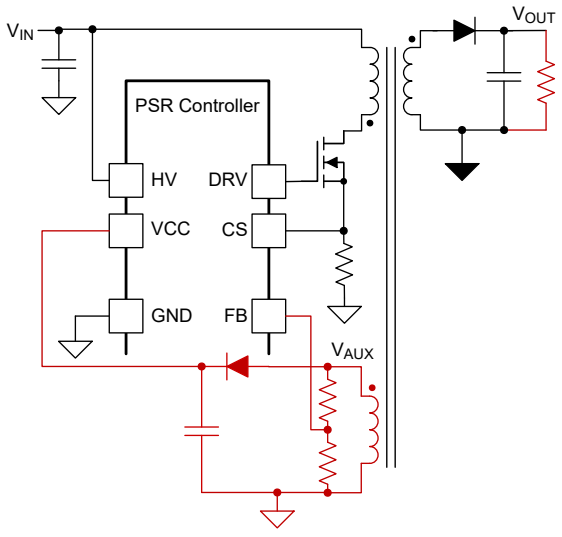


Figure 11. *Flyback converter with a PSR controller.*

Another solution is a low-voltage PSR controller that directly senses the reflected V_{OUT} across the main primary winding, such as the LM5180 from Texas Instruments. This solution eliminates the auxiliary winding completely, as shown in **Figure 12**. However, this method is possible only for lower V_{IN} – typically below 100 V. The benefits are a simpler transformer design and a small solution size.

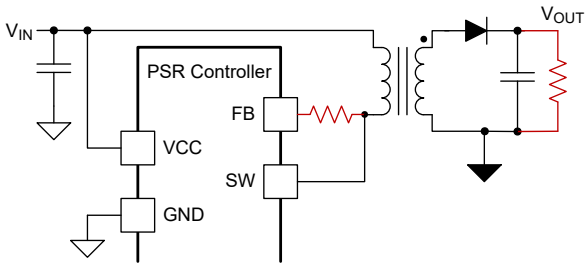


Figure 12. *Flyback converter with a PSR controller without an auxiliary winding.*

The last solution employs a conventional boost controller that uses a rectified and filtered V_{AUX} for regulation, as shown in **Figure 13**. Notice that the feedback looks very similar to the high-voltage PSR example, but the resistor divider senses the voltage after the rectification diode.

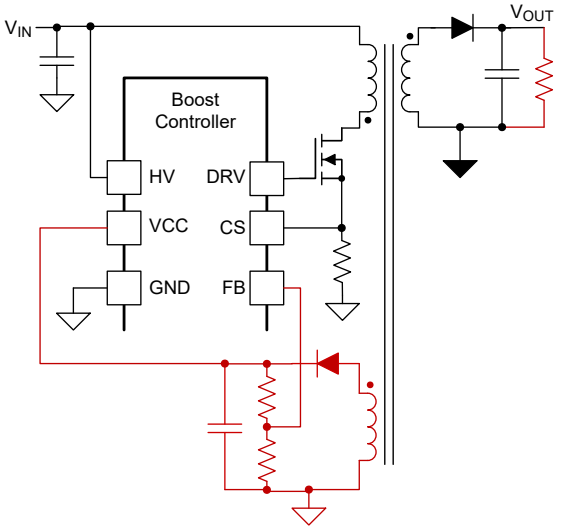


Figure 13. *PSR flyback converter with a conventional boost controller.*

PSR Takeaways

In the previous sections, I described how PSR works and how it differs from SSR with an optocoupler. These takeaways are important:

- The V_{AUX} waveform is composite and carries a lot of information.
- V_{AUX} provides accurate V_{OUT} information only once per period when I_{SEC} drops to zero.
- V_{AUX} carries the V_{OUT} feedback information only when switching.
- PSR controllers and converters use a special sample-and-hold circuit.
- Conventional boost controllers expect continuous feedback voltage (V_{FB}).

Next, let's look in detail at how to implement the PSR flyback with a boost controller, and how to convert the composite V_{AUX} waveform (see **Figure 14**) to the continuous analog signal for the FB pin (see **Figure 15**).

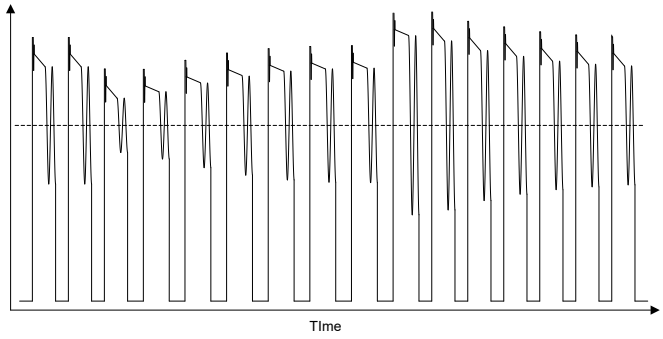


Figure 14. *Auxiliary winding waveform.*

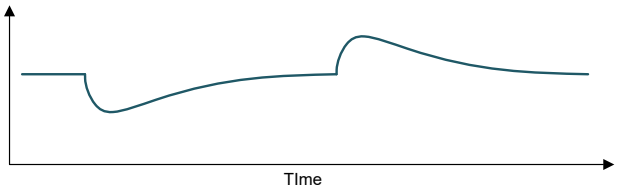


Figure 15. *Conventional controller FB pin waveform.*

PSR Flyback Example with a Conventional Boost Controller

Let's describe what is different in the design process for a PSR flyback using a conventional boost controller vs. using a dedicated PSR controller. For details about selecting all circuit components, see reference [1] and the relevant device-specific data sheet.

The example is an isolated gate-driver bias supply for hybrid electric vehicle and electric vehicle traction inverters (see **Figure 16** through **Figure 18**). The design uses the LM5156-Q1 boost controller, which does not provide any dedicated PSR functionality. The FB pin of the controller monitors a continuous voltage that is a scaled-down representation of V_{OUT}. The controller operates with a constant f_{SW}. Pulse skipping occurs when the controller can't further reduce the duty cycle. The flyback converter has one single isolated output with a virtual ground.

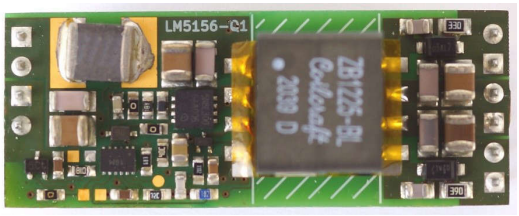


Figure 16. *PSR flyback example (top view).*

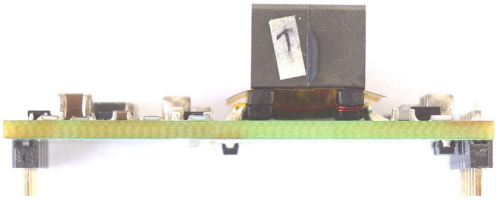


Figure 17. *PSR flyback example (side view).*

Figure 18. *PSR flyback example (bottom view).*

Design Parameters

The first step is to list the design parameters (see **Table 2**). V_{IN}, V_{OUT}, I_{OUT} and isolation requirements are system-defined parameters. f_{SW} and the mode of operation are typically the engineer's decision. These decisions are the result of compromises. Increasing f_{SW} reduces the solution size, especially the transformer. However, it also negatively affects losses, and thus the overall efficiency of the system.

Flyback converters can operate in three modes: continuous conduction mode (CCM), DCM and boundary conduction mode (BCM).

Each of these modes have drawbacks and benefits that are described in detail in [1]. Most low-power flyback converters operate in DCM, which you will see in the example. DCM enables the smallest transformer size and mitigates control-loop stability challenges.

Parameter	Specification
V_{IN}	6 V-42 V (52-V transient)
V_{OUT}	+15 V, –9 V (V_{OUT} = 24 V)
I_{OUT}	0 mA to 180 mA
f_{SW}	400 kHz
Mode of operation	DCM
Primary-to-secondary isolation	Basic, 2.5 kV
Controller	LM5156-Q1

Table 2. *Example PSR flyback parameters.*

Currents and Timing for Various Operating Conditions

The second step is investigating currents and timing for various operating conditions. There are two corner cases: the first is when V_{IN} is at its minimum and I_{OUT} is at its maximum. The converter has to be able to store enough energy during the turnon phase. Additionally, the switching period remains constant. This condition results in the highest possible duty cycle.

The second corner case is when V_{IN} is at its maximum and I_{OUT} is at its minimum. In this case, the converter reduces the duty cycle. The reduced duty cycle avoids

transferring more energy than the load consumes, and results in the lowest possible duty cycle.

Power Stage Designer™ software [2] is a great calculation tool that calculates the transformer inductance and generates waveforms based on a math model. After an iterative process, this example calculates the primary inductance (L_{PRI}) = 4 µH and the secondary inductance (L_{SEC}) = 16 µH. These values allow for operation in DCM with a constant f_{SW}.

Table 3 shows calculated timing and currents for both corner cases.

Parameter	Minimum duty-cycle condition	Maximum duty-cycle condition	LM5156-Q1
t_{ON}	0.13 µs	1.57 µs	Minimum 130 ns (**Figure 8**-**Figure 12**)
t_{OFF}	0.43 µs	0.76 µs	
Duty cycle	5.10%	62.86%	Maximum 92.8% (**Figure 8**-**Figure 16**)
Zero time	1.94 µs	0.16 µs	
Maximum I_{PRI}	1.33 A	2.36 A	
Maximum I_{SEC}	0.66 A	1.18 A	
Required minimum load $I_{L(MIN)}$	60 mA		

Table 3. *Calculated timing and currents for the PSR flyback example.*

Calculations confirm that the maximum duty-cycle condition is not a problem, as it does not exceed the LM5156-Q1 limit. The controller has a minimum t_{ON} = 130 ns. It is important to consider f_{SW} and read the value from **Figure 8** through **Figure 12** ($t_{ON(MIN)}$ vs. frequency) of the device data sheet. The electrical characteristics table lists the typical minimum t_{ON} = 50 ns. This value is, however, for a f_{SW} = 2.2 MHz.

When operating with the minimum t_{ON}, the converter transfers energy to the secondary side that the load has to consume within one switching cycle. When V_{IN} = 42 V, the converter requires a minimum load $I_{OUT(MIN)}$ = 60 mA to maintain a constant f_{SW} of 400 kHz.

Below 60 mA of load, the controller enters pulse-skipping mode, which effectively reduces f_{SW} by skipping complete cycles when the voltage on the FB pin exceeds a certain threshold. Exact circuit behavior during pulse-skipping mode is difficult to predict, as it depends on several parameters. Without switching, the auxiliary winding does not carry the V_{OUT} feedback information and the controller becomes "blind." This mode also compromises the transient response. However, pulse-skipping mode is the only option that allows you to reduce the minimum load on the output of the converter.

Resolving the Feedback

The feedback network uses a peak detector (half-wave rectifier) at the output of the auxiliary winding.

The circuit in **Figure 19** filters out unwanted content and tracks the positive V_{AUX} envelope that indirectly represents V_{OUT}. It is beneficial to set the positive amplitude of V_{AUX} such that it matches the controller's operating voltage range. For the example flyback converter, V_{AUX} is 12 V. Later, I will use V_{AUX} for self-biasing the controller.

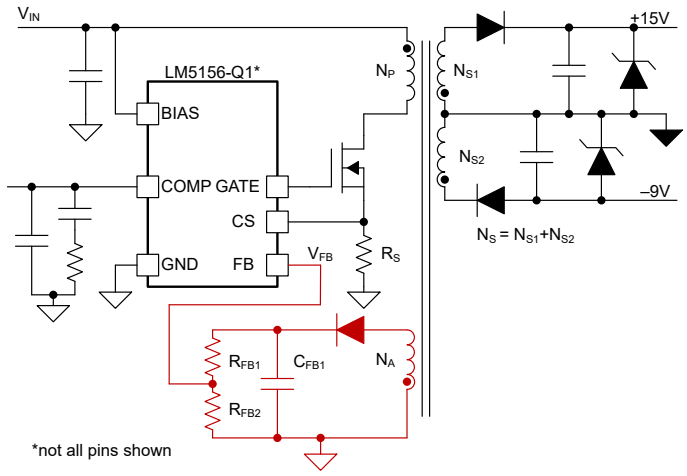


Figure 19. *Peak detector for PSR feedback.*

Equation 3 defines the relationship between V_{CC} (V_{AUX}) and V_{OUT}:

$$V_{CC} \cong V_{OUT} \times \frac{N_A}{N_S} \quad (3)$$

where N_A is the number of turns for the auxiliary winding and N_S is the number of turns for the secondary winding.

Table 4 lists the complete coupled inductor parameters provided by the magnetics manufacturer.

Winding	Inductance	Direct current resistance	Turns (refer to L_{PRI})
L_{PRI}	4 µH	0.015 Ω	1
Auxiliary inductance (L_{AUX})	4 µH	0.050 Ω	1
L_{S1}	5.76 µH	0.050 Ω	1.2
L_{S2}	2.56 µH	0.038 Ω	0.8
Combined (L_{S1} + L_{S2})	16 µH	0.088 Ω	2

Table 4. *Coupled inductor (transformer) parameters.*

After identifying V_{AUX} and the turns ratio, it is possible to design the feedback divider (R_{FB1}, R_{FB2}). The voltage drop across the auxiliary diode is similar to the voltage drop on the secondary side. For this reason, the equation for the feedback divider simplifies to **Equation 4**:

$$V_{FB} = V_{OUT} \times \frac{N_A}{N_S}\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right) \quad (4)$$

where V_{FB} is the reference voltage of the controller when V_{REF} = 1 V.

Keep the total resistance of the feedback divider in a range from kiloohms to tens of kiloohms. The example uses R_{FB1} = 11 kΩ and R_{FB2} = 1 kΩ.

Understanding how the peak detector circuit works in various conditions is important. The diode passes only the positive polarity of the V_{AUX}. This is when the signal carries the V_{OUT} information. This voltage quickly charges the filter capacitor (C_{FB1}). During the turnoff phase, the diode is reverse-biased and C_{FB1} slowly discharges through R_{FB1} and R_{FB2}. The resistor divider and capacitor values define the response time (time constant) of the peak detector and affect the transient response of the flyback converter.

When the time constant is too long, V_{FB} is not able to timely track V_{OUT} changes. With a sudden load increase, V_{OUT} drops, consequently reducing V_{AUX} amplitude during the turnoff phase. The diode does not open, however, because V_{AUX} is smaller than the voltage on C_{FB1}. This is because C_{FB1} does not discharge quickly enough. This event compromises V_{FB} and the transient response of the PSR flyback converter.

When the time constant is too short, the VFB signal has too much ripple, which may cause erratic controller behavior. The LM5156-Q1 boost controller has integrated overvoltage protection (OVP) for V_{OUT}. If the voltage at the FB pin rises above the overvoltage threshold (typically 110% of V_{REF}), the controller stops switching. Too much ripple at the FB pin may cause the controller to false-trigger OVP. If the controller enters pulse-skipping mode in light-load operation, the ripple increases. This is an important consideration.

Figure 20 shows further improvement of the circuit. A small capacitor across R_{FB2} adds a second pole to the low-pass filter and reduces the ripple. This is the preferred approach over increasing the C_{FB1} capacitor value, as it does not limit the transient response as much.

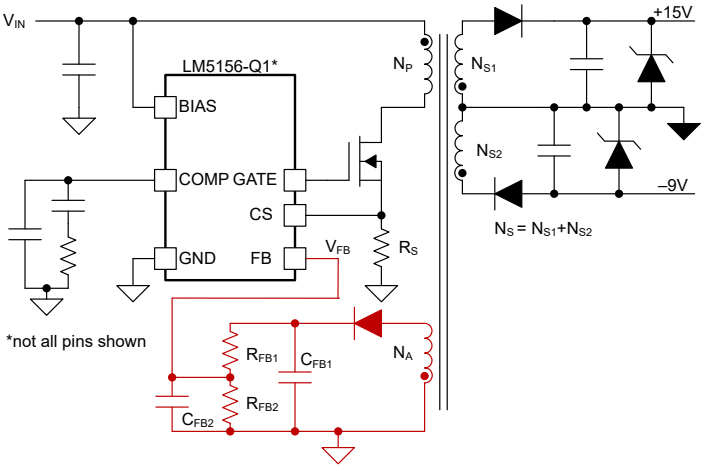


Figure 20. *Second-order filter for the feedback.*

Using a circuit simulator is a simple engineering method to find the ideal C_{FB1} and C_{FB2} values. The circuit simulator enables the investigation of peak detector behavior during transients. **Figure 21** shows a PSpice® for TI circuit for the peak-detector simulation. The circuit splits into three blocks.

On top is the V_{OUT} transient generator (highlighted in red). This circuit mimics the expected flyback converter V_{OUT} during transient events. G1, R4 and C2 form an ideal operational amplifier with a single-pole response. R5 and C3 slow down the feedback to match the flyback transient response. The current source, I_{OUT}, changes rapidly and excites the transient response. Adjust the V_{OUT} power supply, R5, C3 and I_{OUT} load for your circuit.

The auxiliary winding approximator (highlighted in blue) senses the V_{OUT} node. Ideal switches (S1, S2) chop V_{OUT} and approximate the V_{AUX} winding signal. Signal sources (V2, V3) define the expected duty cycle and f_{SW}.

The last block is the peak detector (highlighted in gray). This is the feedback network that this simulation helps optimize. I've already calculated the R_{FB1} and R_{RB2} values. The simulation enables you to change the values of C_{FB1} and C_{FB2} quickly.

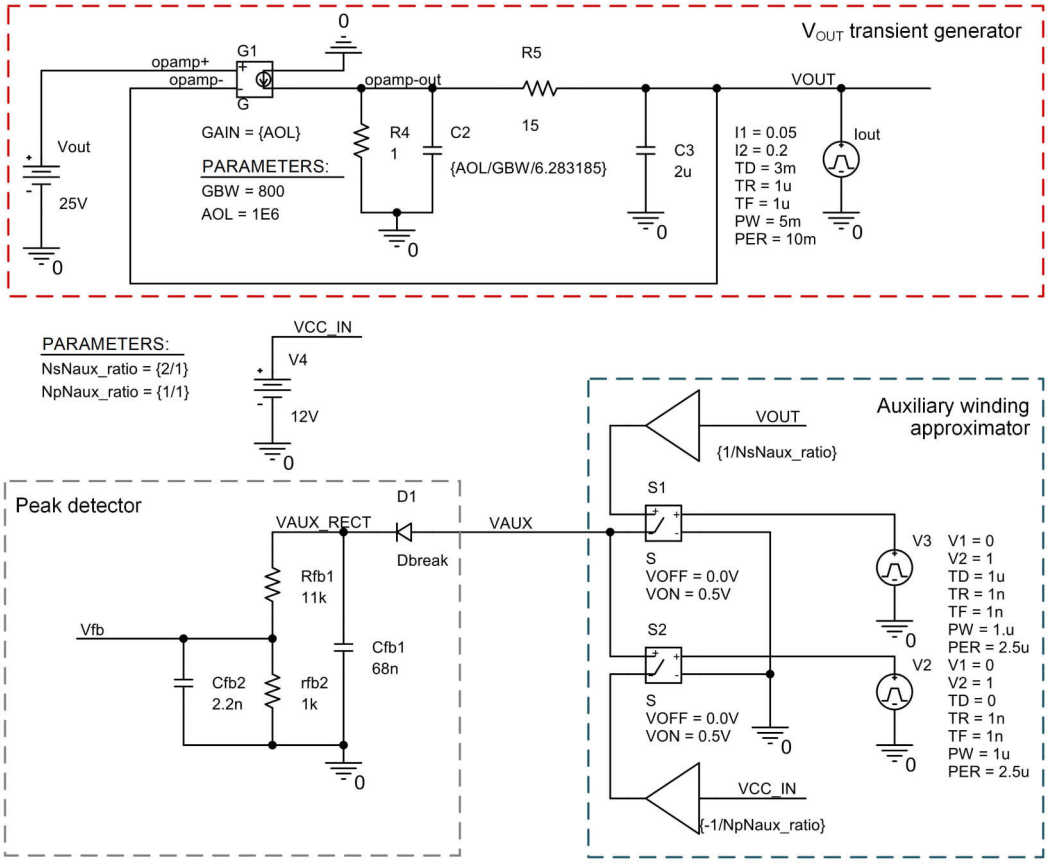


Figure 21. *Simulation circuit for a peak detector.*

Figure 22 shows the resulting signals from all three blocks. The open-loop operation of this circuit enables you to investigate the peak detector without affecting the controller and control-loop compensation.

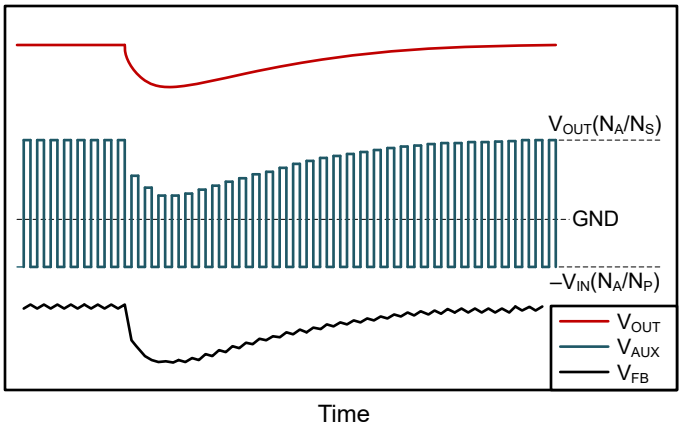


Figure 22. *Simulated circuit waveforms.*

Figure 23 shows a scenario where the time constant is too long. The dashed red trace shows the expected V_{OUT} during load transients. The gray trace represents the V_{FB} seen by the controller. During undershoot at t = 3 ms, C_{FB1} and C_{FB2} discharge at a slower rate than the V_{OUT} change. The diode in the peak detector remains closed and the V_{FB} does not track the output. During the overshoot at t = 8 ms, V_{FB} quickly ramps up, but remains higher even when the output returns to the regulated level.

These waveforms are for educational purposes only and show the open-loop condition. They illustrate an unwanted scenario when the peak detector is not able to track the output. In a closed-loop system, too long of a time constant becomes the dominant part of loop compensation and negatively affects the transient response of the flyback converter. Engineers often mistake this effect for loop compensation and try to adjust it in attempt to improve the response.

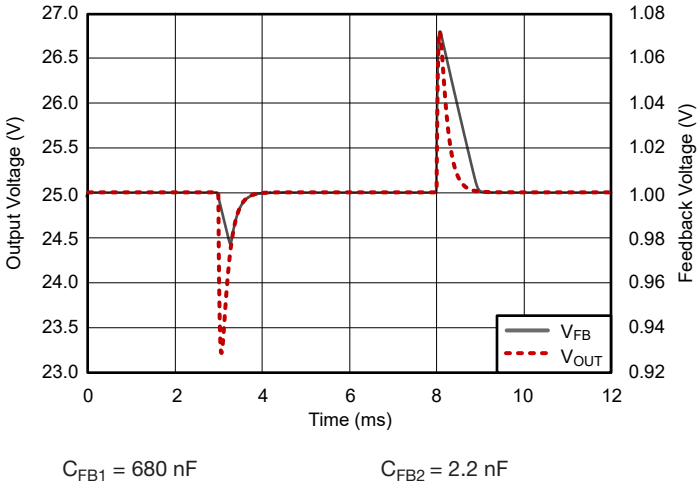


Figure 23. *When the time constant is too long.*

Figure 24 shows a scenario when the time constant of the peak detector circuit is correct. V_{FB} tracks V_{OUT} in both situations.

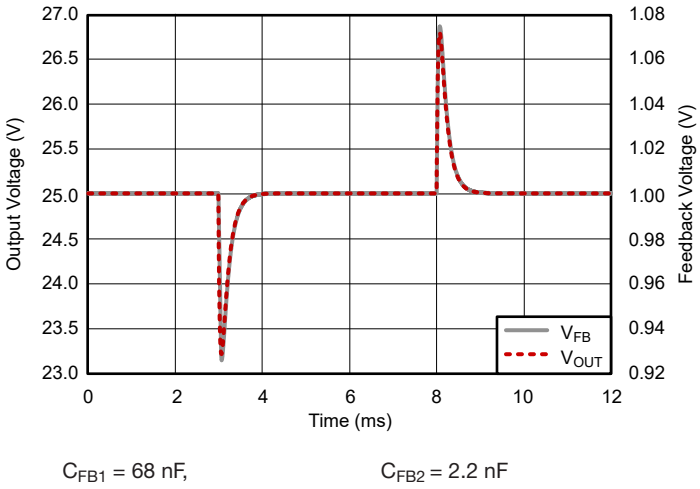


Figure 24. *When the time constant is optimal.*

Figure 25 and **Figure 26** show the V_{OUT} and V_{AUX} transient response of the PSR flyback example. I_{OUT} changes from 45 mA to 135 mA and back. Note the load-regulation effect in **Figure 25**.

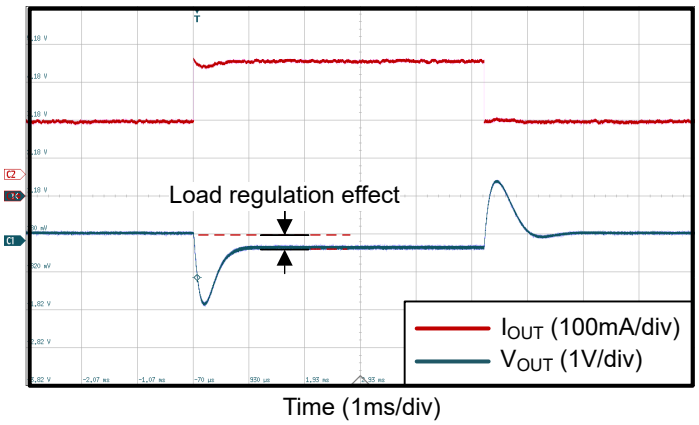


Figure 25. *PSR flyback example V_{OUT} transient response.*

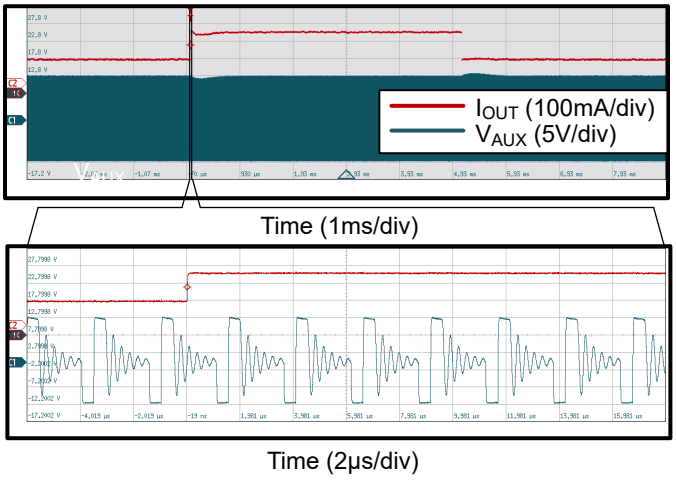


Figure 26. *PSR flyback example V_{AUX} transient response.*

Biasing Scheme to Improve Light-Load Efficiency

Powering the flyback controller from the auxiliary winding is very common. High-voltage flyback controllers cannot continuously operate from the high-voltage rail. The controller integrates a linear regulator (LDO) that stabilizes the voltage for internal circuitry. Powering this LDO from a high voltage is very inefficient and dissipates a lot of heat. For this reason, many controllers have a HV pin that is only in use during startup. After the startup of the converter, an internal switch disconnects the HV pin and the controller takes energy from the auxiliary winding for self-biasing.

Self-biasing from the auxiliary winding is also beneficial for low-voltage flyback converters. This method improves light-load efficiency. Additionally, the controller power consumption reduces the minimum load that the PSR flyback needs to maintain switching.

Figure 27 shows the bias scheme for the design example. The bias voltage for the V_{CC} pin requires a large bulk capacitance to keep the voltage rail stable. However, the feedback path requires a fast transient response to quickly track V_{OUT}. For this reason, there is a second half-bridge rectifier (highlighted in green) that does not compromise the feedback network (highlighted in red). Two separate paths for self-biasing and feedback offer the best performance without compromises. This design technique unfortunately rarely occurs in designs.

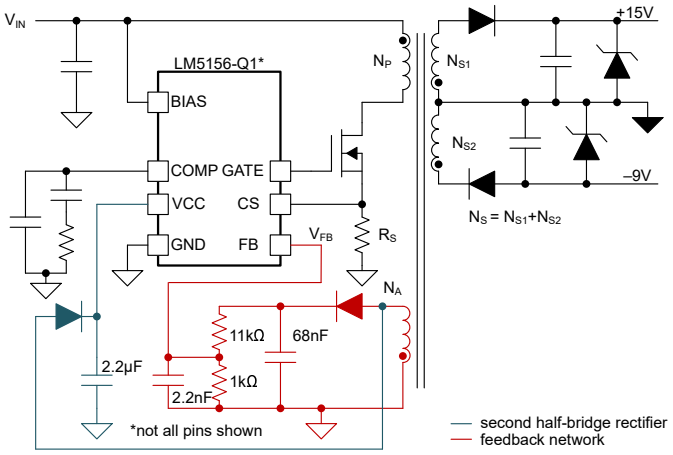


Figure 27. *Self-bias for a PSR flyback with a conventional boost controller.*

Solving the Minimum Load

I mentioned previously that PSR flyback converters require a minimum load to maintain continuous operation. If the load draws zero current, the converter requires a dummy load on the output. Without the dummy load, the output may rise way above the regulated levels and permanently damage the downstream circuits. There are two different solutions for the dummy load; each has drawbacks and benefits:

- Resistors as a dummy load allow for better load regulation of the PSR flyback converter. However, resistors dissipate power under all conditions, thereby reducing the overall efficiency of the system.

- Using Zener diodes is a more pragmatic solution (see **Figure 28**). Certain Zener diodes will have a breakdown voltage slightly above the typical V_{OUT}. When the controller can't further reduce the energy delivered to the secondary side during the switching cycle, V_{OUT} increases to the point where the Zener diodes conduct and sink current. They dissipate the excessive energy in the form of heat but prevent V_{OUT} from increasing significantly above the regulated level (see **Figure 29**).

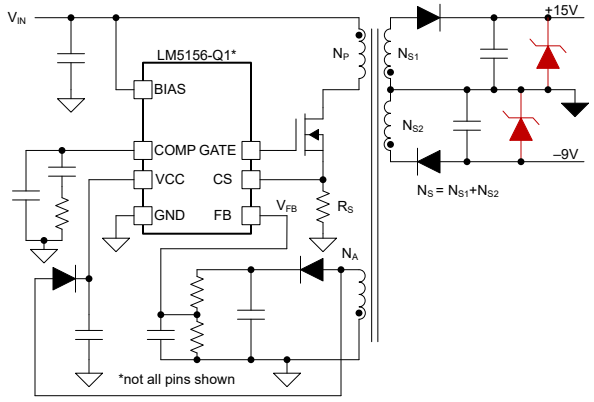


Figure 28. *Zener diodes solve the minimal load.*

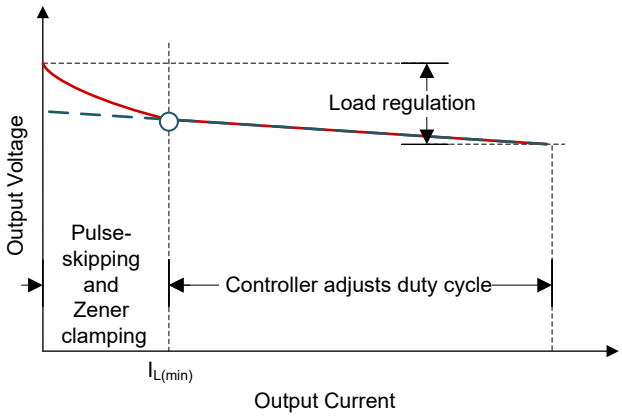


Figure 29. *Load regulation of the PSR flyback with Zener diodes as a dummy load.*

There are challenges associated with Zener diodes, however. Zener diodes with a Zener voltage (V_Z) < 4.7 V have a negative temperature coefficient. Zener diodes with V_Z > 4.7 have a positive temperature coefficient. Additionally, the initial accuracy varies.

Figure 30 shows the tolerance field for a Zener diode with V_Z = 16 V at a Zener current (I_Z) = 5 mA. V_Z varies from 14.6 V to 17.7 V over the typical automotive temperature operating range of –40°C to 125°C. It is important that V_Z never drops below the V_{OUT} regulated level, because that could cause excessive current flow and possibly permanently damage the converter. Ideally, V_Z gets close to V_{OUT} but never below.

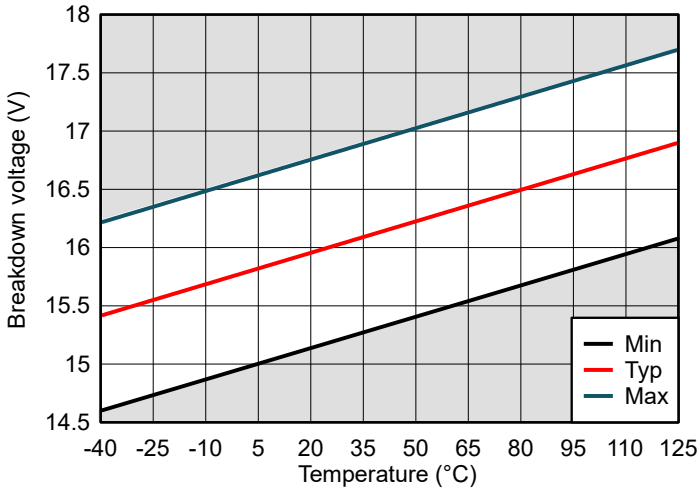


Figure 30. *Zener diode tolerance field.*

Compensating the Current-Sense Resistor

Boost controllers that use the peak current-mode control scheme sense current through the primary winding across the current sense (shunt) resistor (R_S). Every current shunt resistor has a parasitic inductance (L_S). L_S adds error to the current reading, as it causes spikes on the leading and falling edges of the current-sense signal (V_{CS}). Even with an integrated blanking time, the current-sensing circuitry may detect overcurrent events, especially when the t_{ON} is close to minimum. For this reason, it is important to add a compensation circuit.

Figure 31 shows a simple R_C, C_C compensation network, which has to satisfy **Equation 5**:

$$C_C \times R_C = \frac{L_S}{R_S} \quad (5)$$

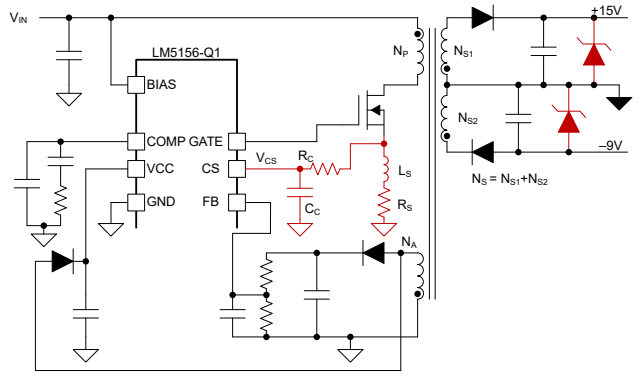
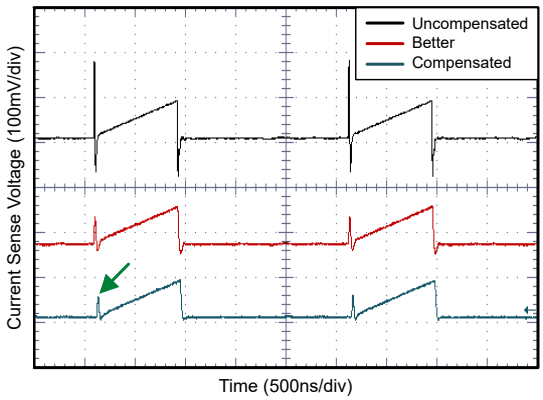


Figure 31. *Compensating the current-sense resistor.*

Figure 32 shows three different waveforms taken under the same conditions. The black trace is V_{CS} without any compensation circuit. The red trace shows improvement with the first iteration of the compensation network. The teal trace represents V_{CS} with a properly compensated shunt resistor. Values in this example are C_C = 15 nF (COG) and R_C = 1.5 Ω for a 0.33-Ω shunt resistor in a 0603 package.



Compensated:

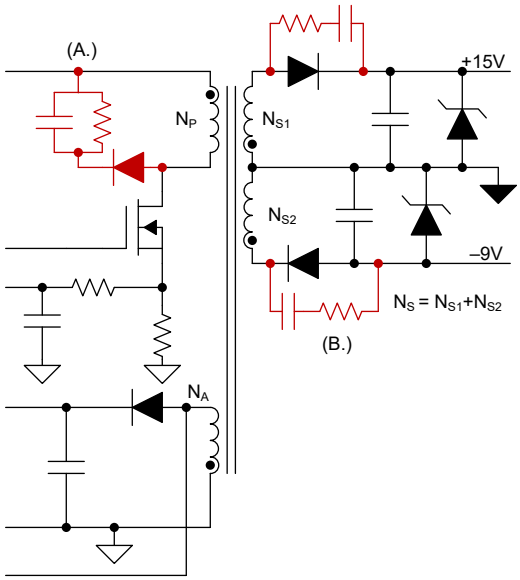
- R_C = 1.5 Ω for a 0.33-Ω shunt resistor in a 0603 package
- C_C = 15 nF (COG)

Figure 32. *V_{CS} waveform with and without compensation.*

The notch (green arrow) is the turnon current from the integrated gate driver. Taking this measurement requires precise probing – ideally with an active oscilloscope probe. It is also an iterative process, where you will need to try different values around an initial guess to find the right combination.

Snubber Circuits

Flyback converters generate unwanted high-frequency ringing. The primary winding leakage inductance and the switch output capacitance form a parasitic inductor-capacitor network that generates ringing during the turnoff transient. The secondary winding leakage inductance and the reverse-recovery current of the secondary rectifier cause ringing during the turnon transient. I highly recommend using snubber circuits that suppress this unwanted ringing for all types of flyback converters. **Figure 33** shows the location and values of snubber circuits in the example flyback. For snubber design guidance, see [**1**-**2**].



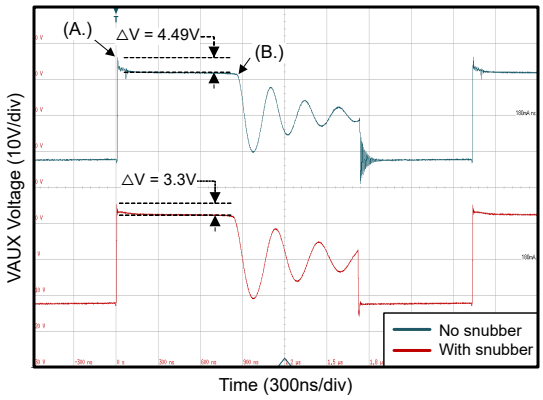
Snubber A	Snubber B
D = Fast (100 V/200 mA)	R = 33 Ω, 0805
R = 2.7 kΩ, 0805	C = 100 pF, 100 V, 0805, COG
C = 10 nF, 100 V, 0805, COG	

Figure 33. *Snubber circuits in a flyback converter.*

The ringing also negatively affects V_{AUX}. **Figure 34** illustrates the problem. The overshoot during the turnoff transient is higher without the snubber circuit. This overshoot charges the peak detector to a higher voltage. Additionally, the overshoot is proportional to I_{OUT}. This behavior adds error to V_{FB}, which also changes with

the load. **Figure 35** shows how snubber circuits affect the load regulation of the PSR flyback example. The practical example shows a nearly 50% load regulation improvement.

Pay attention to snubbers in PSR flyback converters with a conventional boost controller. This is especially important in volume production, when many parts have a second source that secures the supply chain. Changing the transformer supplier, the primary switch (transistor) or the rectifier diode requires design verification. For example, if the leakage inductance changes, the current snubber circuit becomes less efficient because the resonant frequency changes.



A. Detected voltage

B. Ideal sampling point

I_{OUT} = 180 mA

Figure 34. *V_{AUX} waveforms with and without snubber circuits*

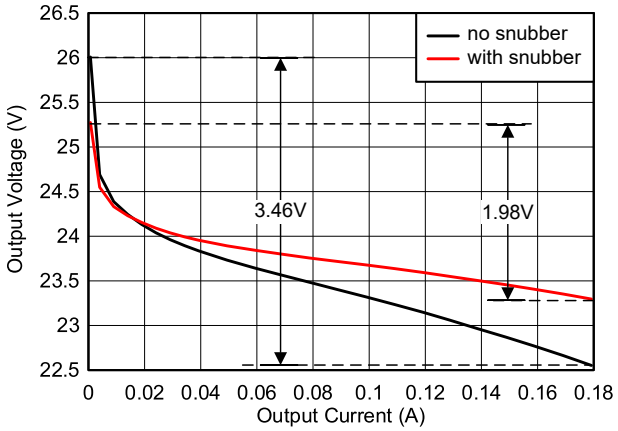


Figure 35. *Load regulation of the PSR flyback example with and without snubber circuits.*

Another way to improve the load regulation is to add a more complicated peak detector with leading-edge blanking. Unfortunately, this solution adds cost and complexity to systems, and ensuring stability over all operational conditions is difficult.

Conclusions

This paper described lesser-known challenges of PSR flyback converters that use boost controllers. The absence of a dedicated sampler circuit available in PSR controllers complicates designs. Applications for which load regulation, fast transient response or low standby current are a concern can benefit greatly from dedicated PSR flyback controllers.

Additionally, most PSR controllers operate in quasi-resonant mode with valley switching, further improving efficiency. Using conventional controllers makes sense in applications with less stringent requirements. Many systems implement a post-regulator that stabilizes V_{OUT}. In this case, the main purpose of the flyback converter is galvanic isolation between the primary and secondary sides. In such applications, compromises on transient response and load regulation are acceptable.

These steps require extra attention during the design process:

- Identify the minimum and maximum duty cycle for the given operating conditions.
- Design the V_{AUX} peak detector such that it can quickly track V_{OUT} during load transients.
- Minimize ringing on the switch node and auxiliary winding with snubber circuits.
- Separate the feedback path from the controller self-bias.
- Use the compensation network that compensates the parasitic inductance of the current-sense (shunt) resistor.
- Design the loop compensation with the envelope detector in mind. Account for a higher phase margin.

- Verify the transient response for minimal, maximal and nominal V_{IN}.
- Evaluate the circuit behavior in conditions when the controller enters pulse-skipping mode.

References

1. Picard, Jean. "**Under the Hood of Flyback SMPS Designs**." Texas Instruments Power Supply Design Seminar SEM1900, literature No. SLUP261, 2010-2011.
2. Texas Instruments. n.d. **Power Stage Designer software**. Accessed Dec. 26, 2023.

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