

## PR209

### Spartan™-II Design 2

Single-Channel Linear Regulator Power Management Solution Providing up to 1.5 A from  $V_{IN} = 3.3\text{ V}$  and 1.2 A from  $V_{IN} = 5.0\text{ V}$

#### FEATURES:

- Independent linear regulators allow higher power dissipation than an integrated dual-channel solution.
- Linear regulator solution saves cost and space over a switching DC/DC solution.
- Control cost by using lower current linear regulators from the TPS79xxx family for U2 and U3 to meet specific application requirements.
- Linear regulators start-up fast, allowing large in-rush currents for charging decoupling capacitors and FPGA start-up. The current draw on the input power supply is minimized by the use of the:
  - o External supervisory (SVS), U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - o Soft-start circuit consisting of the external PMOS transistor Q1 and supporting passive components to provide 10 ms rise time for  $V_{CCINT}$ .
  - o Sequential sequencing of  $V_{CCINT}$  then  $V_{CCO}$  using  $V_{CCINT}$  to enable the  $V_{CCO}$  regulator, U3.
- The design meets Xilinx's  $V_{CCINT}$  and  $V_{CCO}$  start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

#### IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at <http://www.ti.com/xilinuxfpga> for more information and other reference designs.
- Link to datasheets at <http://focus.ti.com/lit/ds/symlink/TPS78601.pdf>, <http://focus.ti.com/lit/ds/symlink/tps79601.pdf>, and <http://focus.ti.com/lit/ds/symlink/tps3809k33.pdf>.
- Link to application note SLVA118 <http://focus.ti.com/lit/an/slva118/slva118.pdf> to explore the thermal considerations in using linear regulators.
- Link to application note SLVA156 <http://focus.ti.com/lit/an/slva156/slva156.pdf> for more details on the soft-start circuit.

#### IMPLEMENTATION NOTES:

- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.
- **$I_{CCINT}$  inrush current:** Mitigated by softstart.

- **Power Dissipation/Thermal Issues:** The DDPACK packaged regulators in this design are limited to 3W @  $T_A = 55^\circ \text{C}$  and no airflow, due to power dissipation limitation of the package.
  - o Refer to the application section of the datasheet for maximum power dissipation at different ambient conditions as well as guidance on sizing the ground plane area underneath the package for heatsinking.
  - o The linear regulator's output current capability can be computed by rearranging the following equation:  

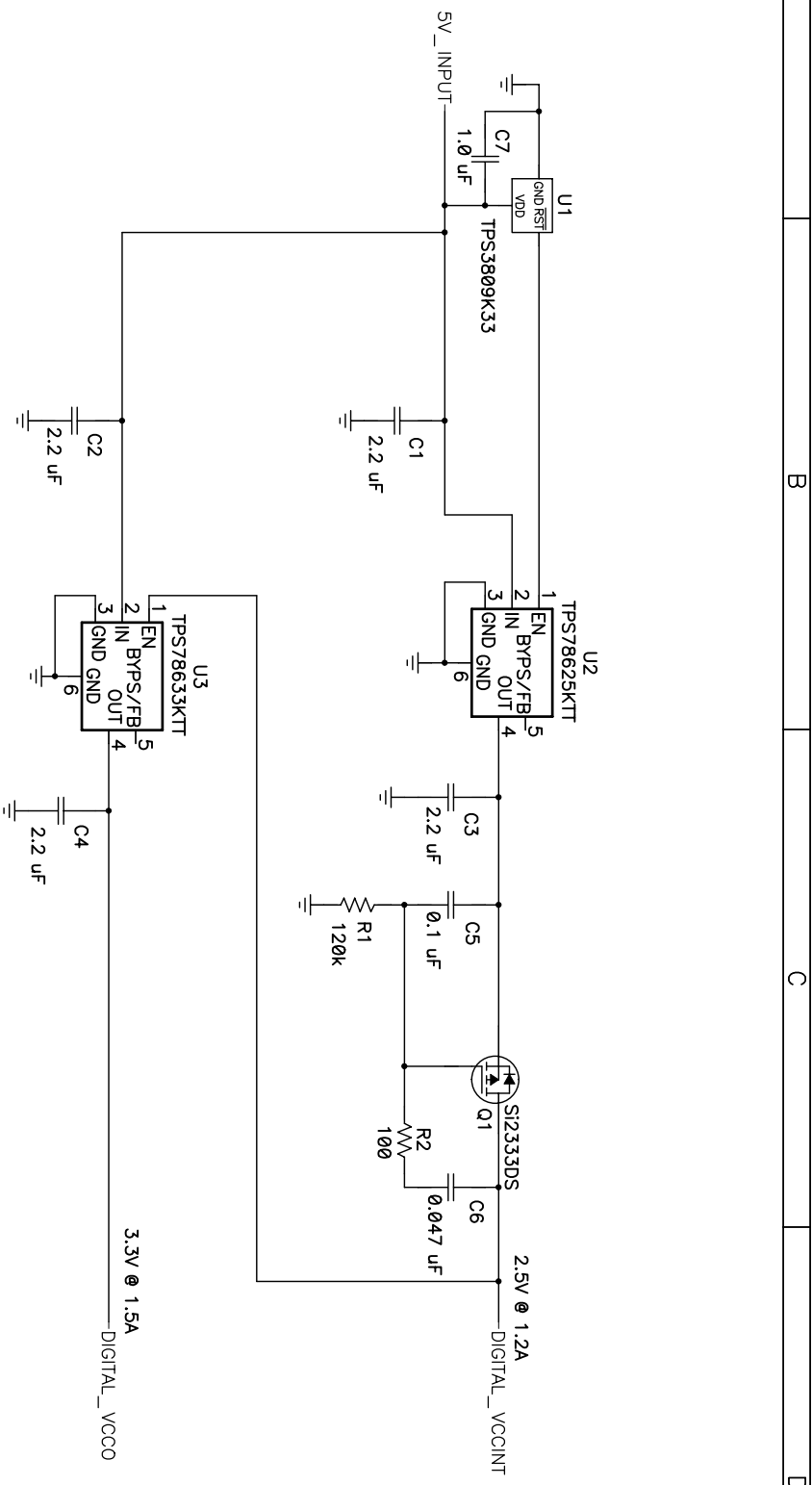
$$P_{Dmax} = (V_{IN} - V_{CCINT}) * I_{CCINTmax}$$

As an example, with  $V_{CCINT} = 2.5 \text{ V}$  and  $P_{Dmax} = 3 \text{ W}$ :

- $I_{CCINTmax} = P_{Dmax} / (V_{IN} - V_{CCINT})$ .
  - $I_{CCINTmax} = 3.75 \text{ A}$  when  $V_{IN} = 3.3 \text{ V}$ . The TPS786xx has a guaranteed dc current rating of 1.5 A but can provide up to its minimum current limit of 2.4 A for short periods.
  - $I_{CCINTmax} = 1.2 \text{ A max}$  when  $V_{IN} = 5.0 \text{ V}$ .
- **Soft Start Circuitry:** PMOS transistor Q1 should be selected so that its threshold voltage,  $V_{TH}$ , is at least 0.9 V below the  $V_{CCO}$  voltage or lower (e.g.,  $V_{TH} < 2.5 \text{ V} - 0.9 \text{ V} = 1.6 \text{ V}$ ). In addition, the transistor's  $R_{DSon}$  should be low enough, when driven by  $V_{CCINT}$ , that the voltage drop across the transistor at maximum current (e.g.,  $I_{CCINTmax} * R_{DSon}$ ) does not cause  $V_{CCINT}$  to fall below its -5% tolerance.
- **Modifications:**
  - o Select the appropriate voltage option from the TPS786xx (1.5A rating) or TPS796xx (1.0A rating) family. TPS78601 and TPS79601 are the adjustable versions, and  $V_{OUT}$  is set by a voltage divider (external resistors) on the FB pin.
  - o Select the appropriate TPS3809 option to monitor the input supply voltage. TPS3809L30 is recommended for monitoring 3.3V.
  - o For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).
  - o Note that with lower input supplies, such as 3.3V, the linear regulators can support higher output currents (see previously presented power dissipation calculations).

## QUESTIONS?

- Send an email to <mailto:fpgasupport@list.ti.com>



|          |           |                       |    |
|----------|-----------|-----------------------|----|
| Title    |           | Spartan II Single LDO |    |
| Size     | Number    | Rev                   |    |
| B        | PR209     |                       |    |
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| Filename | pr209.sch | Sheet                 | of |

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|                         |                | <b>PR209 BOM</b>   |             |            |                    |
|                         |                |  |             |            |                    |
| <b>COUNT</b>            | <b>RefDes</b>  | <b>DESCRIPTION</b>   | <b>SIZE</b> | <b>MFR</b> | <b>PART NUMBER</b> |
| 4                       | C1, C2, C3, C4 | Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%                            | 805         | muRata     | GRM21BR60J225KC01  |
| 1                       | C5             | Capacitor, Ceramic, 0.1-uF, 25-V, X7R, 10%                             | 603         | muRata     | GRM188R71E104KA01  |
| 1                       | C6             | Capacitor, Ceramic, 0.047-uF, 16-V, X7R, 10%                           | 603         | muRata     | GRM188R71C473KA01  |
| 1                       | C7             | Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%                            | 603         | muRata     | GRM188R60J105KA01  |
| 1                       | Q1             | MOSFET,P-ch, -12 V, 4 A, 51 milliohm                                   | SOT23       | Vishay     | Si2333DS           |
| 1                       | R1             | Resistor, Chip, 120k-Ohms, 1/16-W, 1%                                  | 603         | Std        | Std                |
| 1                       | R2             | Resistor, Chip, 100-Ohms, 1/16-W, 1%                                   | 603         | Std        | Std                |
| 1                       | U1             | IC, 3-Pin Supply Voltage Supervisor                                    | SOT23       | TI         | TPS3809K33         |
| 1                       | U2             | IC, Ultra Low-Noise, High PSRR, Fast RF 2.5V 1.5A LDO Linear Regulator | DDPAK-5     | TI         | TPS78625KTT        |
| 1                       | U3             | IC, Ultra Low-Noise, High PSRR, Fast RF 3.3V 1.5A LDO Linear Regulator | DDPAK-5     | TI         | TPS78633KTT        |

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265