PR212

Spartan™-IIE Design 3

TPS64203 Switching DC/DC Controller-Based Power Management Solution Providing up to 3 A from V_{IN} = 5.0 V or 3.3 V

FEATURES:

- Tiny SOT-23 switching DC/DC controller, U2, delivers up to 3 A at low cost.
- Easily customizable design allows for maximum cost control by:
  - Sizing Q1 for the amount of current up to 3 A to meet the application's I_{CCINT} requirement,
  - Omitting current sense resistor R1 and connecting ISNS to the drain of Q1,
  - Selecting the linear regulator from the TPS79xxx family to meet the application's I_{CCO} requirement.
- In-rush current (for charging decoupling capacitors and FPGA start-up) that places a demand on the input power supply is minimized by the use of the:
  - External supervisory (SVS) IC, U1, which monitors the input rail and prevents the regulator from enabling until the input bulk capacitors (not shown in the schematic) are fully charged.
  - Integrated soft-start of U2 with assistance from the additional soft-start circuitry (R7, R8, R9, C4 and Q4) provides 2.5 ms rise time for V_{CCINT}.
  - Sequential sequencing of V_{CCINT} then V_{CCO} using the discrete SVS circuit formed by bipolar transistors Q2 and Q3 and supporting passives to enable the V_{CCO} regulator, U3
- The design meets Xilinx's V_{CCINT} and V_{CCO} start-up profile requirements, where applicable, including monotonic voltage ramp, in-rush current and power voltage ramp time requirements.

IMPORTANT WEB LINKS:

- Link to the TI home page for Xilinx FPGA power management solutions at http://www.ti.com/xilinxfpga for more information and other reference designs.
- Link to datasheets at http://focus.ti.com/lit/ds/symlink/tps64203.pdf, http://focus.ti.com/lit/ds/symlink/tps78601.pdf, and http://focus.ti.com/lit/ds/symlink/tlc7705.pdf.
- Link to application note SLVA118 http://focus.ti.com/lit/an/slva118/slva118.pdf to explore the thermal considerations in using linear regulators.
- Link to application note SLVA160 http://focus.ti.com/lit/an/slva160/slva160.pdf for guidance on selecting a different option from the TPS642xx family.

IMPLEMENTATION NOTES:

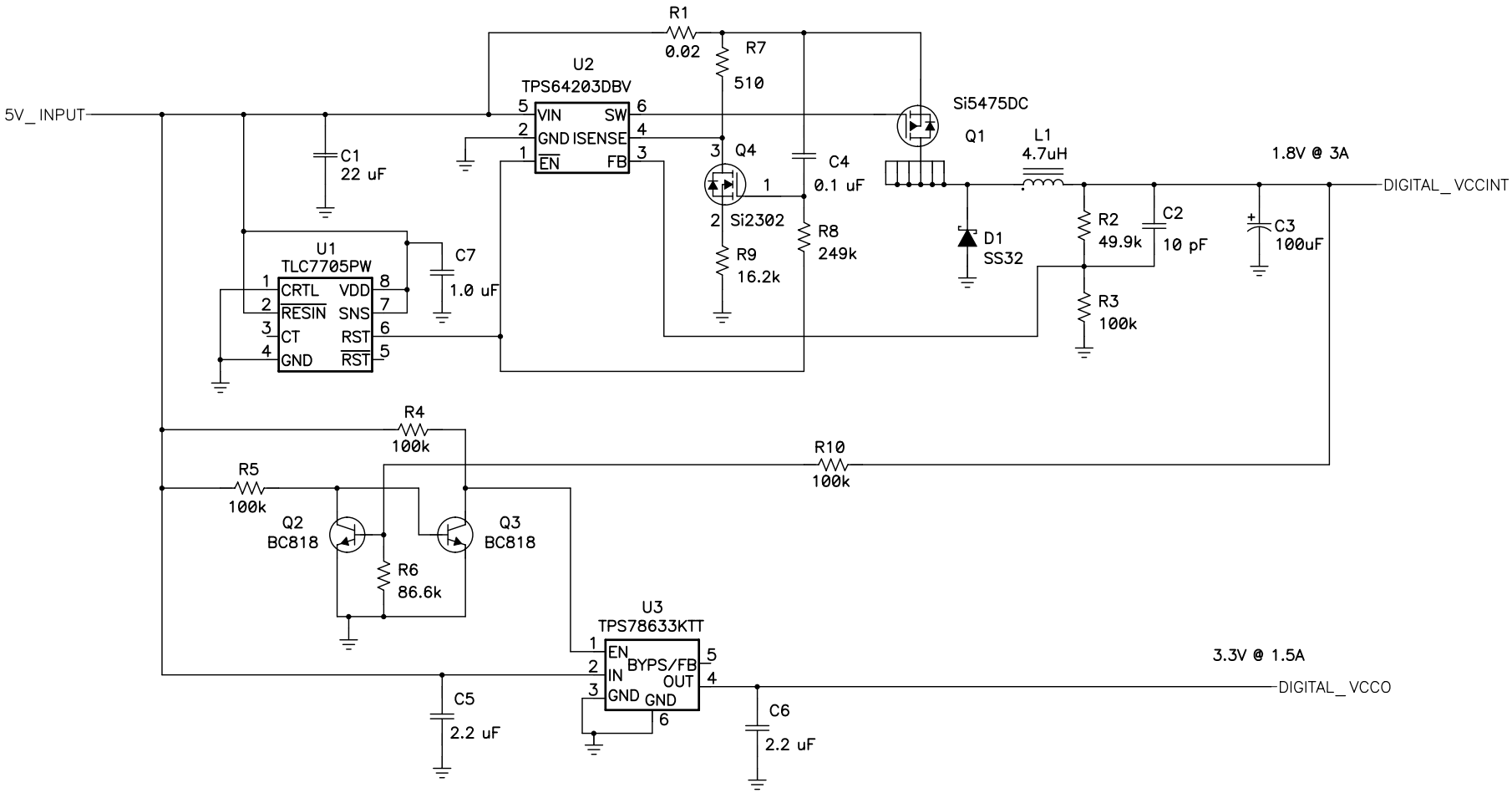
- **Sequencing:** Although Xilinx FPGAs **do NOT require it**, this reference design employs sequencing. This practice is consistent with good power supply design

and prevents the input power supply from being pulled down due to supporting in-rush currents for charging large capacitive loads.

- **V_{CCINT} minimum ramp time:** Met by integrated soft-start of U2 with assistance from the additional soft-start circuitry (R7, R8, R9, C4 and Q4).
- **I_{CCINT} inrush current:** Mitigated by softstart.
- **Power Dissipation/Thermal Issues:** Refer to the application section of the linear regulator datasheet for maximum power dissipation at different ambient conditions as well as guidance on sizing the ground plane area underneath the package for heatsinking.
- **Designing with the TPS64203:**
  - The TPS64203 controller has limited current to drive the gate of the PMOS transistor, Q1. To ensure proper operation of the controller, a PMOS transistor with a maximum total gate charge, Q_g, of less than 50 nC is required.
  - Omitting current sense resistor R1 and connecting ISNS to the drain of Q1, thereby using the R_{DSon} of Q1 as the current sense, results in an effective, but slightly less accurate, current limit function.
- **Soft Start Circuitry:** Although only 100 uF of output capacitance is recommended for the TPS64203 controller to operate when providing 3A, the output of the controller needs at least 470 uF of total capacitance in order for the additional soft-start circuitry (R7, R8, R9, C4 and Q4) to work properly. The additional bulk bypass capacitance (not shown in the schematic) required for the V_{CCINT} rail of the FPGA will most likely meet this requirement.
- **Layout:** The 1.0 uF capacitor, C7, should be placed as close as possible between VDD and GND of the TLC77xx SVS IC.
- **Modifications:**
  - CT of TLC7705 is not connected, but can be used with a capacitor to add a delay between the 5 V rail coming up and RST = /EN of TPS64203.
  - Adapt for 3.3V supply by:
    - Omitting U3 circuit,
    - Replacing TLC7705 with TLC7733.
  - For a low-cost, discrete Supply Voltage Supervisory Circuit alternative to U1, please see reference design PR286 (Active-High Reset Output) or PR281 (Active-Low Reset Output).

QUESTIONS?

- Send an email to mailto:**fpgasupport@list.ti.com**



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PR212 BOM

COUNT	RefDes	Description	SIZE	MFR	Part Number
1	C1	Capacitor, Ceramic, 22-uF, 10-V, X5R, 10%	1210	muRata	GRM32ER61A226KA65
2	C2, C4	Capacitor, Ceramic, 10-pF, 50-V, C0G, +/- 5pF	603	TDK	C1608C0G1H100D
1	C3	Capacitor, Tantalum, 100-uF, 10-V, 80-milliohm, 20%	7343 (D)	Vishay	593D107X0010D2T35
2	C5, C6	Capacitor, Ceramic, 2.2-uF, 6.3-V, X5R, 10%	805	muRata	GRM21BR60J225KC01
1	C7	Capacitor, Ceramic, 1.0-uF, 6.3-V, X5R, 10%	603	muRata	GRM188R60J105KA01
1	D1	Diode, Schottky Barrier Rectifier, 3-A, 20-V	SMC	Vishay	SS32
1	L1	Inductor, High Current, SMT, 4.7-uH, 5.4-A, 18-milliohm	0.26x0.09	Vishay	IDC-5020NB4R7M
1	Q1	MOSFET, P-ch, 20V,4.8-A, 76-milliohm	1206-8	Siliconix	Si5475DC
2	Q2, Q3	Bipolar, NPN, 30-V, 800-mA, 310-mW	SOT23		BC818
1	Q4	MOSFET, N-ch, 20-V, 2.8-A, 85-milliOhms	SOT23		Si2302
1	R1	Resistor, Chip, 0.02-Ohms, 1/4-W, 1%	1210	Std	Std
1	R2	Resistor, Chip, 49.9k-Ohms, 1/16-W, 1%	603	Std	Std
4	R3, R4, R5, R10	Resistor, Chip, 100k-Ohms, 1/16-W, 1%	603	Std	Std
1	R6	Resistor, Chip, 86.6k-Ohms, 1/16-W, 1%	603	Std	Std
1	R7	Resistor, Chip, 510-Ohms, 1/16-W, 1%	603	Std	Std
1	R8	Resistor, Chip, 249k-Ohms, 1/16-W, 1%	603	Std	Std
1	R9	Resistor, Chip, 16.2k-Ohms, 1/16-W, 1%	603	Std	Std
1	U1	IC, Voltage Supervisor, Micropower	TSSOP-8	TI	TLC7705PW
1	U2	IC, Step-Down Controller	SOT23-6	TI	TPS64203DBV
1	U3	IC, Ultra Low-Noise, High PSRR, Fast RF 1.5A LDO Linear Regulator	DDPAK-5	TI	TPS78633KTT

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