

High-Efficiency Power Solution Using DC/DC Converter For TMS320C2834x Microcontrollers

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PMP - DC/DC Low-Power Converters

ABSTRACT

This reference design is intended for users designing with the TMS320C2834x microcontrollers. This design, employing sequenced power supplies, describes a system with an input voltage of 5 V and uses high-efficiency DC/DC converters with integrated FETs for a simple, small design.

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1 Introduction

In multivoltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power-up and power-down operations.

Sequencing refers to the order, timing, and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long-term reliability of the dual-voltage device, whereas the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic, or data converter integrated circuits (IC).

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition in which the processor and another device both attempt to control a bidirectional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

[Table 1](#) shows the power-on sequencing for TMS320C2834x microcontrollers. As mentioned in the table, all voltage rails must be powered up within 5 ms.

2 Power Requirements

The power requirements are as specified in [Table 1](#).

Table 1. TMS320C2834x Power Specifications

	Pin Name	Voltage (V)	I _{max} (mA)	Tolerance	Sequencing Order	Timing Delay
Core	VDD	1.1 / 1.2 ⁽¹⁾	1000 ⁽²⁾	±5%	1	All voltage rails must be powered up within 5 ms.
I/O	VDD18	1.8	80	±5%	2	
I/O	VDDIO	3.3	200	±5%	2	

(1) CVDD = 1.2 V for 300-MHz devices; CVDD = 1.1 V for 200-MHz devices.

(2) Maximum current on VDD at 300 MHz is 1000 mA; maximum current on VDD at 200 MHz is 600 mA.

3 Features

The design uses the following high-efficiency DC/DC converters with integrated FETs ([Table 2](#)).

Table 2. DC/DC Converters With Integrated FETs

Devices	TPS62290 (for 1.2 V), TPS62240 (for 3.3 V), TPS71718(1.8 V)
Power supply specs:	
V _{in}	5 V ± 10%
V _{out1}	1.1 V/1.2 V ± 5% at 1000 mA
V _{out2}	1.8 V ± 5% at 80 mA
V _{out3}	3.3 V ± 5% at 200 mA
Sequencing	1) V _{out1} 2) V _{out2} and V _{out3}

TPS62240

- High-efficiency, step-down converter
- Output current up to 300 mA
- Power Save mode at light-load currents
- Allows <1-mm solution height

TPS62290

- High-efficiency, step-down converter
- Up to 1-A output current
- Power Save mode at light-load currents
- Output voltage accuracy in PWM mode ±1.5%

TPS71718

- 150-mA low-dropout regulator with Enable
- Low Noise: 30 μV typical (100 Hz to 100 kHz)
- Excellent load/line transient response
- Small SC70-5, 2-mm × 2-mm SON-6, and 1.5-mm × 1.5-mm SON-6 packages

More information on the devices can be found in the following data sheets.

1. *TPS62240/42/43, 2.25 MHz 300 mA Step Down Converter in 2x2SON/TSOT23 Package* data sheet ([SLVS762](#))
2. *TPS62290/91/93, 1-A Step Down Converter in 2 x 2 SON Package* data sheet ([SLVS764](#))
3. *TPS71718 (TPS717xx), Low Noise, High-Bandwidth PSRR Low-Dropout 150mA Linear Regulator* data sheet ([SBVS068](#))

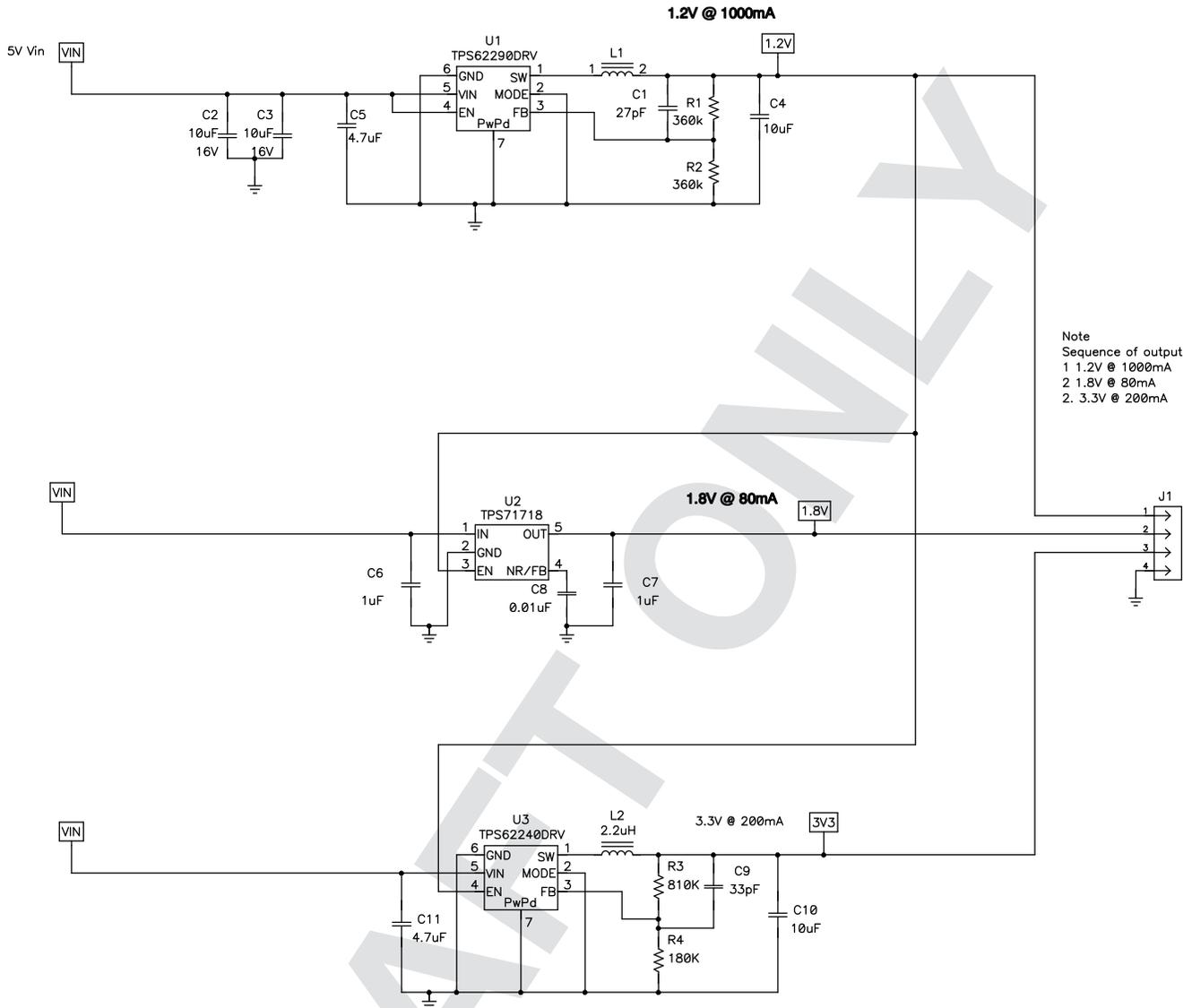


Figure 1. PMP4998 Reference Design Schematic

Proper sequencing is ensured in the design with the use of Enable pins. As required, Core 1.2 V at 1000 mA (TPS62290) comes first, which in turn enables the TPS62240 and TPS71718 devices. Hence, the required sequence is followed.

4 Bill of Materials

Table 3. PMP4998 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	27 pF	Capacitor, Ceramic, 0.01 µF, 10-V, X7R, 15%	0603	Std	TDK	5650
2	C2	10 µF	Capacitor, Ceramic, 16V, X7R, 20%	1206	C3216X7R1C106M T	TDK	15390
	C3	10 µF	Capacitor, Ceramic, 16V, X7R, 20%	1206	C3216X7R1C106M T	TDK	15390
1	C4	10 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C0603CH0J106k	TDK	5650
1	C5	4.7 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	C0603CH1A475K	TDK	5650
2	C6	1 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650

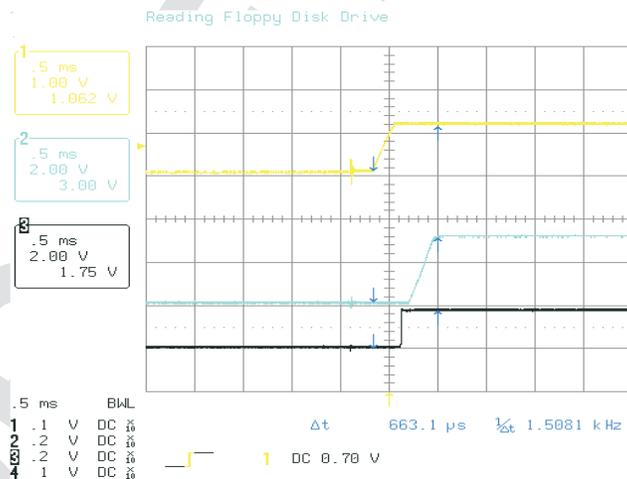
Table 3. PMP4998 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
	C7	1 μ F	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	C1608X5R1E105M	TDK	5650
1	C8	0.01 μ F	Capacitor, Ceramic, 50V, COG, 10%	0402	Std	Std	2800
1	C9	33 pF	Capacitor, Ceramic, 16V, X7R, 15%	0402	Std	TDK	2800
1	C10	10 μ F	Capacitor, Ceramic, 6.3V, X5R, 15%	0603	Std	TDK	5650
1	C11	4.7 μ F	Capacitor, Ceramic, 6.3V, X5R, 15%	0603	Std	TDK	5650
1	J1	PEC36SAAN	Header, Male 4-pin, 100mil spacing, (36-pin strip)	0.100 inch \times 4	PEC36SAAN	Sullins	50000
1	L1	2.2 μ H	Inductor, SMT, 2.1A, 0.110 Ω	0.118 \times 0.118 inch	LPS3015-222ML	Coilcraft	26,560
1	L2	2.2 μ H	Inductor, 1A, 200-m Ω	0.080 \times 0.080 inch	EPL2010-222ML	Coilcraft	108,300
2	R1	360k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R2	360k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R3	810K	Resistor, Chip, 1/16W, 1%	0402	Std	Std	2800
1	R4	180K	Resistor, Chip, 1/16W, 1%	0402	Std	Std	2800
1	U1	TPS62290DRV	IC, 1A xx V Step Down Converter	SON-6	TPS6229xDRV	TI	16416
1	U2	TPS71718	IC, 150mA, Low Iq, Wide Bandwidth, LDO Linear Regulators	SC70	TPS71718	TI	18600
1	U3	TPS62240DRV	IC, 2.25MHz 300mA Step-Down Converter	SON-6[DRV]	TPS62240DRV	TI	20736

- Notes:
1. These assemblies are ESD sensitive; ESD precautions shall be observed.
 2. These assemblies must be clean and free from flux and all contaminants. Failure to use clean flux is unacceptable.
 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
 4. Reference designators marked with an asterisk (***) cannot be substituted. All other components can be substituted with equivalent MFG's components.

5 Test Result

The start-up waveform is shown in [Figure 2](#), which specifies the sequencing order that is required.


Figure 2. Sequencing in Start-up Waveform

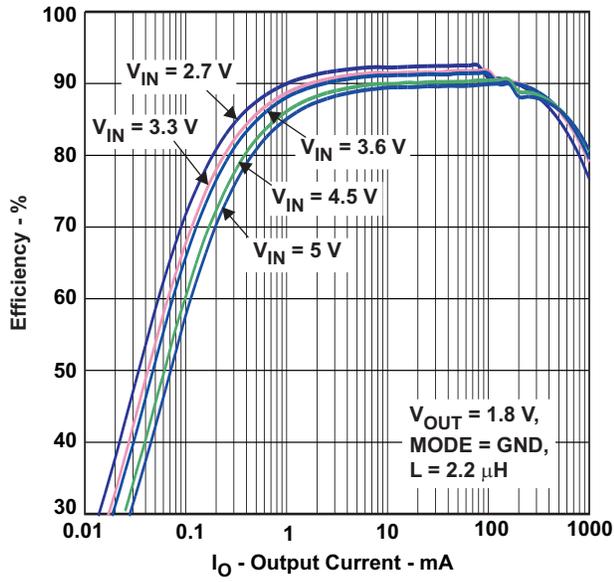


Figure 3. Efficiency vs Output Current, TPS62290

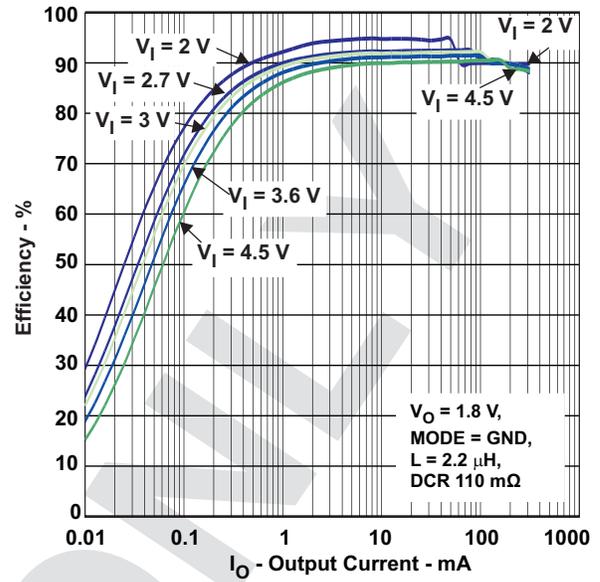


Figure 4. Efficiency vs Output Current, TPS62240

DRAFT

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