Application Note

Using the TPS62125 in an Inverting Buck-Boost Topology

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Low Power DC-DC Applications

ABSTRACT

The *TPS62125 3-V to 17-V, 300-mA Step-Down Converter With Adjustable Enable Threshold and Hysteresis* data sheet is a DCS-Control™ topology synchronous buck dc-to-dc converter designed for low-power applications. It features a wide operating input voltage range from 3 V to 17 V, 300-mA output current, and adjustable output voltage of 1.2 V to 10 V. This device is well-suited for applications such as ultra low-power microprocessors, energy harvesting, and low-power RF applications. Even though the TPS62125 can be configured in an inverting buck-boost topology, where the output voltage is inverted or negative with respect to ground. This application note describes the TPS62125 in an inverting buck-boost topology for use in low current negative rails for operational amplifier or optical module biasing and other low-power applications.

Note

The TPS62125 configured as an inverting buck-boost topology is risky. We highly recommend using TPS629203 family for inverting buck-boost applications.

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1 Inverting Buck-Boost Topology

1.1 Design Considerations

The TPS62125 for inverting buck-boost application is very risky. We strongly recommend using our new generation buck converter TPS629203 or -Q1 family (including TPS629206 or -Q1 and TPS629210 or -Q1) instead of the TPS62125 for inverting buck-boost applications. The TPS629203 family not only has a higher current limit threshold, but most importantly, it does not require the inductor current to fall to zero before starting a new switching cycle. For example TPS629203 family has 0.9A typ. low-side current limit threshold, thus, the device will continue to switch as long as the DC bias current of downstream circuitry is below this 0.9A typ. threshold. More detailed information for TPS629203 inverting buck-boost application can be found in Using the TPS629210-Q1 in an Inverting Buck-Boost Topology.

The TPS62125 integrates a high-side MOSFET current limit I_{LIMF} to protect the device against over current or short circuit fault. The current in high-side MOSFET is monitored by current limit comparator and once the current reaches the limit of I_{LIMF}, the high-side MOSFET is turned off and low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET is turned on again once **zero** current comparator trips and the inductor current has become **zero**.

The inverting buck-boost application is most commonly used to drive differential (+V/-V) rails. At some scenarios, the downstream devices become active as soon as the input voltage is present, their Iq current feeds into the negative (-V) rail even if the negative (-V) rail is not being enabled. There is a positive DC bias voltage is likely existed on the negative (-V) rail, then TPS62125 is more prone to get stuck as it may never see a zero-crossing current while getting into an over current fault due to this positive DC bias voltage.

A possible workaround solution for TPS62125 in inverting buck-boost application: Adjust the system power up sequence to prevent the downstream devices from loading the negative (-V) rail prior to the negative rail being enabled. That means to enable the negative (-V) rail first and then enable other downstream devices. Otherwise, TPS62125 probably gets stuck during power up.

1.2 Concept

The inverting buck-boost topology is very similar to the buck topology. In the buck configuration shown in Figure 1-1, the positive connection (V_{OUT}) is connected to the inductor and the return connection is connected to the integrated circuit (IC) ground. However, in the inverting buck-boost configuration shown in Figure 1-2, the IC ground is used as the negative output voltage pin (labeled as $-V_{OUT}$). What used to be the positive output in the buck configuration is used as the ground (GND). This inverting topology allows the output voltage to be inverted and always lower than the ground.

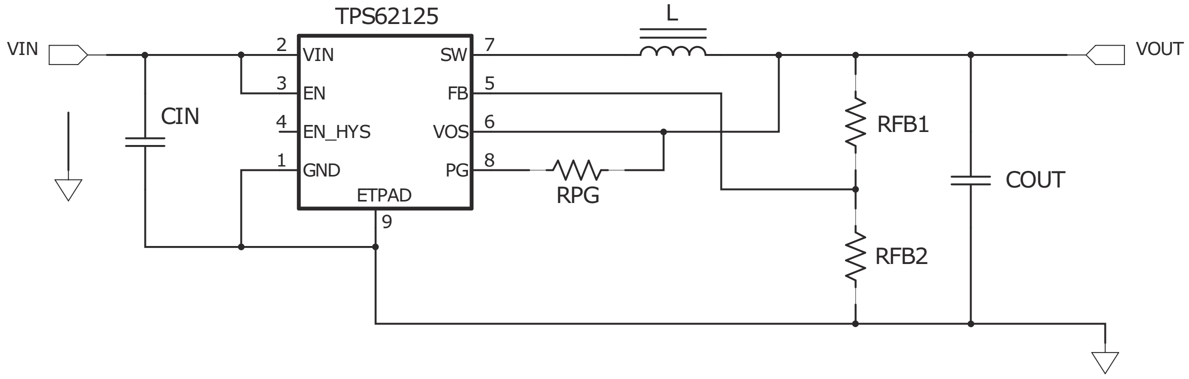


Figure 1-1. TPS62125 Buck Topology

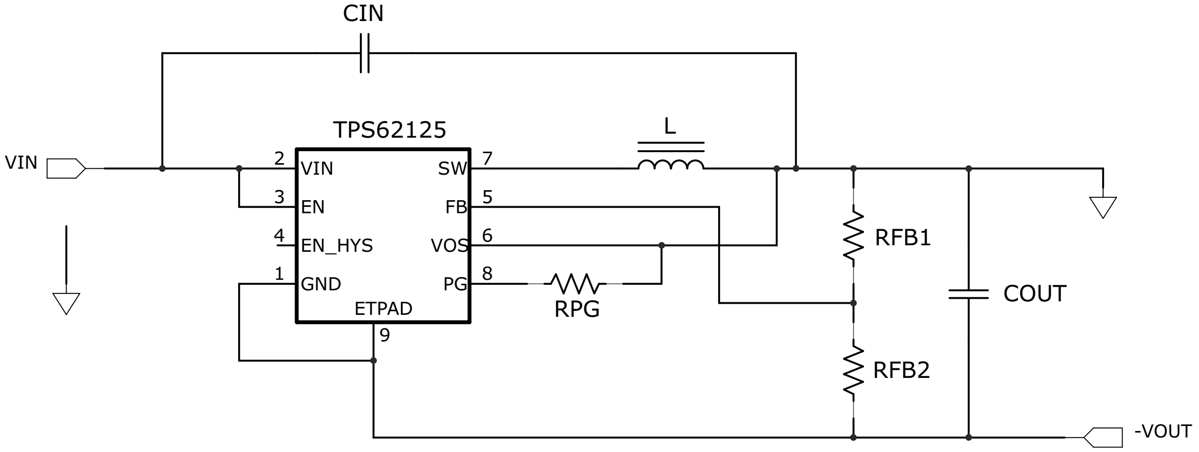


Figure 1-2. TPS62125 Inverting Buck-Boost Topology

The circuit operation is different in the inverting buck-boost topology than in the buck topology. Figure 1-3 **(a)** illustrates that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in Figure 1-3 **(b)**, the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in Figure 1-3 **(c)**, the inductor provides current to the load and the output capacitor. These changes affect many parameters as described in the upcoming sections.

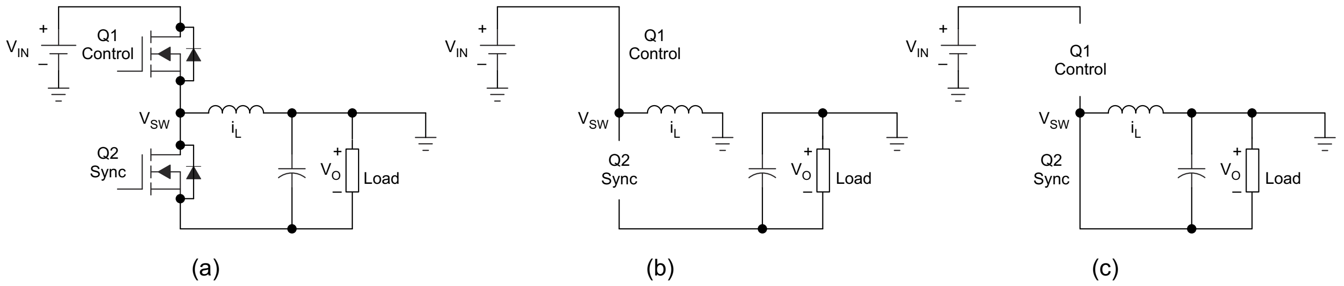


Figure 1-3. Inverting Buck-Boost Configuration

1.3 Output Current Calculations

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck-boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output cap and the load (see Figure 1-3). Knowing that the off time is 1 – D of the switching period, then the average inductor current is:

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} \tag{1}$$

The duty cycle for the typical buck converter is simply V_{OUT} / V_{IN} but the duty cycle for an inverting buck-boost converter becomes:

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN})} \tag{2}$$

Finally, the maximum inductor current becomes:

$$I_{L(Max)} = I_{L(Avg)} + \frac{\Delta I_{L(Max)}}{2} \tag{3}$$

Where,

D: Duty cycle

ΔI_L (A): Peak to peak inductor ripple current

V_{IN} (V): Input voltage with respect to ground, instead of IC ground or $-V_{OUT}$.

The TPS62125's current limit technique allows a simple maximum output current calculation. If the current exceeds I_{LIMF} (the high-side MOSFET current limit), the high-side MOSFET switch turns off and the low-side MOSFET switch turns on until the inductor current ramps down to 0. If an overload is still present after reaching 0 current, the low-side MOSFET switch turns off and the high-side MOSFET switch turns on until current limit is reached again. In current limit, the inductor's current goes from I_{LIMF} to 0—its ripple current becomes I_{LIMF}. Operating the TPS62125 in this state (with $I_{L(Max)}$ equal to $\Delta I_{L(Max)}$ equal to I_{LIMF}) reduces the average inductor current to ½ I_{LIMF} (from Equation 3). With the TPS62125's minimum current limit value of 600 mA, this gives an $I_{L(Avg)}$ of 300 mA when current limit is reached. With this, the maximum allowable output current is calculated from Equation 1 and Equation 2, with a 5-V input voltage to –5-V output voltage system as an example:

$D = -5 / (-5 - 5) = 0.5$

This result is then used in Equation 1:

$I_{OUT} = I_{L(Avg)} \times (1 - D) = 300 \times (1 - 0.5) = 150$ mA

Due to increased duty cycles when operating at either lower input voltages (≤ 5 V) or with higher ambient temperatures (for example, at 85°C), the duty cycle used for the maximum output current calculation above should be increased by 10% for these conditions. This provides a more accurate maximum output current calculation. For the given example of a 5-V input and –5-V output, the maximum output current is then 300 x (1 - 0.6) = 120 mA.

The maximum output current for –5-V, –3.3-V and –8-V output voltages at different input voltages is displayed in Figure 1-4 and accounts for the above duty cycle increase for lower input voltages. Operation at higher temperatures would decrease the maximum output current shown for input voltages above 6 V as well.

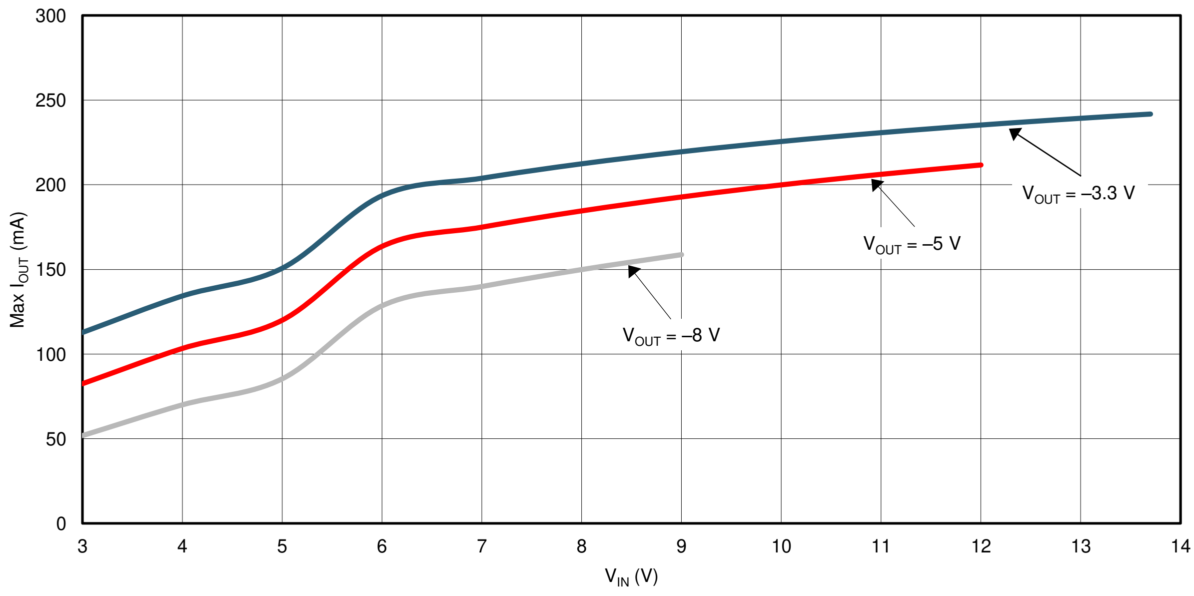


Figure 1-4. Maximum Output Current versus Input Voltage

1.4 V_{IN} and V_{OUT} Range

The input voltage that can be applied to an IC operating in the inverting buck-boost topology is less than the input voltage for the same IC operating in the buck topology. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range of the TPS62125 is 3 V to 17 + V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck-boost topology should be set between –1.2 V and –10 V. It is set the same way as in the buck configuration, with two resistors connected to the FB pin.

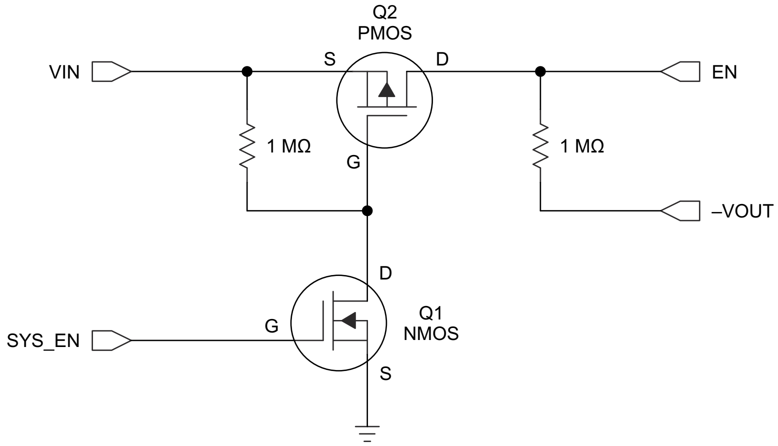
2 Digital Pin Configurations

2.1 Enable Pin

The device is enabled once the voltage at the EN pin trips its threshold and the input voltage is above the UVLO threshold. The TPS62125 stops operation once the voltage on the EN pin falls below its threshold or the input voltage falls below the UVLO threshold.

Because V_{OUT} is the IC ground in this configuration, the EN pin must be referenced to V_{OUT} instead of ground. In the buck configuration, 1.2 V is considered a high and less than 1.15 V is considered a low. In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 1.2 V + V_{OUT} and the low threshold is 1.15 V + V_{OUT}. For example, if V_{OUT} = –5 V, then V_{EN} is considered at a high level for voltages above –3.8 V and a low level for voltages below –3.85 V.

This behavior can cause difficulties enabling or disabling the part, since in some applications, the IC providing the EN signal may not be able to produce negative voltages. The level shifter circuit shown in Figure 2-1 alleviates any difficulties associated with the offset EN threshold voltages by eliminating the need for negative EN signals. If disabling the TPS62125 is not desired, the EN pin may be directly connected to V_{IN} without this circuit.



VOUT is the negative output voltage of the inverting buck-boost converter

Figure 2-1. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 sees 0 V across its V_{GS} and also remains off. In this state, the EN pin sees –5 V which is below the low-level threshold and disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (V_{GS} threshold as specified in the MOSFET datasheet), the gate of Q2 sees ground through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. Now, V_{IN} ties to EN through Q2 and the pin is above the high-level threshold, turning the device on. Be careful to ensure that the V_{GD} and V_{GS} of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs.

The enable and disable sequence is illustrated in Figure 2-2 and Figure 2-3. The SYS_EN signal activates the enable circuit, and the G/D Node signal represents the shared node between Q1 and Q2. This circuit was tested with a 5-V SYS_EN signal and dual N/PFET Si1029X. The EN signal is the output of the circuit and goes from V_{IN} to V_{OUT} properly enabling and disabling the device. The PG pin was used as an output discharge to accelerate V_{OUT}'s return to 0V, when the IC is disabled.

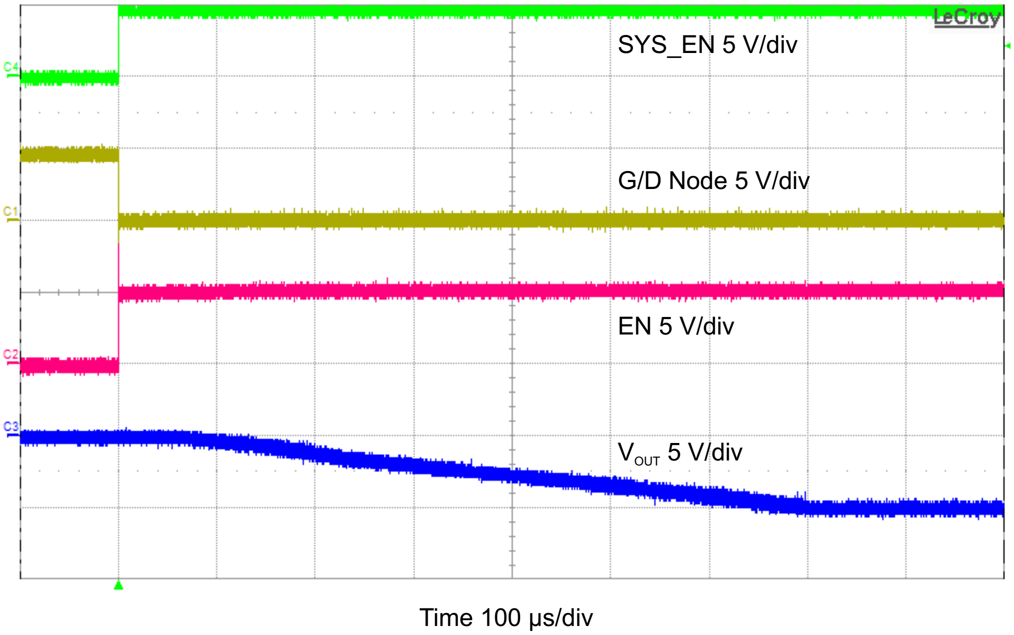


Figure 2-2. Enable Sequence

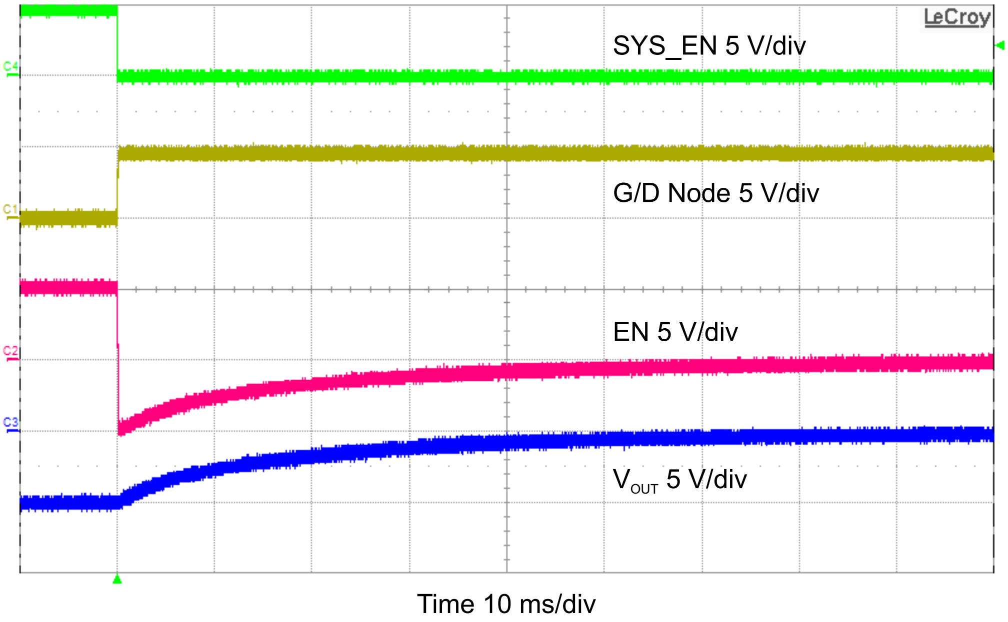


Figure 2-3. Disable Sequence

2.2 Enable Hysteresis Pin

The enable comparator typically has a built-in hysteresis of 50 mV. This hysteresis can be increased with an external resistor divider connected to the EN_hys pin. The equations to calculate the external resistor values for a buck converter are located in the applications section of the data sheet (Equations 6–10). Because the device is now an inverting buck-boost converter, the equations must be modified to account for V_{OUT}, which is the GND terminal of the device. The $V_{EN\_TH\_ON}$ variable remains the same since there is usually no negative output voltage when the part is enabled. The equations for the inverting buck-boost topology are:

$$V_{IN\_startup} = V_{EN\_TH\_ON} \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) = 1.2\text{ V} \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right) \quad (4)$$

$$V_{IN\_stop} = V_{EN\_TH\_OFF} \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}}\right) + V_{OUT} = 1.15\ V \times \left(1 + \frac{R_{EN1}}{R_{EN2} + R_{EN\_hys}}\right) + V_{OUT} \quad (5)$$

In order for the V_{IN_stop} threshold to operate, $V_{IN\_startup}$ must be greater than V_{IN_stop} - V_{OUT}, where V_{OUT} is a negative value.

If the EN_hys pin is not being used to adjust the hysteresis, it can instead be used to provide an output discharge path (explained in Section 2.4).

2.3 Power Good Pin

The TPS62125 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because V_{OUT} is the IC ground in this configuration, the PG pin is referenced to V_{OUT} instead of ground, which means that the TPS62125 pulls PG to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin may not be able to withstand negative voltages. The level shifter circuit shown in Figure 2-4 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it may be left floating or connected to V_{OUT} without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 6 V above the negative output voltage (IC ground).

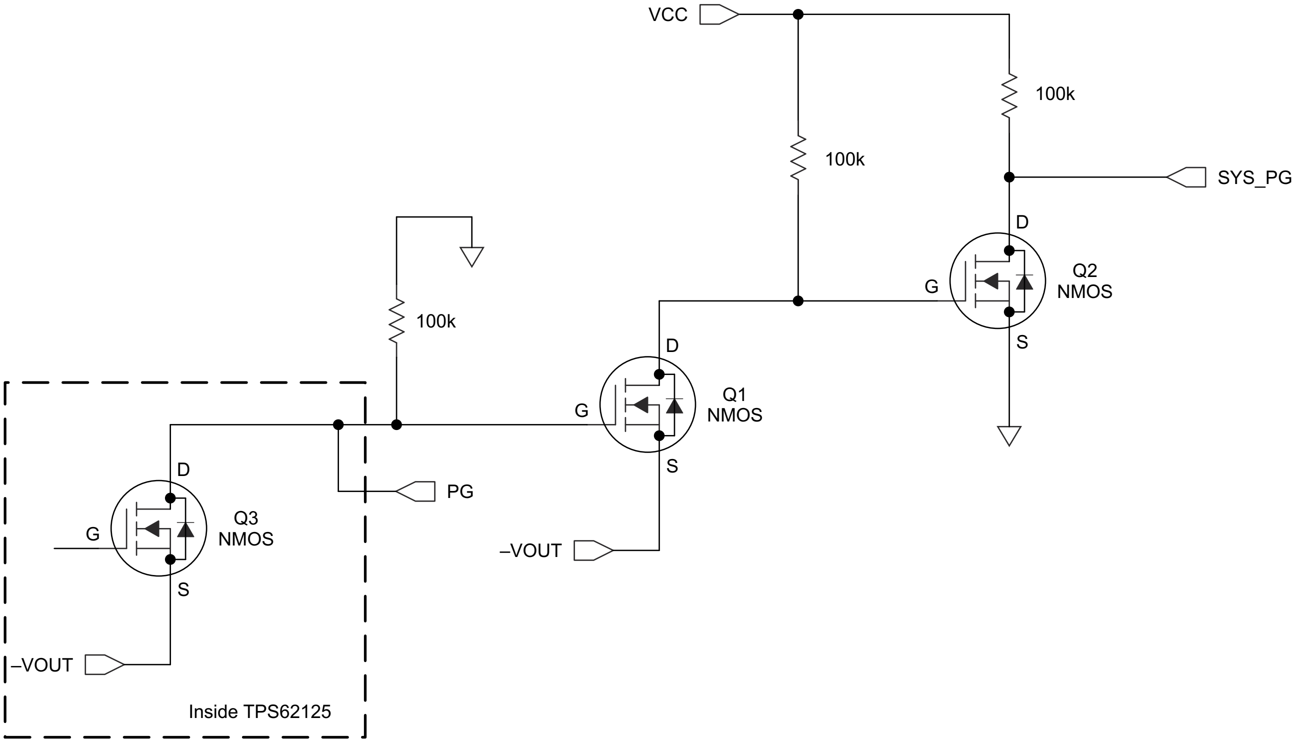


Figure 2-4. PG Pin Level Shifter

Inside the TPS62125, the PG pin is connected to an N-channel MOSFET (Q3). By tying the PG pin to the gate of Q1, when the PG pin is pulled low, Q1 is off and Q2 is on because its V_{GS} sees V_{CC}. SYS_PG is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG net.

This PG pin level shifter sequence is illustrated in Figure 2-5 and Figure 2-6. The PG signal activates the PG pin level shifter circuit, and the G/D Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 5 V and dual NFET Si1902DL. The SYS_PG net is the output of the circuit and goes between ground and 5 V, and is easily read by a separate device. The EN_hys pin was used to accelerate V_{OUT}'s return to 0V, when the IC is disabled.

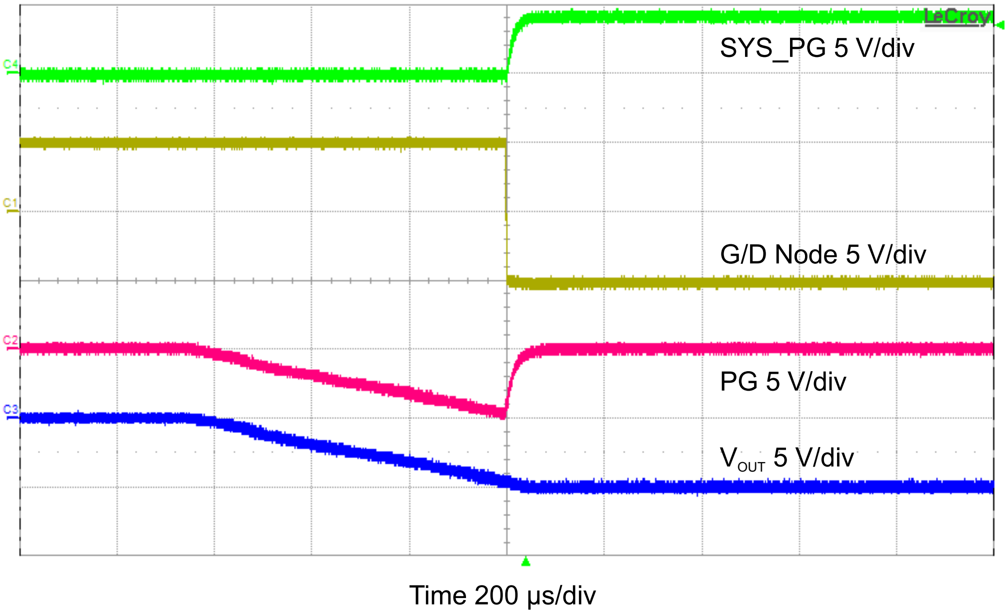


Figure 2-5. PG Pin Level Shifter on Startup

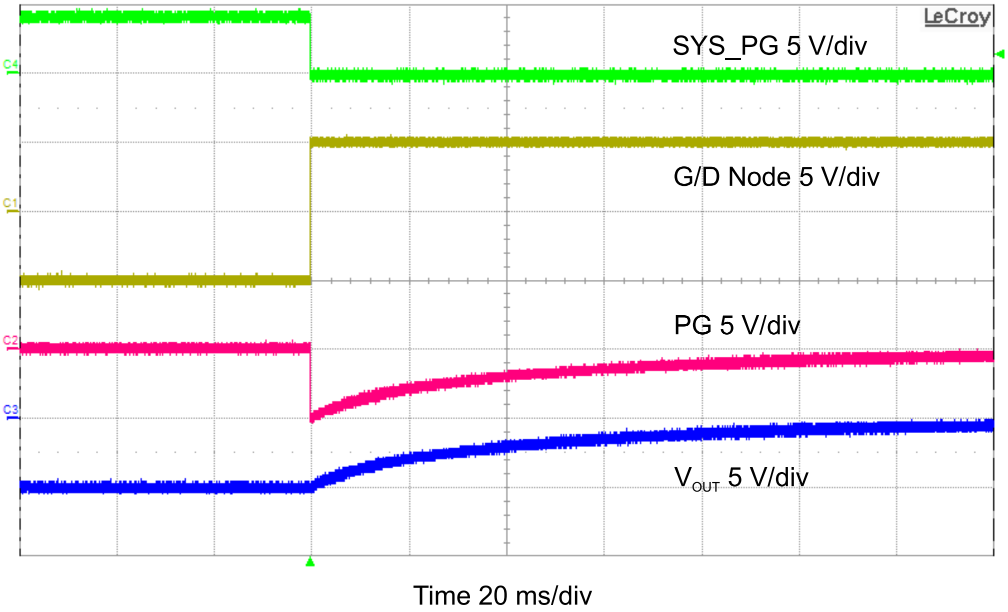


Figure 2-6. PG Pin Level Shifter on Shutdown

2.4 Discharging the Output Voltage

If the TPS62125 is disabled in a light-load or no-load condition, the PG or EN_hys pins can accelerate V_{OUT}'s return to 0 V by providing an additional discharge path. When the IC is disabled via the EN pin, the PG and EN_hys pins are connected to the device ground (V_{OUT}) through an internal MOSFET. Placing a resistor between ground and the PG or EN_hys pins creates a discharge path to ground. If the EN_hys pin is already being used to adjust the enable thresholds, do not use this pin as a discharge path. If the PG pin is already being used, do not use this pin as a discharge path.

The added resistor should be sized to limit the current into the PG or EN_hys pin to a safe level. The PG output typically has an internal resistance of 600 Ω and a 400-Ω minimum. The maximum sink current into the PG pin is

10 mA. In order to limit the discharge current to the maximum allowable sink current into the PG pin, an external resistor is calculated using:

$$R = (-V_{OUT} / I_{PG\_MAX}) - R_{PG\_MIN} = (-V_{OUT} / 0.01\ A) - 400\ \Omega \quad (6)$$

Use a 100-Ω resistor for a –5-V output. Figure 2-7 and Figure 2-8 illustrate the purpose of the PG/EN_hys pin discharge path – the output voltage returns to 0 V quicker with the discharge circuit.

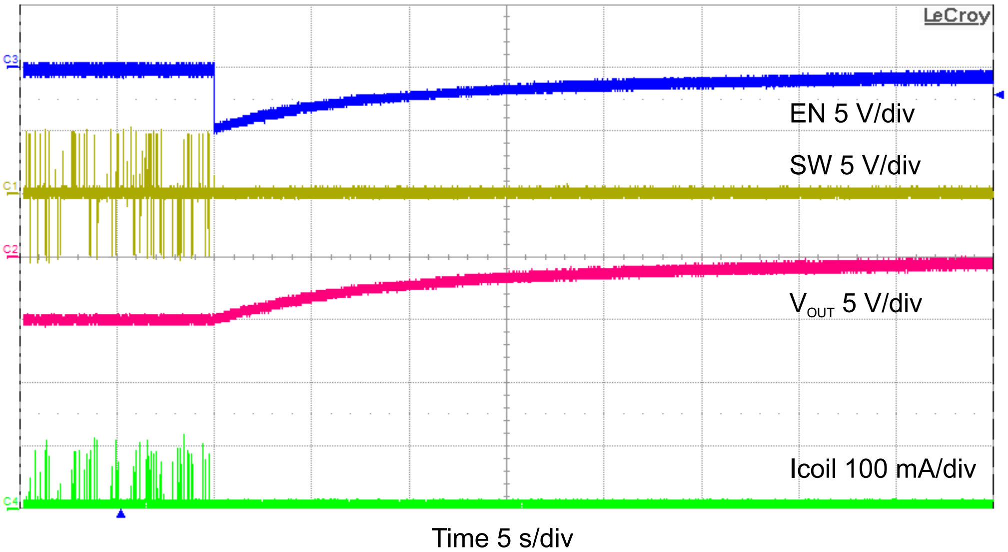


Figure 2-7. Shutdown at No Load and No PG Pin Discharge

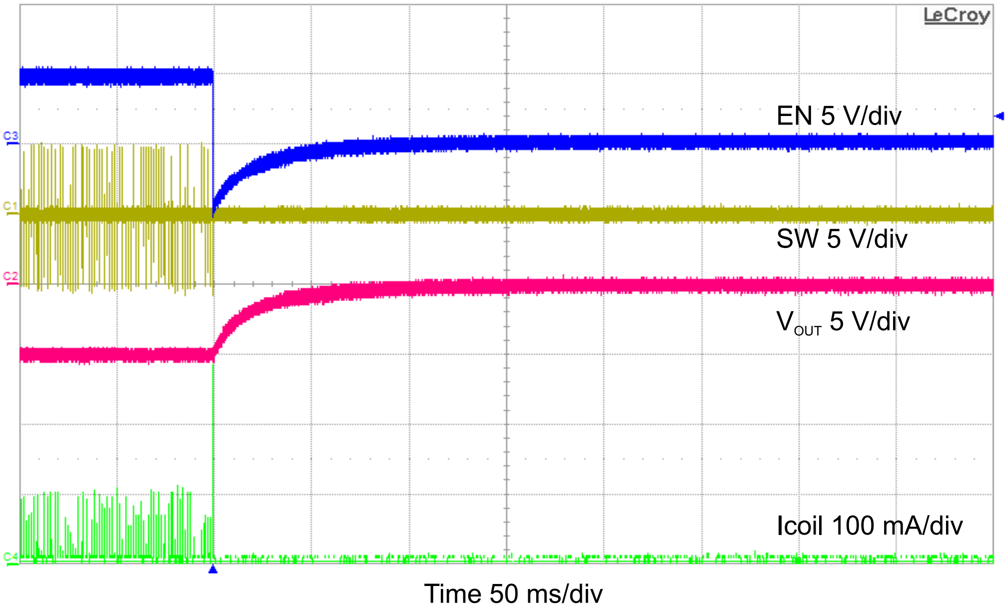


Figure 2-8. Shutdown at No Load and PG Pin Discharge of 100 Ohm

3 Startup Behavior and Switching Node Consideration

Figure 3-1 shows the startup behavior in the inverting configuration. After EN is taken high, the device starts switching after about a 50-μs delay. Due to the higher peak currents in the inverting topology, current limit is frequently reached during startup. This is acceptable as long as the saturation current of the inductor is chosen appropriately.

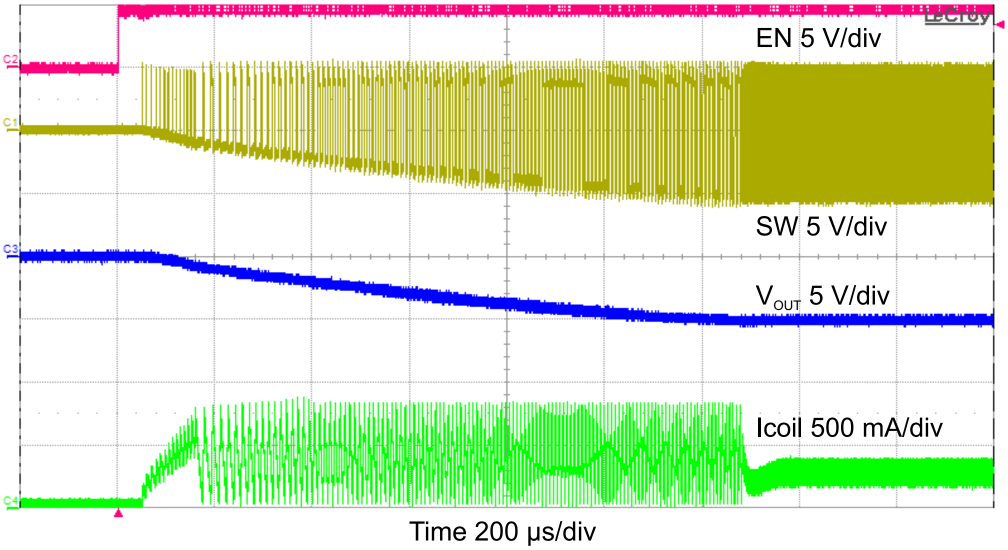


Figure 3-1. Startup Behavior in the Inverting Configuration with V_{IN} = 5 V and 120-mA load

Figure 3-1 also shows the SW node voltage as the device starts up. The voltage on the SW pin switches from V_{IN} to V_{OUT}. As the high-side MOSFET turns on, the SW node sees the input voltage and as the low-side MOSFET turns on, the SW node sees the IC ground, which is the output voltage. As V_{OUT} continues to ramp down, the SW node low level follows it down.

4 External Component Selection

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See Section 4.3 for a discussion of stability.

4.1 Inductor Selection

When selecting the inductor value for the inverting buck-boost topology, the equations provided in Output Current Calculations should be used instead of the ones provided in the data sheet. ($I_{L(max)}$ should be kept below the minimum current limit value of the device (0.6 A) for a reliable design.) It is recommended to size the inductor for the current limit level of the TPS62125, as this level is sometimes reached during startup (shown in Figure 3-1). See Section 4.3 for the stability impact of the inductor selection.

4.2 Input Capacitor Selection

An input capacitor, C_{IN}, is required to provide a local bypass for the input voltage source. A low ESR, X5R or X7R ceramic capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 10-µF ceramic capacitor is recommended from V_{IN} to ground (system ground, not $–V_{OUT}$). The C_{IN} capacitor value can be increased without any limit for better input voltage filtering.

For the inverting buck-boost configuration of the TPS62125, it is not recommended to install a capacitor from V_{IN} to V_{OUT}. Such a capacitor, if installed, provides an AC path from V_{IN} to V_{OUT}. When V_{IN} is applied to the circuit, this dV/dt across a capacitor from V_{IN} to V_{OUT} creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS62125 and is not recommended. Therefore, a capacitor from V_{IN} to V_{OUT} is not needed or recommended. If such a capacitor (CBP) is present, then a Schottky diode should be installed on the output, per Figure 4-1. Startup testing should be conducted to ensure that the VOS pin is not driven more than 0.3 V below IC ground when V_{IN} is applied.

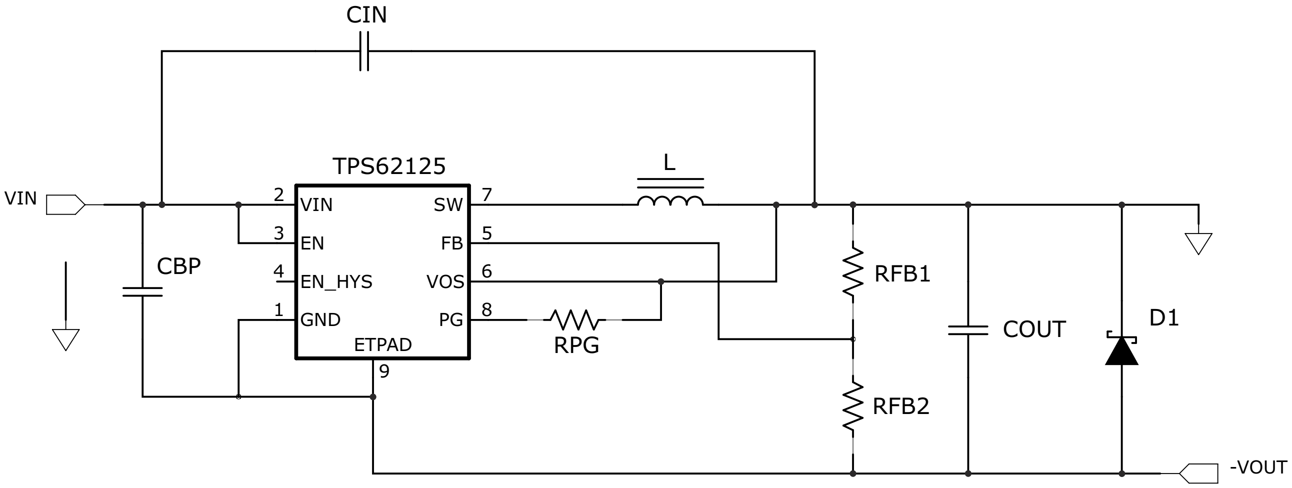


Figure 4-1. If Installing CBP, Installing Schottky D1 is Required

The AC path through CBP might also worsen the line transient response. If strong line transients are expected, the output capacitance should be increased to keep the output voltage within acceptable levels during the line transient.

4.3 Selecting L and C_{OUT} for Stability

The switch node, inductor current, and the output voltage ripple during steady state are signals that need to be checked first for the stability of the system. Oscillations on the output voltage or the inductor current as well as jitter on the switch node are good indicators of the instability of the system. Figure 5-7 shows both the switch node and output voltage ripple of this topology. Load transient response is another good test for stability, as described in the *Simplifying Stability Checks* application note.

The recommended nominal inductor and output capacitor values to use for this topology are in the range of 15 µH to 22 µH and from 22 µF to 100 µF, respectively. In this application note, a 22-µH inductor and 2 x 22-µF capacitors are used.

The inverting buck-boost topology contains a Right Half Plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. This can cause instability. Equation 7 estimates the frequency of the RHP zero.

$$f_{(RHP)} = \frac{-(1-D)^2 \times V_{OUT}}{(D \times L \times I_{OUT} \times 2 \times \pi)} \tag{7}$$

It is recommended to keep the loop crossover frequency to, at most, 1/4th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. *How to Measure the Control Loop of DCS-Control™ Devices* application note explains how to measure the control loop of a DCS-Control™ device while Figure 4-2 shows the bode plot of Figure 5-1.

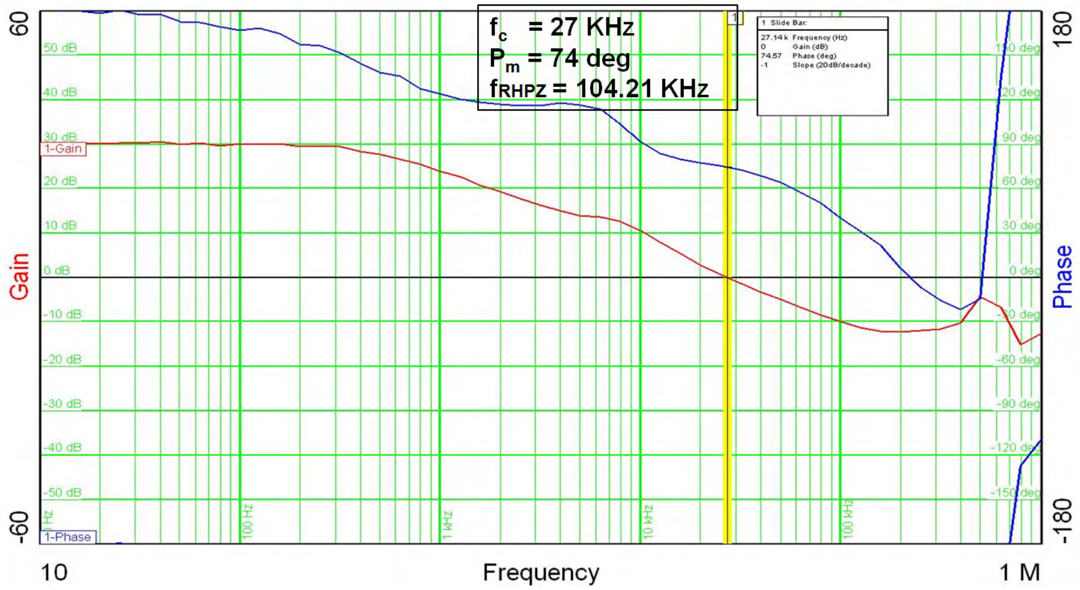


Figure 4-2. Bode Plot with V_{IN} = 5 V and 120-mA Load

5 Typical Performance and Waveforms

The application circuit shown in Figure 5-1 is used to generate the data presented in Figure 5-2 – Figure 5-7. To reach the total effective capacitance of 22 μF, the design used 2 x 22-μF Murata [GRM21BR61A226ME44L] capacitors, 2 × 22-μF Samsung [CL21A226MAQNNNE] capacitors, or 3 × 10-μF TDK [C2012X7R0J106K125AB] capacitors. For a 5-V output, loss of capacitance from the DC bias effect can be significant. Unless otherwise specified, V_{IN} = 5 V and V_{OUT} = –5 V. The inductor used in the tested circuit is a 22-μH Coilcraft [LPS5030-223].

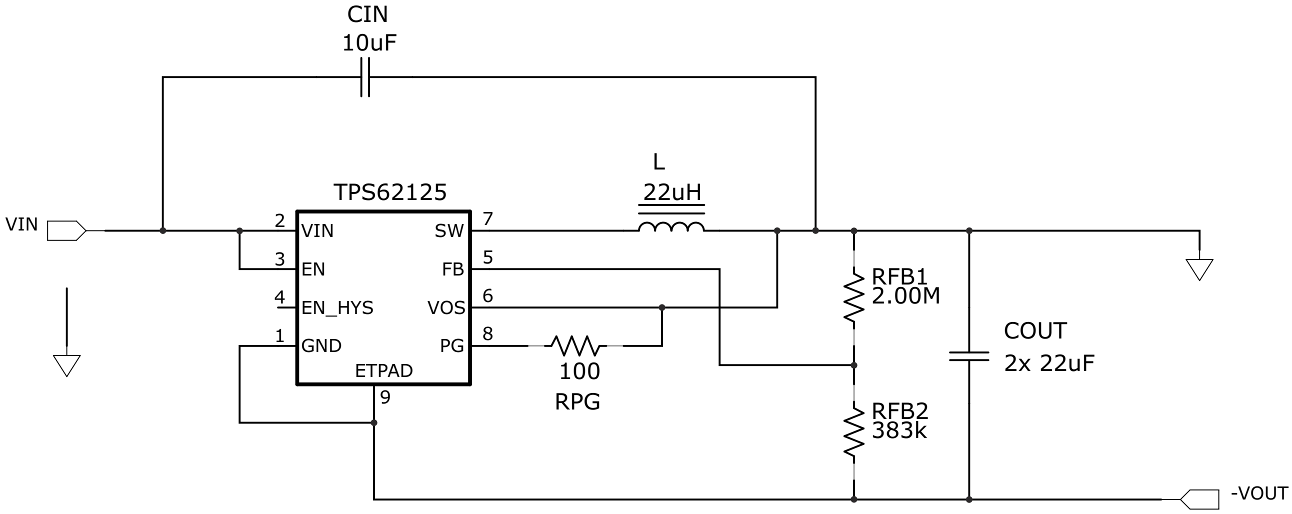


Figure 5-1. Schematic of the Tested Circuit

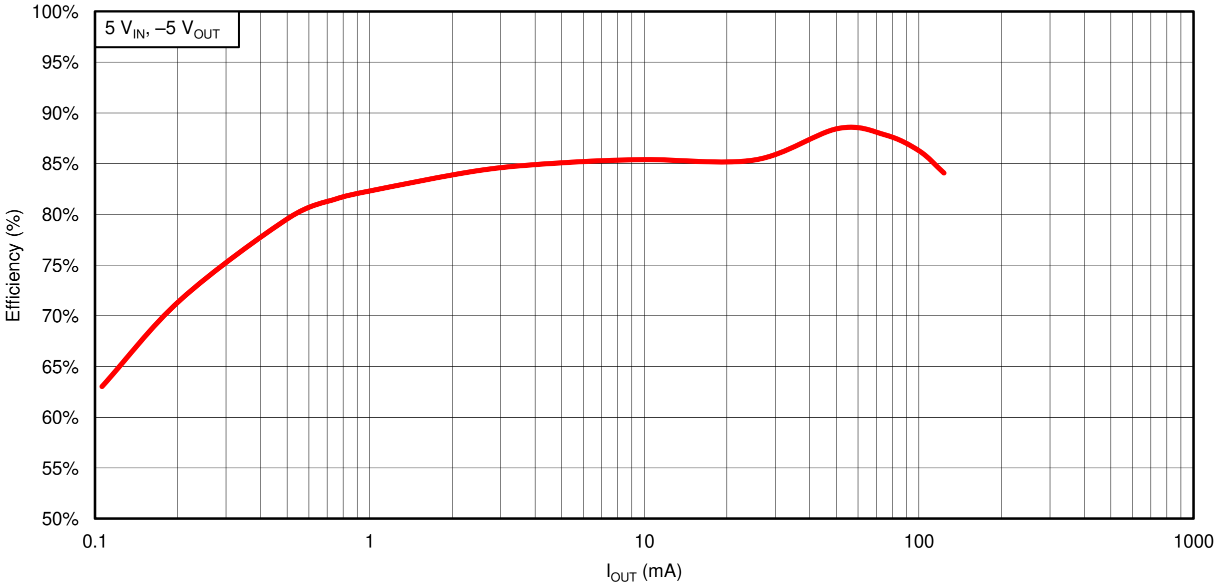


Figure 5-2. Efficiency vs. Load Current with V_{OUT} = –5 V

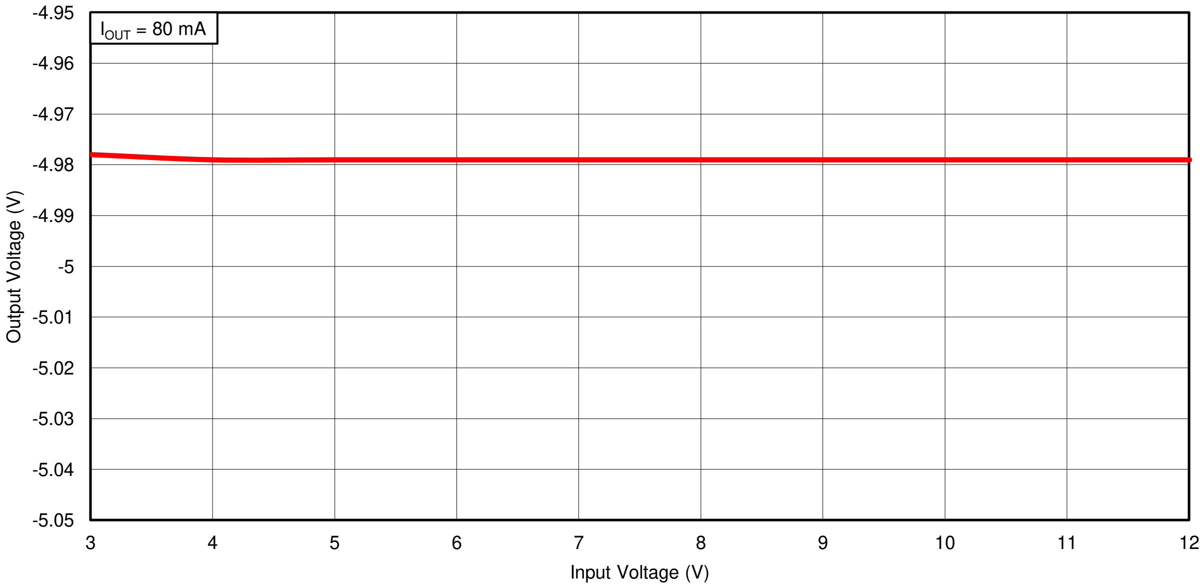


Figure 5-3. Line Regulation

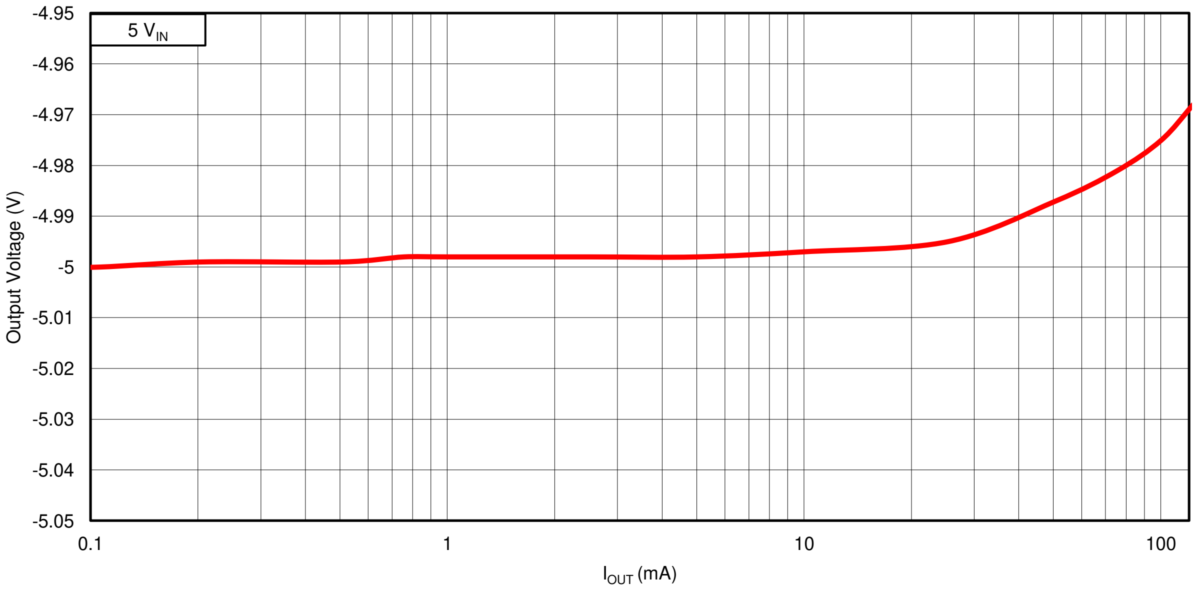


Figure 5-4. Load Regulation

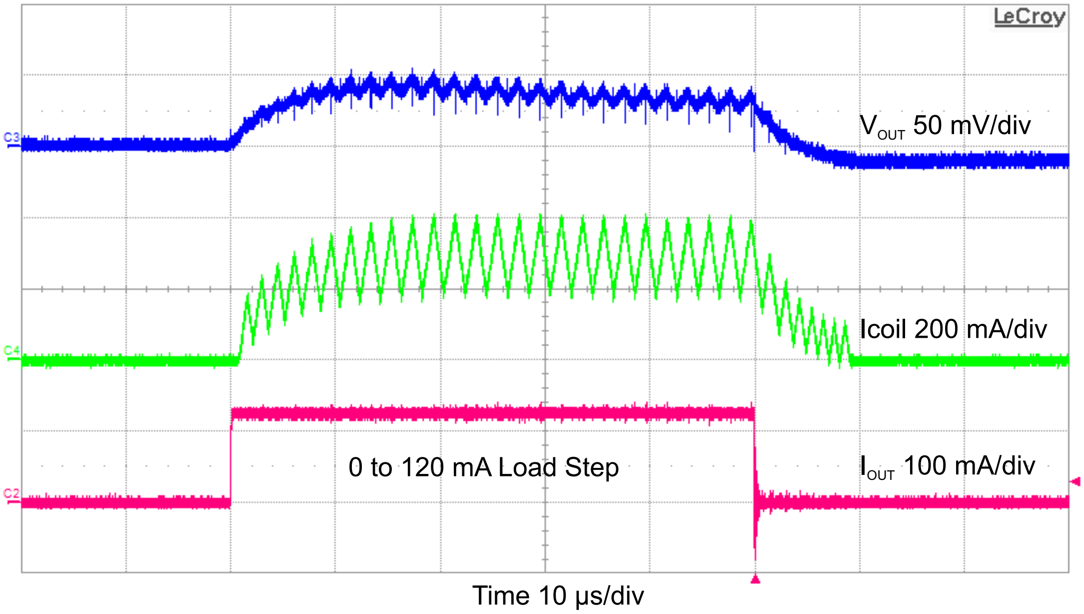


Figure 5-5. Load Transient Response with V_{IN} = 5 V

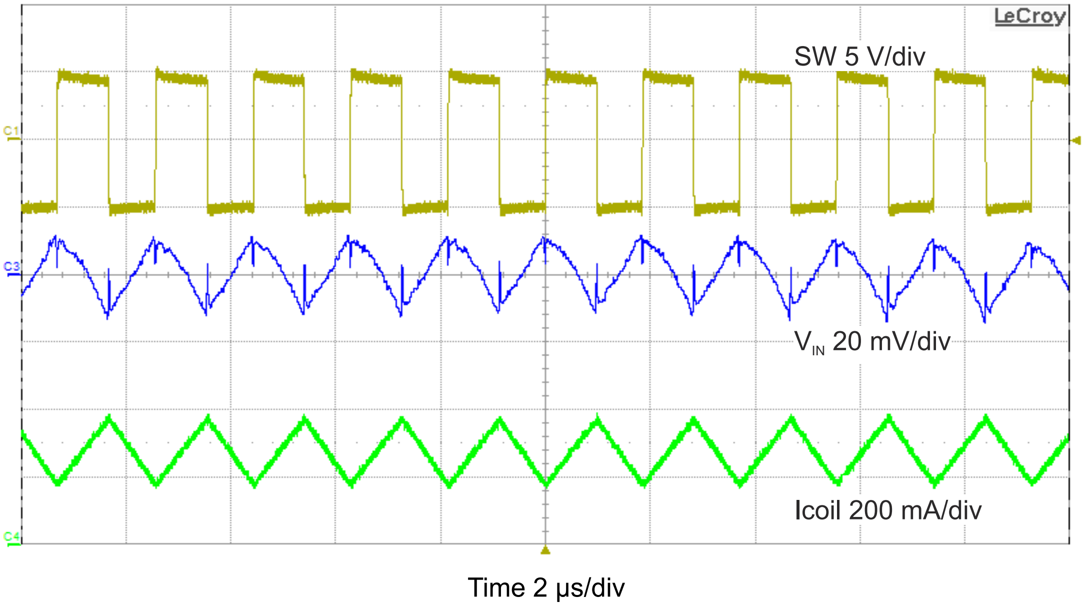


Figure 5-6. Input Voltage Ripple with V_{IN} = 5 V and 120-mA Load

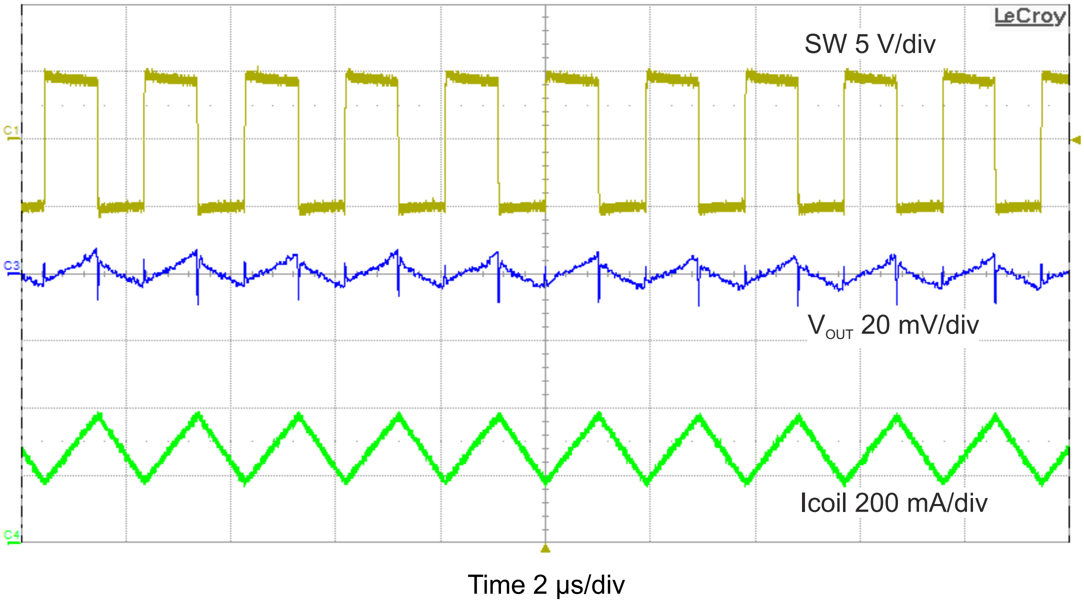


Figure 5-7. Output Voltage Ripple with V_{IN} = 5 V and 120-mA Load

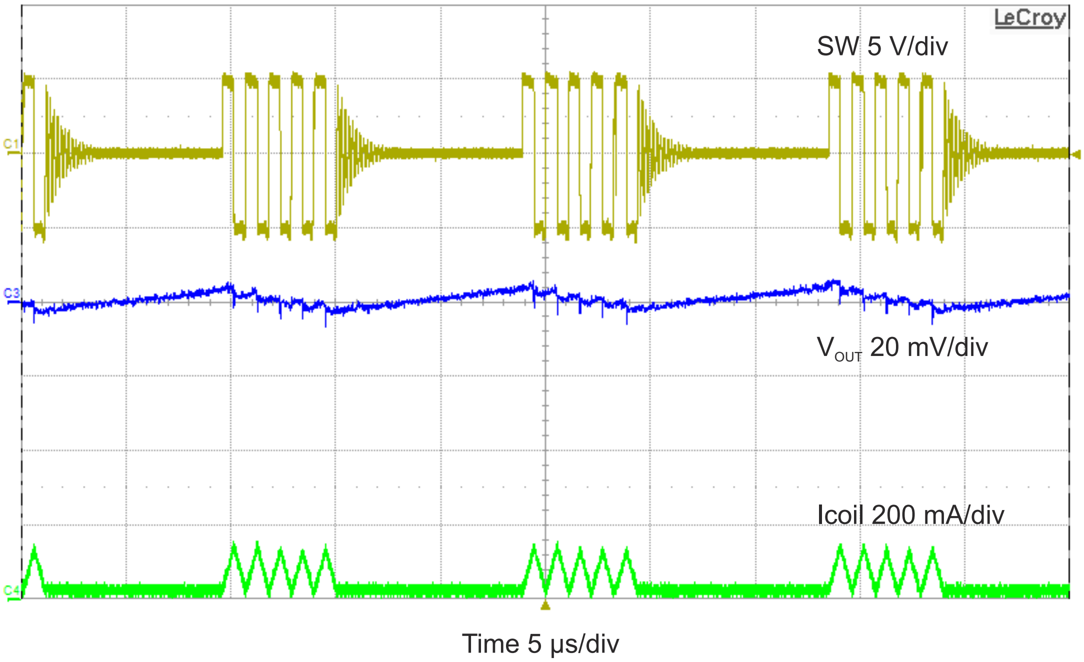


Figure 5-8. Output Voltage Ripple with V_{IN} = 5 V and 10-mA Load

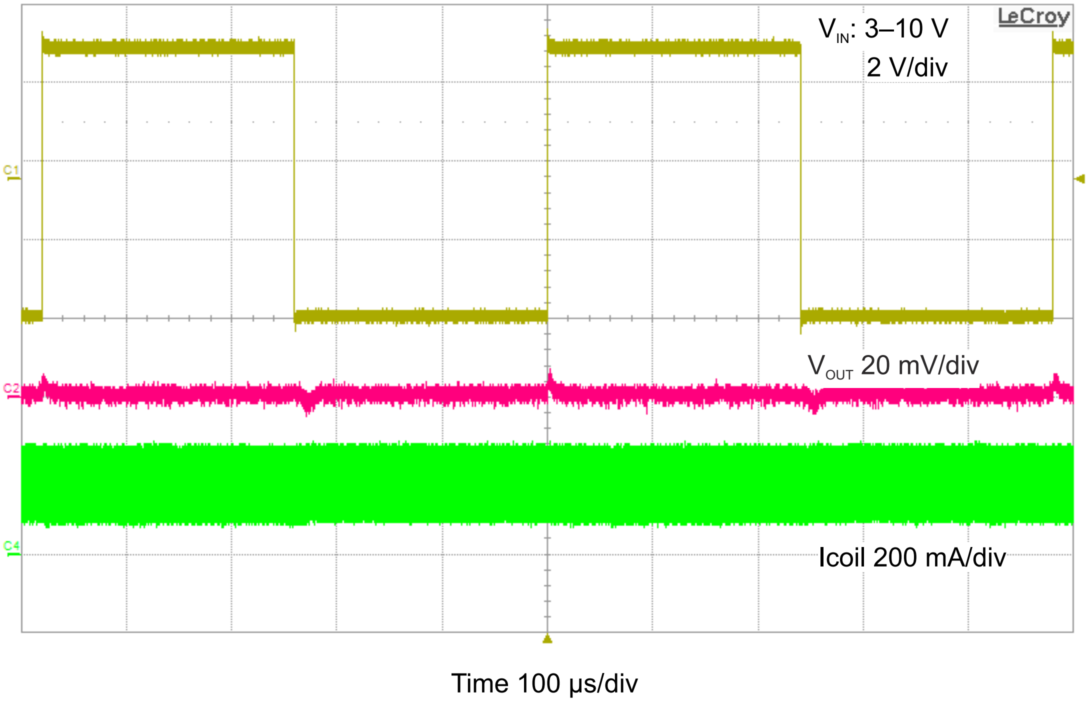


Figure 5-9. Line Transient Response with 120-mA Load

6 Conclusion

Even if the TPS62125 can be configured as an inverting buck-boost converter to generate a negative output voltage. But we don't recommend TPS62125 for inverting buck-boost applications. The detailed explanation is in section 1.1 Design Considerations. The inverting buck-boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck-boost topology and how to select the external components with the changed system characteristics. Measured data from the example design are provided.

7 References

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3. Texas Instruments, *Using a Buck Converter in an Inverting Buck-Boost Topology* analog design journal
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6. Texas Instruments, *Simplifying Stability Checks* application note
7. Robert W. Erickson: *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 1997
8. Texas Instruments, *How to Measure the Control Loop of DCS-Control™ Devices* application note
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8 Revision History

Changes from Revision B (July 2014) to Revision C (December 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.................. 1
- Added Design Consideration topic for inverting buck-boost application issue.. 3

Changes from Revision A (September 2013) to Revision B (June 2014) **Page**

- Updated abstract text.. 1
- Updated descriptions of both figures in the first paragraph of the Concept topic.. 3
- Updated *TPS62125 Buck Topology* and *TPS62125 Inverting Buck-Boost Topology* figures............................. 3
- Updated *Inverting Buck-Boost Configuration* figure.. 3
- Updated equations in *Output Current Calculations* section... 4
- Updated *Maximum Output Current versus Input Voltage* figure, Maximum Output Current versus V_{IN} 4
- Updated *Digital Pin Configurations* section; headings, text, equations, and images... 7
- Updated *External Component Selection* topic.. 13
- Updated *Typical Performance and Waveforms* topic.. 15
- Added Output Voltage Ripple V_{IN} = 5 V and 10-mA Load image.. 15
- Added references to the *References* section.. 21

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