TEXAS INSTRUMENTS

TPS54611, TPS54612, TPS54613
TPS54614, TPS54615, TPS54616

SLVS400D – AUGUST 2001 – REVISED JANUARY 2015

# TPS5461x 3-V to 6-V Input, 6-A Output Synchronous Buck PWM Switcher With Integrated FETs (SWIFT™)

## 1 Features

- 30-mΩ, 12-A Peak MOSFET Switches for High Efficiency at 6-A Continuous Output Source and Sink
- 0.9-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V Fixed Output Voltage Devices With 1.0% Initial Accuracy
- Internally Compensated for Easy Use and Minimal Component Count
- Fast Transient Response
- Wide PWM Frequency − Fixed 350 kHz, 550 kHz or Adjustable 280 kHz to 700 kHz
- Load Protected by Peak Current Limit and Thermal Shutdown
- Integrated Solution Reduces Board Area and Total Cost

## 2 Applications

- Low-Voltage, High-Density Systems With Power Distributed at 5 V or 3.3 V
- Point of Load Regulation for High Performance DSPs, FPGAs, ASICs and Microprocessors
- Broadband, Networking and Optical Communications Infrastructure
- Portable Computing/Notebook PCs

## 3 Description

The SWIFT™ family of dc/dc regulators, the TPS54611, TPS54612, TPS54613, TPS54614, TPS54615 and TPS54616 low-input voltage high-output current synchronous-buck PWM converters integrate all required active components. Included on the substrate are true, high-performance, voltage error amplifiers that provide high performance under transient conditions; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a powergood output useful for processor/logic reset, fault signaling, and supply sequencing.

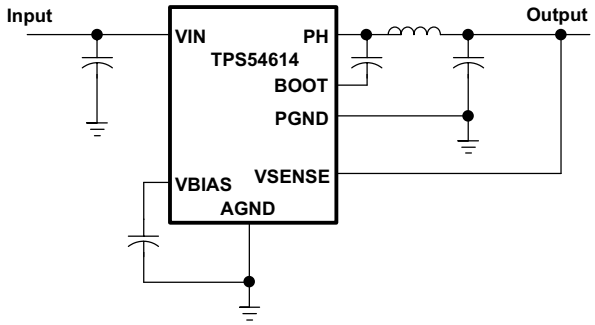
The TPS5461x devices are available in a thermally enhanced 28-pin TSSOP (PWP) PowerPAD™ package, which eliminates bulky heatsinks. TI provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

**Device Information(1)**

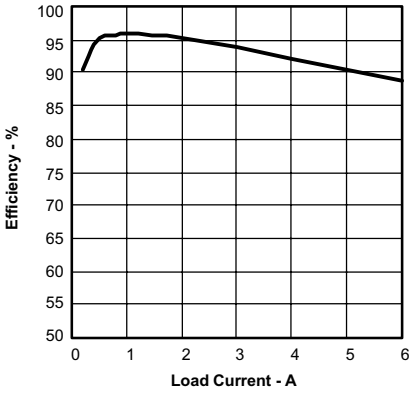
| PART NUMBER | PACKAGE | OUTPUT VOLTAGE |
|---|---|---|
| TPS54611 | HTSSOP (28) | 0.9 V |
| TPS54612 | | 1.2 V |
| TPS54613 | | 1.5 V |
| TPS54614 | | 1.8 V |
| TPS54615 | | 2.5 V |
| TPS54616 | | 3.3 V |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematic**




**Efficiency at 350 kHz**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

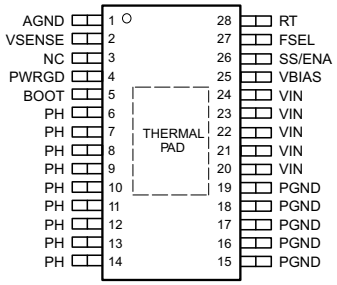
**Changes from Revision C (April 2005) to Revision D** **Page**

- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1


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# 5 Pin Configuration and Functions

**TPS5461x PWP Package**
**28-Pin HTSSOP**
**Top View**




## Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 1 | G | Analog ground. Return for slow-start capacitor, VBIAS capacitor, RT resistor FSEL. Make PowerPAD connection to AGND. |
| BOOT | 5 | S | Bootstrap input. 0.022-µF to 0.1-µF low-ESR capacitor connected from BOOT to PH generates floating drive for the high-set FET driver. |
| FSEL | 27 | I | Frequency select input. Provides logic input to select between two internally set switching frequencies. |
| NC | 3 | – | No connection |
| PGND | 15−19 | G | Power ground. High current return for the low-side driver and power MOSFET. Connect PGND with large copper areas to the input and output supply returns, and negative terminals of the input and output capacitors. |
| PH | 6−14 | O | Phase input/output. Junction of the internal high-side and low-side power MOSFETs, and output inductor. |
| PWRGD | 4 | O | Powergood open-drain output. High-Z when VSENSE ≥ 90% Vref, otherwise PWRGD is low. Note that output is low when SS/ENA is low or internal shutdown signal active. |
| RT | 28 | I | Frequency setting resistor input. Connect a resistor from RT to AGND to set the switching frequency. |
| SS/ENA | 26 | I | Slow-start/enable input/output. Dual function pin which provides logic input to enable/disable device operation and capacitor input to externally set the start-up time. |
| VBIAS | 25 | S | Internal bias regulator output. Supplies regulated voltage to internal circuitry. Bypass VBIAS pin to AGND pin with a high quality, low-ESR 0.1-µF to 1-µF ceramic capacitor. |
| VIN | 20−24 | I | Input supply for the power MOSFET switches and internal bias regulator. Bypass VIN pins to PGND pins close to device package with a high quality, low-ESR 1-µF to 10-µF ceramic capacitor. |
| VSENSE | 2 | I | Error amplifier inverting input. Connect directly to output voltage sense point. |

(1) I = Input, O = Output, S = Supply, G = Ground

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage | VIN, SS/ENA, FSEL | −0.3 | 7 | V |
| | | RT | −0.3 | 6 | V |
| | | VSENSE | −0.3 | 4 | V |
| | | BOOT | −0.3 | 17 | V |
| $V_O$ | Output voltage | VBIAS, PWRGD | −0.3 | 7 | V |
| | | PH | −0.6 | 10 | V |
| $I_O$ | Source current | PH | Internally Limited | | V |
| | | VBIAS | | 6 | mA |
| $I_S$ | Sink current | PH | | 12 | A |
| | | SS/ENA, PWRGD | | 10 | mA |
| | Voltage differential | AGND to PGND | –0.3 | 0.3 | V |
| | Continuous power dissipation | | See *Thermal Information* | | |
| $T_J$ | Operating virtual junction temperature | | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Controller Input Voltage, $V_{IN}$ | 3 | | 6 | V |
| Junction Temperature, $T_J$ | –40 | | 125 | °C |

## 6.3 Thermal Information(1)

| THERMAL METRIC(2) | | TPS5461x | UNIT |
|---|---|---|---|
| | | PWP (28 PINS) | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance, with solder | 18.2 | °C/W |
| | Junction-to-ambient thermal resistance, without solder | 40.5 | |

(1) Test Board Conditions:
(a) 3 inches × 3 inches, 4 layers, thickness: 0.062 inch
(b) 1.5 oz. copper traces located on the top of the PCB
(c) 1.5 oz. copper ground plane on the bottom of the PCB
(d) 0.5 oz. copper ground planes on the 2 internal layers
(e) 12 thermal vias. See Figure 19 for more information.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.4 Dissipation Ratings(1)(2)

| | TA = 25°C POWER RATING | TA = 70 °C POWER RATING | TA = 85 °C POWER RATING | UNIT |
|---|---|---|---|---|
| 28 Pin PWP with Solder | 5.49 (3) | 3.02 | 2.20 | W |

(1) For more information on the PWP package, refer to TI technical brief, SLMA002
(2) Test Board Conditions:
(a) 3 inches × 3 inches, 4 layers, thickness: 0.062 inch
(b) 1.5 oz. copper traces located on the top of the PCB
(c) 1.5 oz. copper ground plane on the bottom of the PCB
(d) 0.5 oz. copper ground planes on the 2 internal layers
(e) 12 thermal vias. See Figure 19 for more information.
(3) Maximum power dissipation may be limited by over-current protection


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## Dissipation Ratings[1][2] (continued)

| | TA = 25°C POWER RATING | TA = 70 °C POWER RATING | TA = 85 °C POWER RATING | UNIT |
|---|---|---|---|---|
| 28 Pin PWP without Solder | 2.48 | 1.36 | 0.99 | W |

## 6.5 Electrical Characteristics

$T_J$ = –40°C to 125°C, $V_I$ = 3 V to 6 V (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE, VIN** | | | | | | | |
| $V_{IN}$ | Input voltage range | | | 3.0 | | 6.0 | V |
| $I_{(Q)}$ | Quiescent current | | $f_S$ = 350 kHz, FSEL ≤ 0.8 V, RT open, phase pin open | | 6.2 | 9.6 | mA |
| | | | $f_S$ = 550 kHz, FSEL ≤ 2.5 V, RT open, phase pin open | | 8.4 | 12.8 | |
| | | | Shutdown, SS/ENA = 0 V | | 1 | 1.4 | |
| **UNDERVOLTAGE LOCK OUT** | | | | | | | |
| UVLO | Start threshold voltage | | | | 2.95 | 3.0 | V |
| | Stop threshold voltage | | | 2.70 | 2.80 | | V |
| | Hysteresis voltage | | | 0.14 | 0.16 | | V |
| | Rising and falling edge deglitch[1] | | | | 2.5 | | µs |
| **BIAS VOLTAGE** | | | | | | | |
| VBIAS | Output voltage | | $I_{(VBIAS)}$ = 0 | 2.70 | 2.80 | 2.90 | V |
| | Output current[2] | | | | | 100 | µA |
| **OUTPUT VOLTAGE** | | | | | | | |
| $V_O$ | Output voltage | TPS54611 | $T_J$ = 25°C, VIN = 5 V | | 0.9 | | V |
| | | | 3 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40°C ≤ $T_J$ ≤ 125°C | –2.0% | | 2.0% | |
| | | TPS54612 | $T_J$ = 25°C, VIN = 5 V | | 1.2 | | V |
| | | | 3 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40°C ≤ $T_J$ ≤ 125°C | –2.0% | | 2.0% | |
| | | TPS54613 | $T_J$ = 25°C, VIN = 5 V | | 1.5 | | V |
| | | | 3 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40°C ≤ $T_J$ ≤ 125°C | –2.0% | | 2.0% | |
| | | TPS54614 | $T_J$ = 25°C, VIN = 5 V | | 1.8 | | V |
| | | | 3 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40°C ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| | | TPS54615 | $T_J$ = 25°C, VIN = 5 V | | 2.5 | | V |
| | | | 3 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40° ≤ $T_J$ ≤ 125°C | –3.0% | | 3.0% | |
| | | TPS54616 | $T_J$ = 25°C, VIN = 5 V | | 3.3 | | V |
| | | | 4 V ≤ VIN ≤ 6 V, 0 ≤ $I_L$ ≤ 6 A, −40° ≤ $T_J$ ≤ 125°C | −3.0% | | 3.0% | |
| **REGULATION** | | | | | | | |
| | Line regulation[1][3] | | $I_L$ = 3 A, 350 ≤ $f_S$ ≤ 550 kHz, $T_J$ = 85°C | | 0.088 | | %/V |
| | Load regulation[1][3] | | $I_L$ = 0 A to 6 A, 350 ≤ $f_S$ ≤ 550 kHz, $T_J$ = 85°C | | 0.0917 | | %/A |
| **OSCILLATOR** | | | | | | | |
| | Internally set – free running frequency | | FSEL ≤ 0.8 V, RT open | 280 | 350 | 420 | kHz |
| | | | FSEL ≥ 2.5 V, RT open | 440 | 550 | 660 | |
| | Externally set – free running frequency range | | RT = 180 kΩ (1% resistor to AGND)[1] | 252 | 280 | 308 | kHz |
| | | | RT = 100 kΩ (1% resistor to AGND) | 460 | 500 | 540 | |
| | | | RT = 68 kΩ (1% resistor to AGND)[1] | 663 | 700 | 762 | |
| FSEL | High level threshold | | | 2.5 | | | V |
| | Low level threshold | | | | | 0.8 | V |
| | Ramp valley[1] | | | | 0.75 | | V |
| | Ramp amplitude (peak-to-peak)[1] | | | | 1 | | V |

(1) Specified by design
(2) Static resistive loads only
(3) Tested using circuit in Figure 10.

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## Electrical Characteristics (continued)

$T_J$ = –40°C to 125°C, $V_I$ = 3 V to 6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Minimum controllable on time(1) | | | | | 200 | ns |
| Maximum duty cycle(1) | | | 90% | | | |
| **ERROR AMPLIFIER** | | | | | | |
| Error amplifier open loop voltage gain(1) | | | | 26 | | dB |
| Error amplifier unity gain bandwidth(1) | | | 3 | 5 | | MHz |
| Error amplifier common mode input voltage range | | Powered by internal LDO(1) | 0 | | VBIAS | V |
| **PWM COMPARATOR** | | | | | | |
| PWM comparator propagation delay time, PWM comparator input to PH pin (excluding deadtime) | | 10-mV overdrive(1) | | 70 | 85 | ns |
| **SLOW-START/ENABLE** | | | | | | |
| Enable threshold voltage, SS/ENA | | | 0.82 | 1.20 | 1.40 | V |
| Enable hysteresis voltage, SS/ENA(1) | | | | 0.03 | | V |
| Falling edge deglitch, SS/ENA(1) | | | | 2.5 | | µs |
| Internal slow-start time(1) | TPS54611 | | 2.6 | 3.3 | 4.1 | ms |
| | TPS54612 | | 3.5 | 4.5 | 5.4 | |
| | TPS54613 | | 4.4 | 5.6 | 6.7 | |
| | TPS54614 | | 2.6 | 3.3 | 4.1 | |
| | TPS54615 | | 3.6 | 4.7 | 5.6 | |
| | TPS54616 | | 4.7 | 6.1 | 7.6 | |
| Charge current, SS/ENA | | SS/ENA = 0V | 3 | 5 | 8 | µA |
| Discharge current, SS/ENA | | SS/ENA = 0.2 V, $V_I$ = 2.7 V | 1.5 | 2.3 | 4.0 | mA |
| **POWERGOOD** | | | | | | |
| Powergood threshold voltage | | VSENSE falling | | 90 | | $\%V_O$ |
| Powergood hysteresis voltage | | See (1) | | 3 | | $\%V_O$ |
| Powergood falling edge deglitch | | See (1) | | 35 | | µs |
| Output saturation voltage, PWRGD | | $I_{(sink)}$ = 2.5 mA | | 0.18 | 0.3 | V |
| Leakage current, PWRGD | | $V_I$ = 5.5 V | | | 1 | µA |
| **CURRENT LIMIT** | | | | | | |
| Current limit | | $V_I$ = 3 V(1) | 7.2 | 10 | | A |
| | | $V_I$ = 6 V(1) | 10 | 12 | | |
| Current limit leading edge blanking time(1) | | | | 100 | | ns |
| Current limit total response time(1) | | | | 200 | | ns |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal shutdown trip point(1) | | | 135 | 150 | 165 | °C |
| Thermal shutdown hysteresis(1) | | | | 10 | | |
| **OUTPUT POWER MOSFETS** | | | | | | |
| $r_{DS(on)}$ | Power MOSFET switches | $I_O$ = 3 A, $V_I$ = 6 V(4) | | 26 | 47 | mΩ |
| | | $I_O$ = 3 A, $V_I$ = 3 V(4) | | 36 | 65 | |

(4) Matched MOSFETs, low-side $r_{DS(on)}$ production tested, high-side $r_{DS(on)}$ specified by design.


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## 6.6 Typical Characteristics

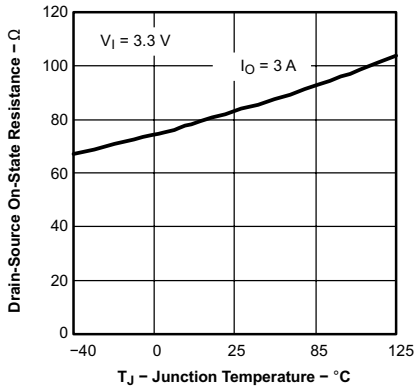



**Figure 1. Drain-source On-state Resistance vs Junction Temperature**

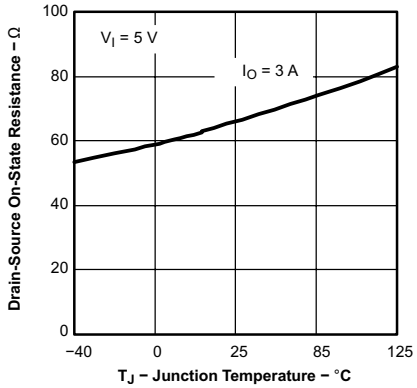



**Figure 2. Drain-source On-state Resistance vs Junction Temperature 2**

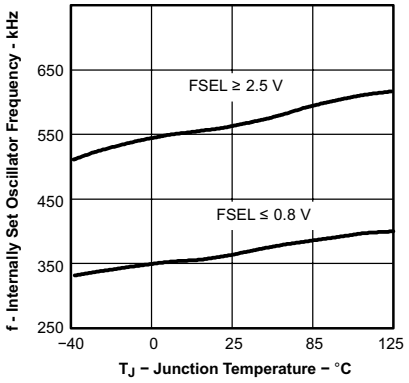



**Figure 3. Internally Set Oscillator Frequency vs Junction Temperature 3**

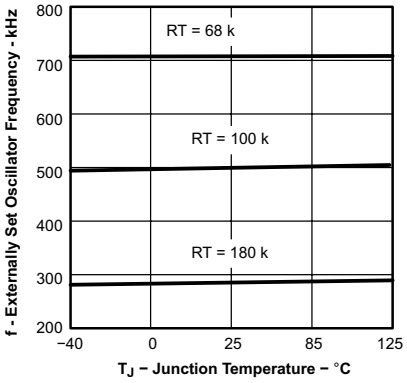



**Figure 4. Externally Set Oscillator Frequency vs Junction Temperature 4**

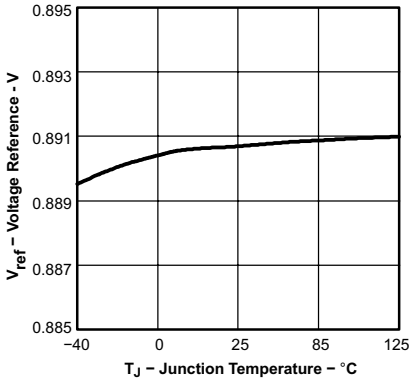
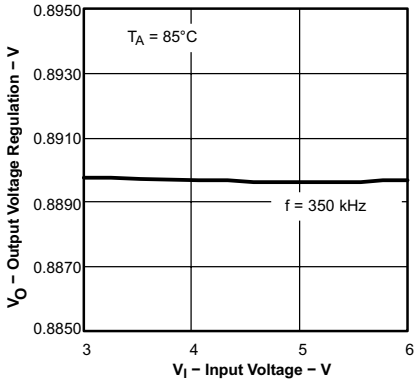



**Figure 5. Voltage Reference vs Junction Temperature**




Tested using TPS54611

**Figure 6. Output Voltage Regulation vs Input Voltage**

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## Typical Characteristics (continued)

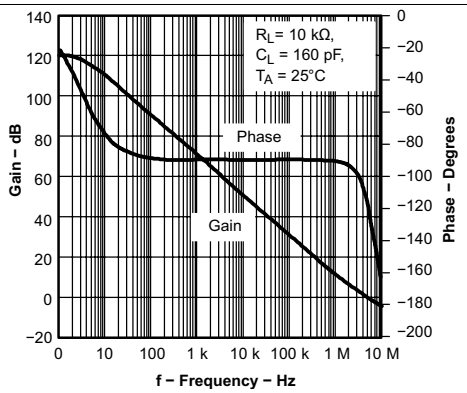
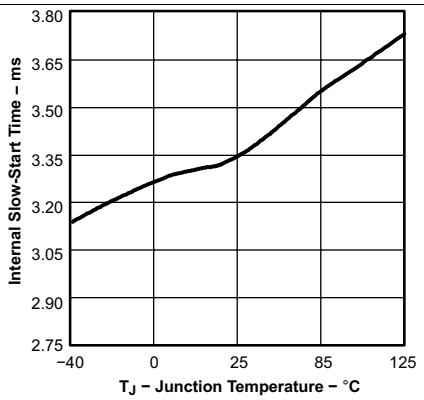



**Figure 7. Error Amplifier Open Loop Response**




Tested using TPS54611

**Figure 8. Internal Slow-Start Time vs Junction Temperature**

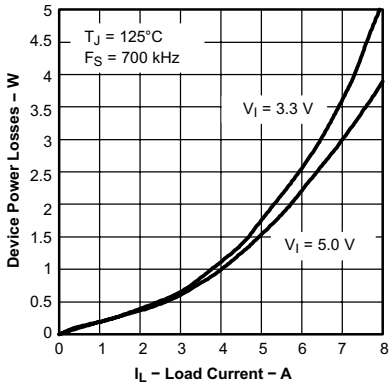



**Figure 9. Device Power Losses vs Load Current**

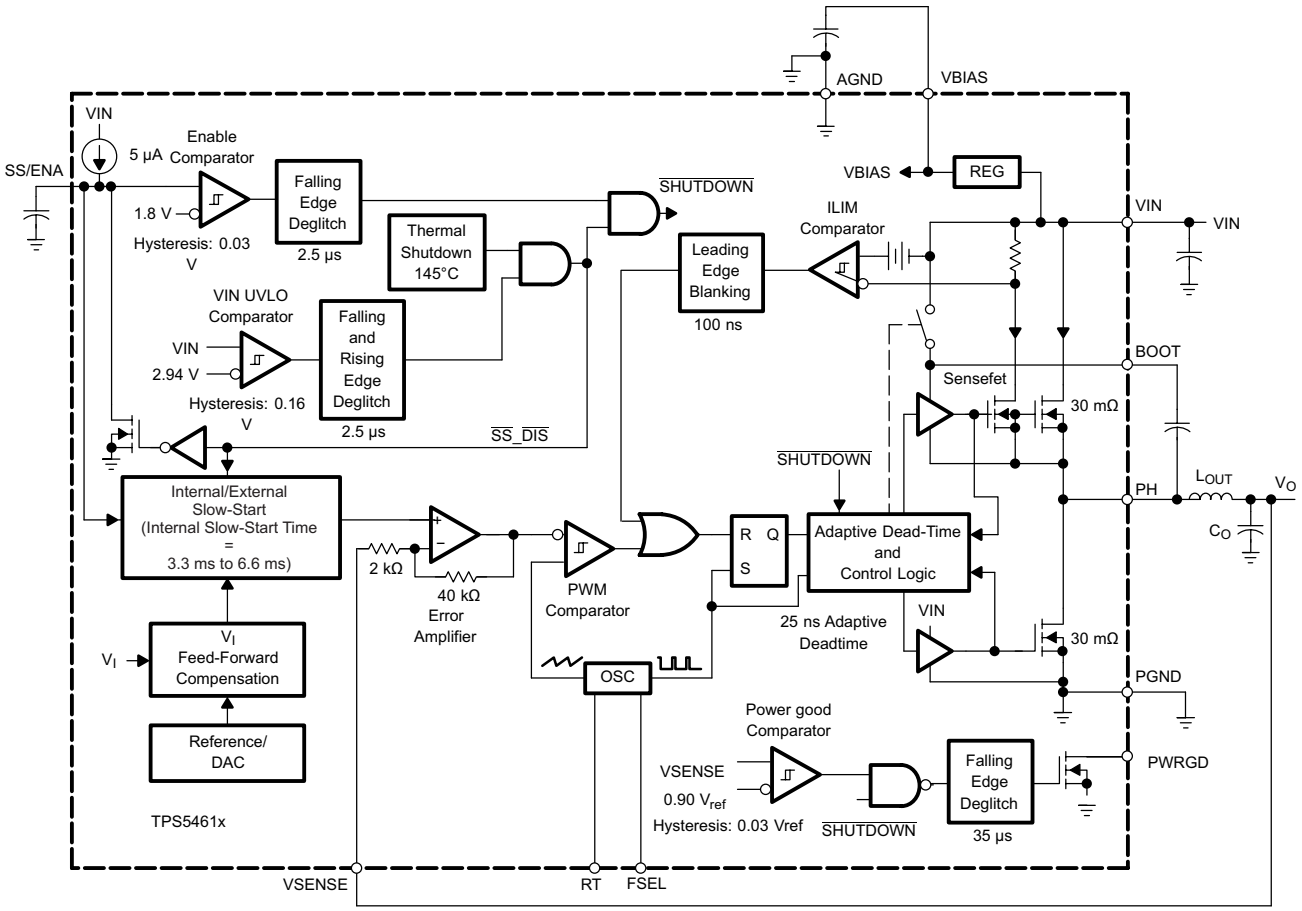

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# 7 Detailed Description

## 7.1 Overview

The SWIFT family of DC - DC regulators, the TPS54611, TPS54612, TPS54613, TPS54614, TPS54615, and TPS54616 are low-input voltage high-output current synchronous-buck PWM converters integrate all required active components. Included on the substrate are true, high-performance, voltage error amplifiers that provide high performance under transient conditions; an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 3 V; an internally and externally set slow-start circuit to limit in-rush currents; and a powergood output useful for processor/logic reset, fault signaling, and supply sequencing.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

### 7.3.1 Undervoltage Lock Out (UVLO)

The TPS5461x incorporates an UVLO circuit to keep the device disabled when the input voltage (VIN) is insufficient. During power up, internal circuits are held inactive until VIN exceeds the nominal UVLO threshold voltage of 2.95 V. Once the UVLO start threshold is reached, device start-up begins. The device operates until VIN falls below the nominal UVLO stop threshold of 2.8 V. Hysteresis in the UVLO comparator, and a 2.5-µs rising and falling edge deglitch circuit, reduces the likelihood of shutting the device down due to noise on VIN.

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## Feature Description (continued)

### 7.3.2 Slow-Start and Enable (SS/ENA)

The slow-start/enable pin provides two functions. First, the pin acts as an enable (shutdown) control by keeping the device turned off until the voltage exceeds the start threshold voltage of approximately 1.2 V. When SS/ENA exceeds the enable threshold, device start up begins. The reference voltage fed to the error amplifier is linearly ramped up from 0 V to 0.891 V in 3.35 ms. Similarly, the converter output voltage reaches regulation in approximately 3.35 ms. Voltage hysteresis and a 2.5-µs falling edge deglitch circuit reduce the likelihood of triggering the enable due to noise. Refer to Table 1 for startup times for each device.

**Table 1. Device Startup Times**

| DEVICE | OUTPUT VOLTAGE | SLOW-START |
|---|---|---|
| TPS54611 | 0.9 V | 3.3 ms |
| TPS54612 | 1.2 V | 4.5 ms |
| TPS54613 | 1.5 V | 5.6 ms |
| TPS54614 | 1.8 V | 3.3 ms |
| TPS54615 | 2.5 V | 4.7 ms |
| TPS54616 | 3.3 V | 6.1 ms |

The second function of the SS/ENA pin provides an external means for extending the slow-start time with a ceramic capacitor connected between SS/ENA and AGND. Adding a capacitor to the SS/ENA pin has two effects on start-up. First, a delay occurs between release of the SS/ENA pin and start-up of the output. The delay is proportional to the slow-start capacitor value and lasts until the SS/ENA pin reaches the enable threshold. The start-up delay is approximately:

$$t_d = C_{(SS)} \times \frac{1.2\ V}{5\ \mu A} \quad (1)$$

Second, as the output becomes active, a brief ramp up at the internal slow-start rate may be observed before the externally set slow-start rate takes control and the output rises at a rate proportional to the slow-start capacitor. The slow-start time set by the capacitor is approximately:

$$t_{(SS)} = C_{(SS)} \times \frac{0.7\ V}{5\ \mu A} \quad (2)$$

The actual slow-start time is likely to be less than the above approximation due to the brief ramp up at the internal rate

### 7.3.3 VBIAS Regulator

The VBIAS regulator provides internal analog and digital blocks with a stable supply voltage over variations in junction temperature and input voltage. A high quality, low-ESR, ceramic bypass capacitor is required on the VBIAS pin. X7R or X5R grade dielectrics are recommended because their values are more stable over temperature. The bypass capacitor should be placed close to the VBIAS pin and returned to AGND.

External loading on VBIAS is allowed, with the caution that internal circuits require a minimum VBIAS of 2.7 V, and external loads on VBIAS with ac or digital switching noise may degrade performance. The VBIAS pin may be useful as a reference voltage for external circuits.

### 7.3.4 Voltage Reference

The voltage reference system produces a precise, temperature-stable voltage from a bandgap circuit. A scaling amplifier and DAC are then used to produce the reference voltages for each of the fixed output devices.

### 7.3.5 Oscillator and PWM Ramp

The oscillator frequency can be set to internally fixed values of 350 kHz or 550 kHz using the FSEL pin as a static digital input. If a different frequency of operation is required for the application, the oscillator frequency can be externally adjusted from 280 kHz to 700 kHz by connecting a resistor from the RT pin to AGND and floating the FSEL pin. The switching frequency is approximated by the following equation, where R is the resistance from RT to AGND


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$$\text{Switching Frequency} = \frac{100\ \text{k}\Omega}{\text{R}} \times 500\ \text{[kHz]} \quad (3)$$

Table 2 summarizes the frequency selection configurations:

**Table 2. Switching Frequencies**

| SWITCHING FREQUENCY | SYNC PIN | RT PIN |
|---|---|---|
| 350 kHz, internally set | Float or AGND | Float |
| 550 kHz, internally set | ≥2.5 V | Float |
| Externally set 280 kHz to 700 kHz | Float | R = 180 k to 68 k |

### 7.3.6 Error Amplifier

The high performance, wide bandwidth, voltage error amplifier is gain-limited to provide internal compensation of the control loop. The user is given limited flexibility in choosing output L and C filter components. Inductance values of 4.7 µH to 10 µH are typical and available from several vendors. The resulting designs exhibit good noise and ripple characteristics, but with exceptional transient response. Transient recovery times are typically in the range of 10 µs to 20 µs.

### 7.3.7 PWM Control

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, OR gate, PWM latch, and portions of the adaptive dead-time and control logic block. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately set and reset the PWM latch. Once the PWM latch is set, the low-side FET remains on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to its valley voltage. When the ramp begins to charge back up, the low-side FET turns off and high-side FET turns on. As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side FET remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output could be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset, and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the low-side FET on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set-point, setting VSENSE to approximately the same voltage as $V_{ref}$. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The low-side FET remains on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS5461x devices are capable of sinking current continuously until the output reaches the regulation set-point.

If the current limit comparator trips for longer than 100 ns, the PWM latch resets before the PWM ramp exceeds the error amplifier output. The high-side FET turns off and the low-side FET turns on to decrease the energy in the output inductor and consequently decrease the output current. This process is repeated each cycle in which the current limit comparator is tripped.

### 7.3.8 Dead-Time Control and MOSFET Drivers

Adaptive dead-time control prevents shoot-through current from flowing in both N-channel power MOSFETs during the switching transitions by actively controlling the turnon times of the MOSFET drivers. The high-side driver does not turn on until the voltage at the gate of the low-side FET is below 2 V. The high-side and low-side drivers are designed with 300 mA source and sink capability to quickly drive the power MOSFETs gates. The low-side driver is supplied from VIN, while the high-side drive is supplied from the BOOT pin. A bootstrap circuit uses an external BOOT capacitor and internal 2.5-Ω bootstrap switch connected between the VIN and BOOT pins. The integrated bootstrap switch improves drive efficiency and reduces external component count.

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### 7.3.9 Overcurrent Protection

Cycle-by-cycle current limiting is achieved by sensing the current flow through the high-side MOSFET and a differential amplifier with preset overcurrent threshold. The high-side MOSFET is turned off within 200 ns of reaching the current limit threshold. A 100 ns leading edge blanking circuit prevents false tripping of current limit. Current limit detection occurs only when current flows from VIN to PH when sourcing current to the output filter. Load protection during current sink operation is provided by thermal shutdown.

### 7.3.10 Thermal Shutdown

The device uses the thermal shutdown to turn off the power MOSFETs and disable the controller if the junction temperature exceeds 150°C. The device is released from shutdown when the junction temperature decreases to 10°C below the thermal shutdown trip point, and starts up under control of the slow-start circuit. Thermal shutdown provides protection when an overload condition is sustained for several milliseconds. With a persistent fault condition, the device cycles continuously: starting up by control of the slow-start circuit, heating up due to the fault, and then shutting down upon reaching the thermal shutdown trip point.

### 7.3.11 Powergood (PWRGD)

The powergood circuit monitors for undervoltage conditions on VSENSE. If the voltage on VSENSE falls 10% below the reference voltage, the open-drain PWRGD output is pulled low. PWRGD is also pulled low if VIN is less than the UVLO threshold, or SS/ENA is low, or thermal shutdown is asserted. When VIN = UVLO threshold, SS/ENA = enable threshold, and VSENSE > 90% of $V_{ref}$, the open-drain output of the PWRGD pin is high. A hysteresis voltage equal to 3% of $V_{ref}$ and a 35-µs falling edge deglitch circuit prevent tripping of the powergood comparator due to high-frequency noise.

## 7.4 Device Functional Modes

### 7.4.1 Continuous Conduction Mode

These devices operate in continuous conduction mode (CCM) at a fixed frequency regardless of the output current.


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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS5461x devices are fixed output voltage synchronous step-down DC-DC converters. These devices are used to convert a higher DC input voltage to a lower DC output voltage with a maximum output current of 6A.

## 8.2 Typical Application

Figure 10 shows the schematic diagram for a typical TPS54614 application. The TPS54614 (U1) can provide greater than 6 A of output current at a nominal output voltage of 1.8 V. For proper operation, the exposed thermal PowerPAD underneath the integrated circuit package needs to be soldered to the printed-circuit board.

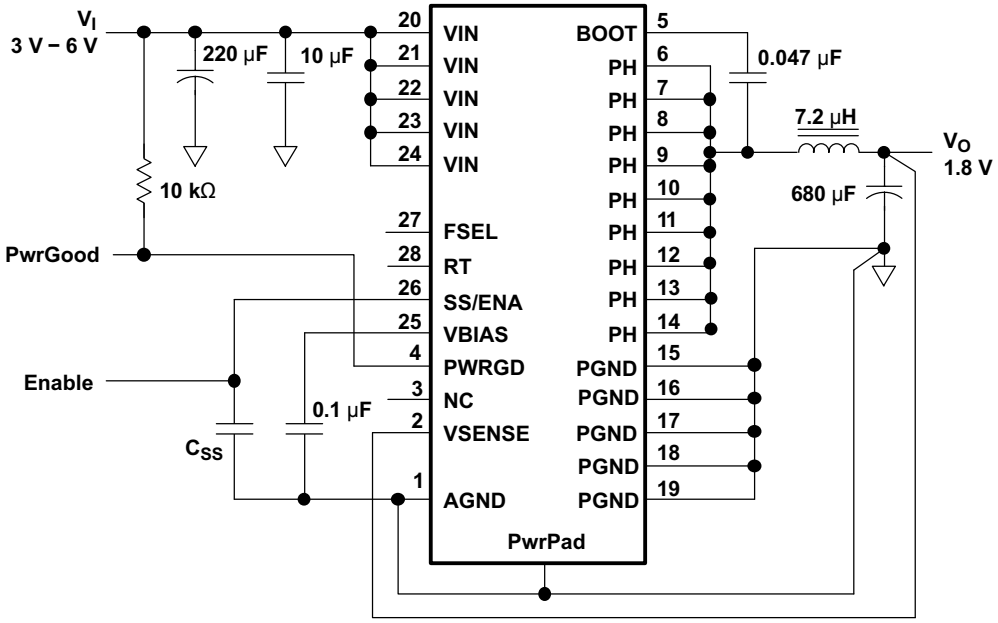



**Figure 10. Application Circuit**

### 8.2.1 Design Requirements

The design requirements for this example are listed in Table 3.

**Table 3. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| DC Input Voltage Range | 3 V – 6 V |
| DC Output Voltage | 1 V |
| DC Output Current Range | 0A – 6 A |
| Load Transient Step | 3A – 6 A |
| Load Regulation Control | ± 5 mV |
| Loop Crossover Frequency | 50 kHz |
| Control Loop Phase Margin | 55° |

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### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Component Selection*

The values for the components used in this design example were selected using the SWIFT designer software tool. SWIFT designer provides a complete design environment for developing dc-dc converters using the TPS54614, or other devices in the SWIFT product family. Additional design information is available at www.ti.com.

#### *8.2.2.2 Input Filter*

The input to the circuit is a nominal 3.3 VDC or 5 VDC. The input filter is a 220-µF POSCAP capacitor, with a maximum allowable ripple current of 3 A. A 10-µF ceramic capacitor for the TPS54614 is required, and must be located as close as possible to the device.

#### *8.2.2.3 Feedback Circuit*

The output voltage of the converter is fed directly into the VSENSE pin of the TPS54614. The TPS54614 is internally compensated to provide stability of the output under varying line and load conditions.

#### *8.2.2.4 Operating Frequency*

In the application circuit, 350 kHz operation is selected by leaving FSEL open. Different operating frequencies can be selected by connecting a resistor between RT pin and AGND. Choose the value of R using Equation 4 for the desired operating frequency:

$$R = \frac{500\ \text{kHz}}{\text{SwitchingFrequency}} \times 100\ \text{k}\Omega \tag{4}$$

Alternately, a preset operating frequency of 550 kHz can be selected by leaving RT open and connecting the FSEL pin to $V_I$.

#### *8.2.2.5 Output Filter*

The output filter is composed of a 5.2-µH inductor and a 470-µF capacitor. The inductor is low dc resistance (16-mΩ) type, Sumida CDRH104R−5R2. The capacitor used is a 4-V POSCAP with a maximum ESR of 40 mΩ. The output filter components work with the internal compensation network to provide a stable closed loop response for the converter.

### 8.2.3 Application Curves

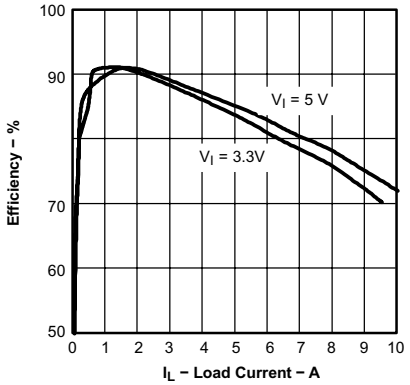



**Figure 11. Efficiency vs Load Current**

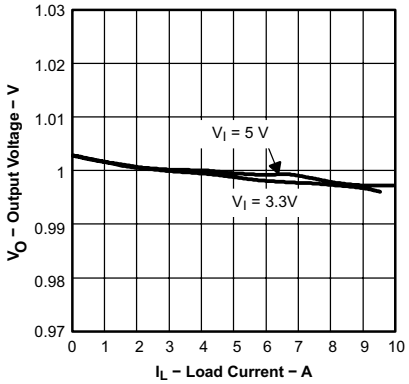



**Figure 12. Output Voltage vs Load Current**


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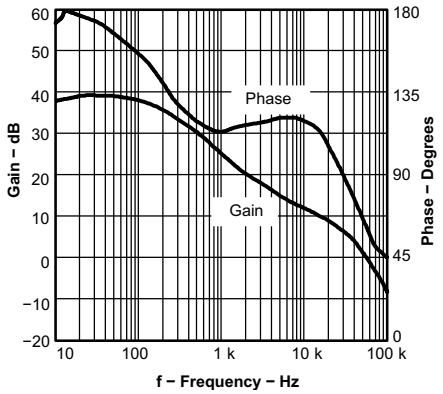



Figure 13. Loop Response

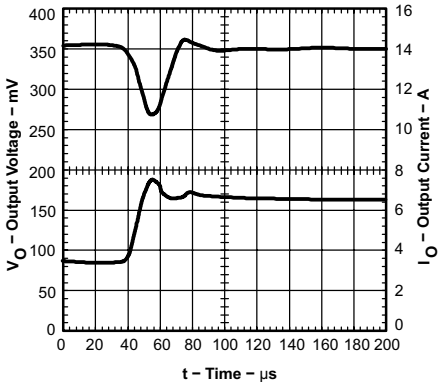



Figure 14. Transient Response

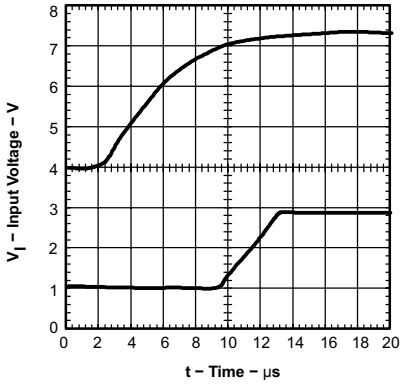



Figure 15. Start-up Waveforms

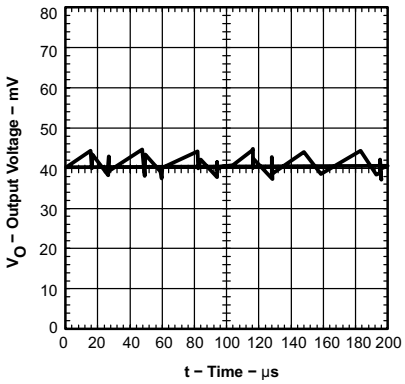



Figure 16. Output Ripple Voltage

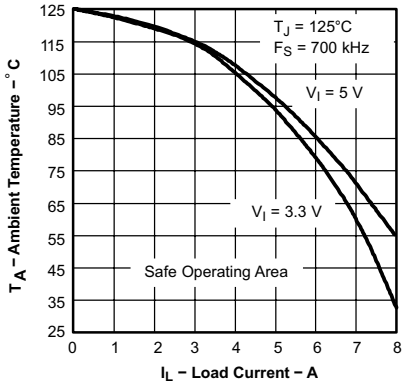



Figure 17. Ambient Temperature vs Load Current

# 9 Power Supply Recommendations

These devices operate from an input supply voltage between 3 V and 6 V. This supply must be well-regulated. Proper bypassing of input supplies and internal regulators is critical for noise performance, as is good PCB layout practice. See the recommendations in *Layout*.

# 10 Layout

## 10.1 Layout Guidelines

Figure 18 shows a generalized PCB layout guide for the TPS5461x.

- The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54311−16 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.
- The TPS54311−16 has two internal grounds (analog and power). Inside the TPS54311−16, the analog ground ties to all of the noise sensitive signals, while the power ground ties to the noisier power signals. Noise injected between the two grounds can degrade the performance of the TPS54311−16, particularly at higher output currents. Ground noise on an analog ground plane can also cause problems with some of the control and bias signals. For these reasons, separate analog and power ground traces are recommended. There should be an area of ground one the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. The only components that should tie directly to the power ground plane are the input capacitors, the output capacitors, the input voltage decoupling capacitor, and the PGND pins of the TPS54311−16. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the timing resistor RT, slow start capacitor and bias capacitor grounds. Connect this trace directly to AGND (pin 1).
- The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.
- Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as practical.
- Connect the output of the circuit directly to the VSENSE pin. Do not place this trace too close to the PH trace. Do to the size of the IC package and the device pinout, they will have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.
- Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350-kHz operating frequency, connect them to this trace as well.


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## 10.2 Layout Example

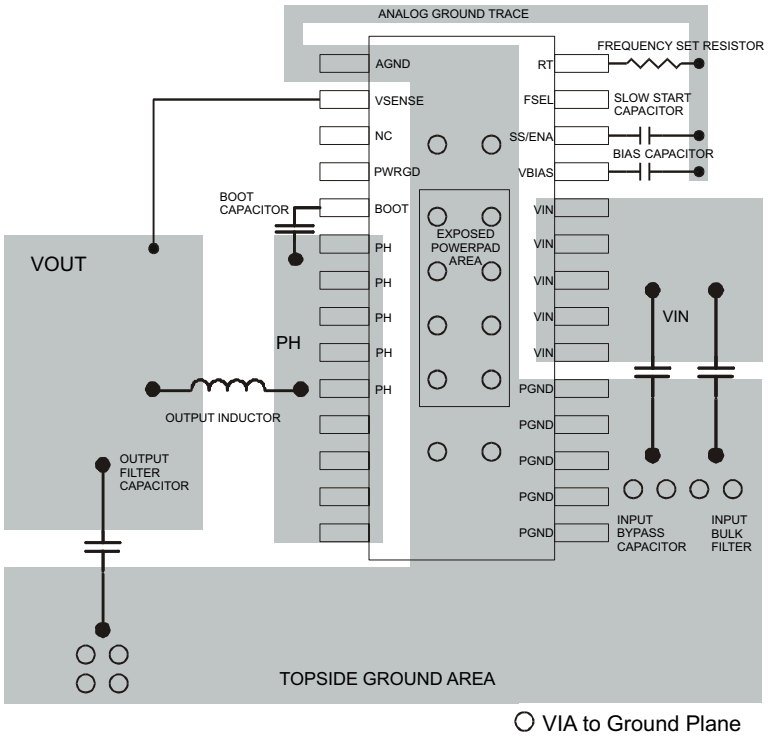



**Figure 18. TPS5461x PCB Layout**

## 10.3 Thermal Considerations

For operation at full rated load current, the analog ground plane must provide adequate heat dissipating area. A 3 inch by 3 inch plane of 1 ounce copper is recommended, though not mandatory, depending on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the top or bottom layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposes area of the PowerPAD to the analog ground plane layer should be made using 0.013 inch diameter vias to avoid solder wicking through the vias. Eight vias should be in the PowerPAD area with four additional vias located under the device package. The size of the vias under the package, but not in the exposed thermal pad area, can be increased to 0.018. Additional vias beyond the ten recommended that enhance thermal performance should be included in areas not under the device package.

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## Thermal Considerations (continued)

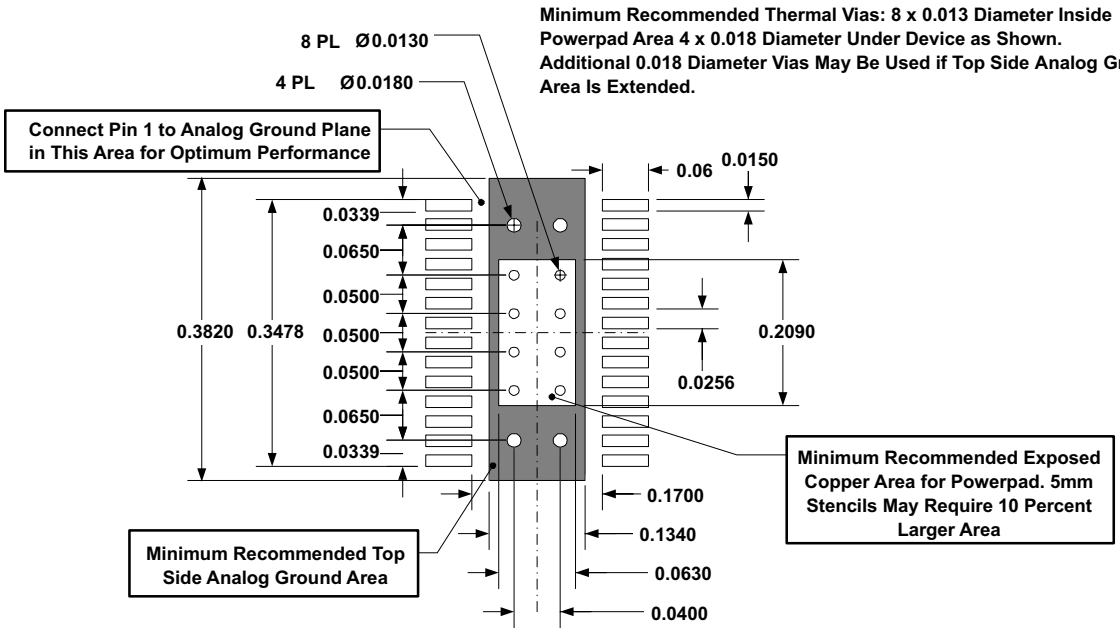



**Figure 19. Recommended Land Pattern for 28-Pin PWP PowerPAD 12**


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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Related DC - DC Products

- TPS40000—Low-input, voltage-mode synchronous buck controller
- TPS759xx—7.5-A low dropout regulator
- PT6440 series—6-A plugin modules

## 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS54611 | Click here | Click here | Click here | Click here | Click here |
| TPS54612 | Click here | Click here | Click here | Click here | Click here |
| TPS54613 | Click here | Click here | Click here | Click here | Click here |
| TPS54614 | Click here | Click here | Click here | Click here | Click here |
| TPS54615 | Click here | Click here | Click here | Click here | Click here |
| TPS54616 | Click here | Click here | Click here | Click here | Click here |

## 11.3 Trademarks

SWIFT, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

## 11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54611PWP | NRND | HTSSOP | PWP | 28 | 50 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54611 | |
| TPS54612PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54612 | Samples |
| TPS54612PWPRG4 | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54612 | Samples |
| TPS54613PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54613 | Samples |
| TPS54614PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54614 | Samples |
| TPS54615PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54615 | Samples |
| TPS54616PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TPS54616 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS54615 :**

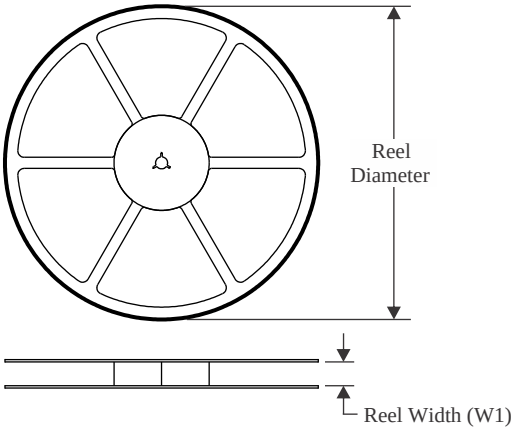
- Enhanced Product : TPS54615-EP

NOTE: Qualified Version Definitions:

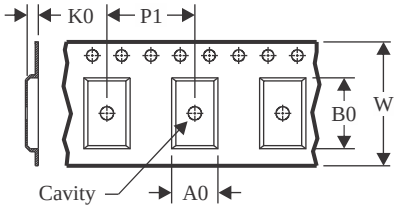
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

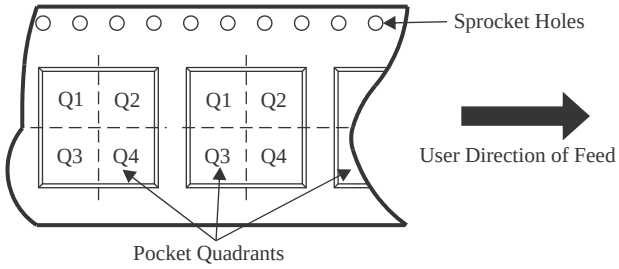



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

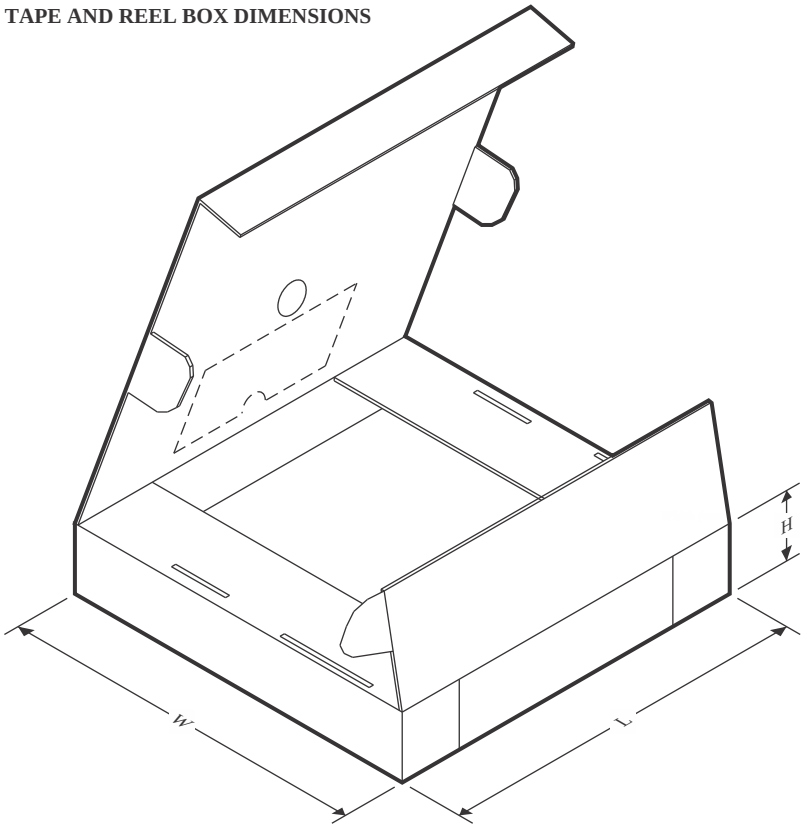
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54613PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54613PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54615PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54615PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

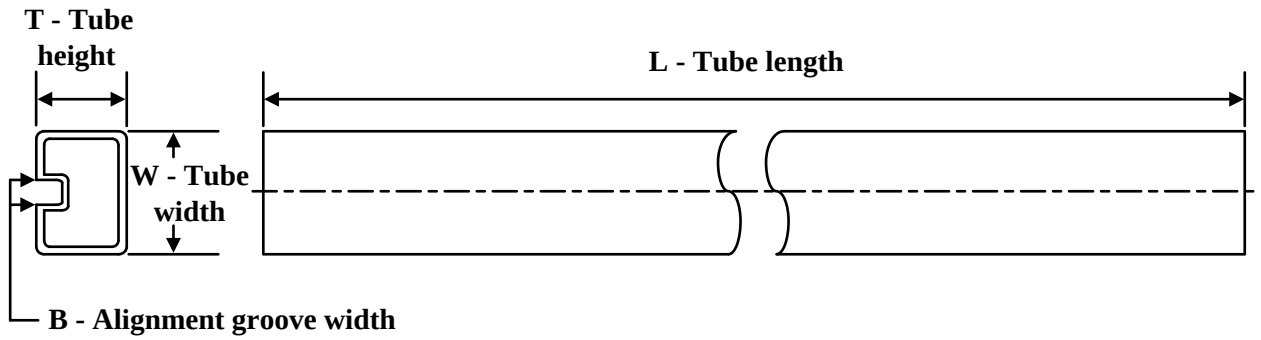
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54612PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54613PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54613PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54614PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54615PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54615PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 356.0 | 356.0 | 35.0 |
| TPS54616PWPR | HTSSOP | PWP | 28 | 2000 | 350.0 | 350.0 | 43.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| TPS54611PWP | PWP | HTSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |

# GENERIC PACKAGE VIEW

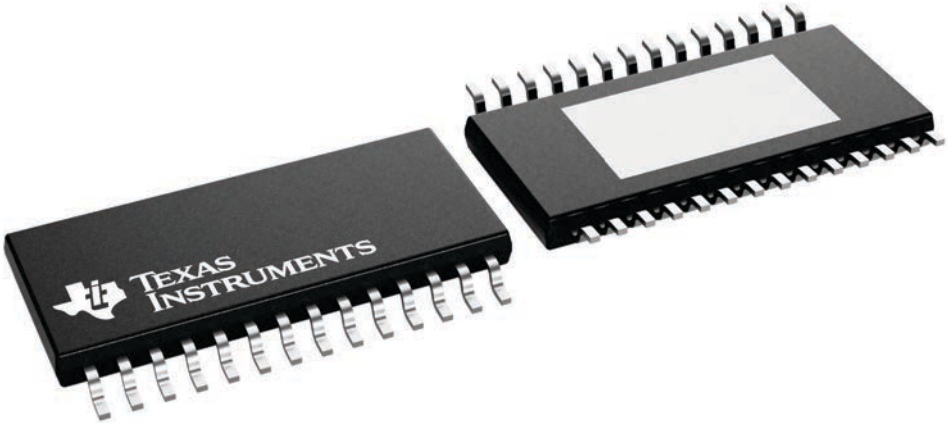
## PWP 28

## PowerPAD™ TSSOP - 1.2 mm max height

**4.4 x 9.7, 0.65 mm pitch**

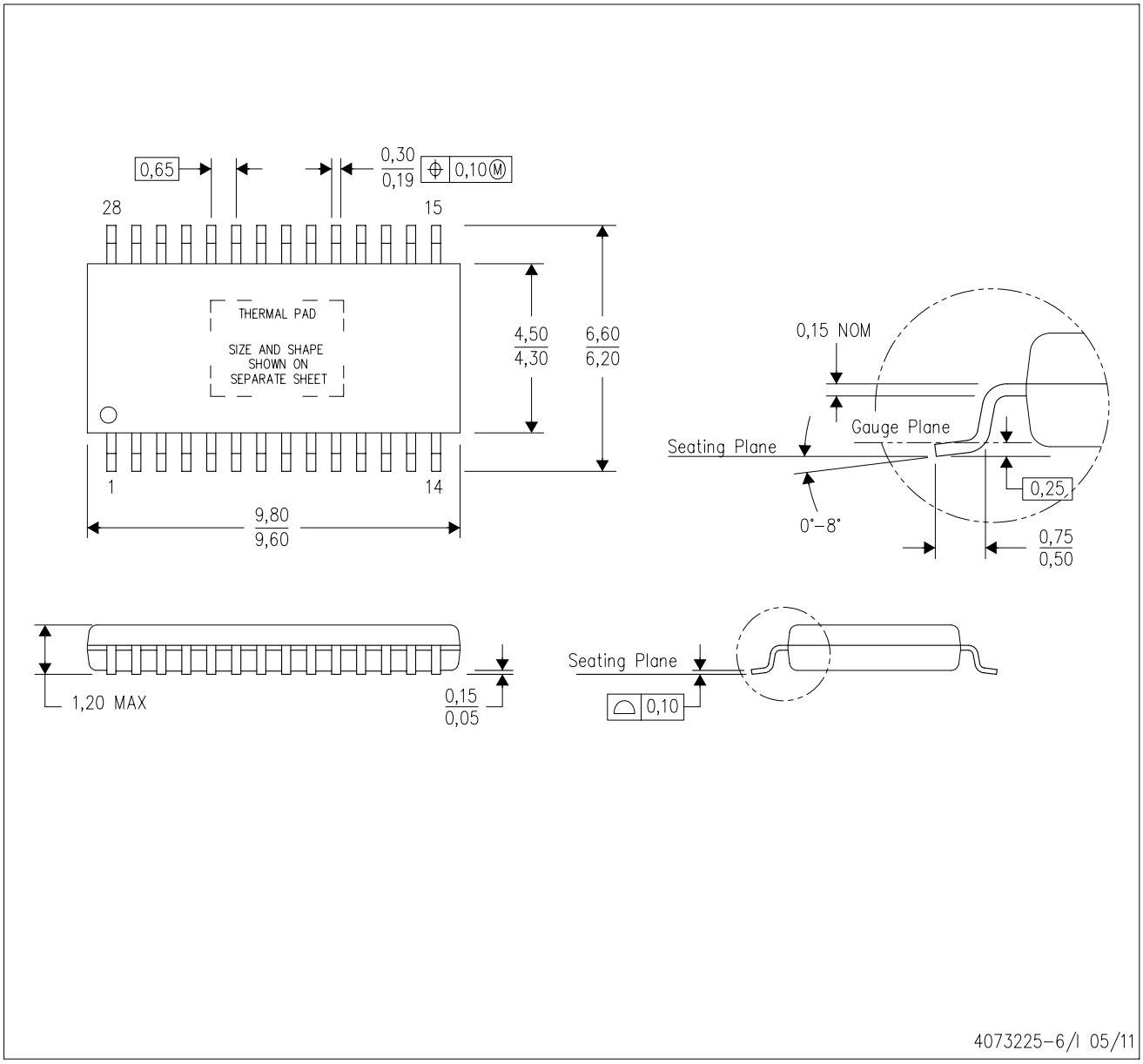
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

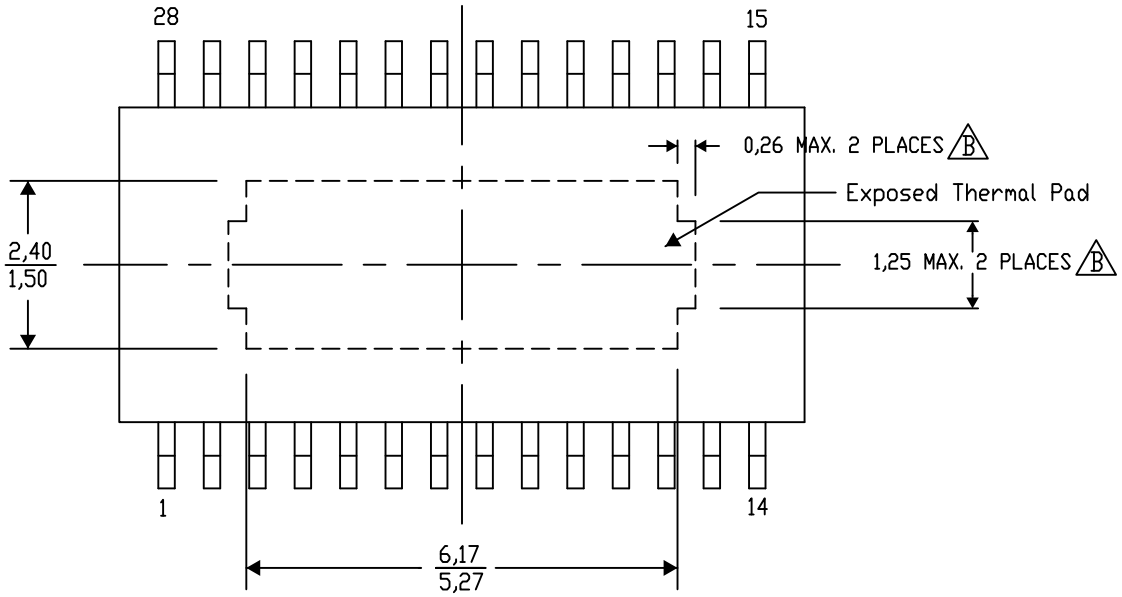
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

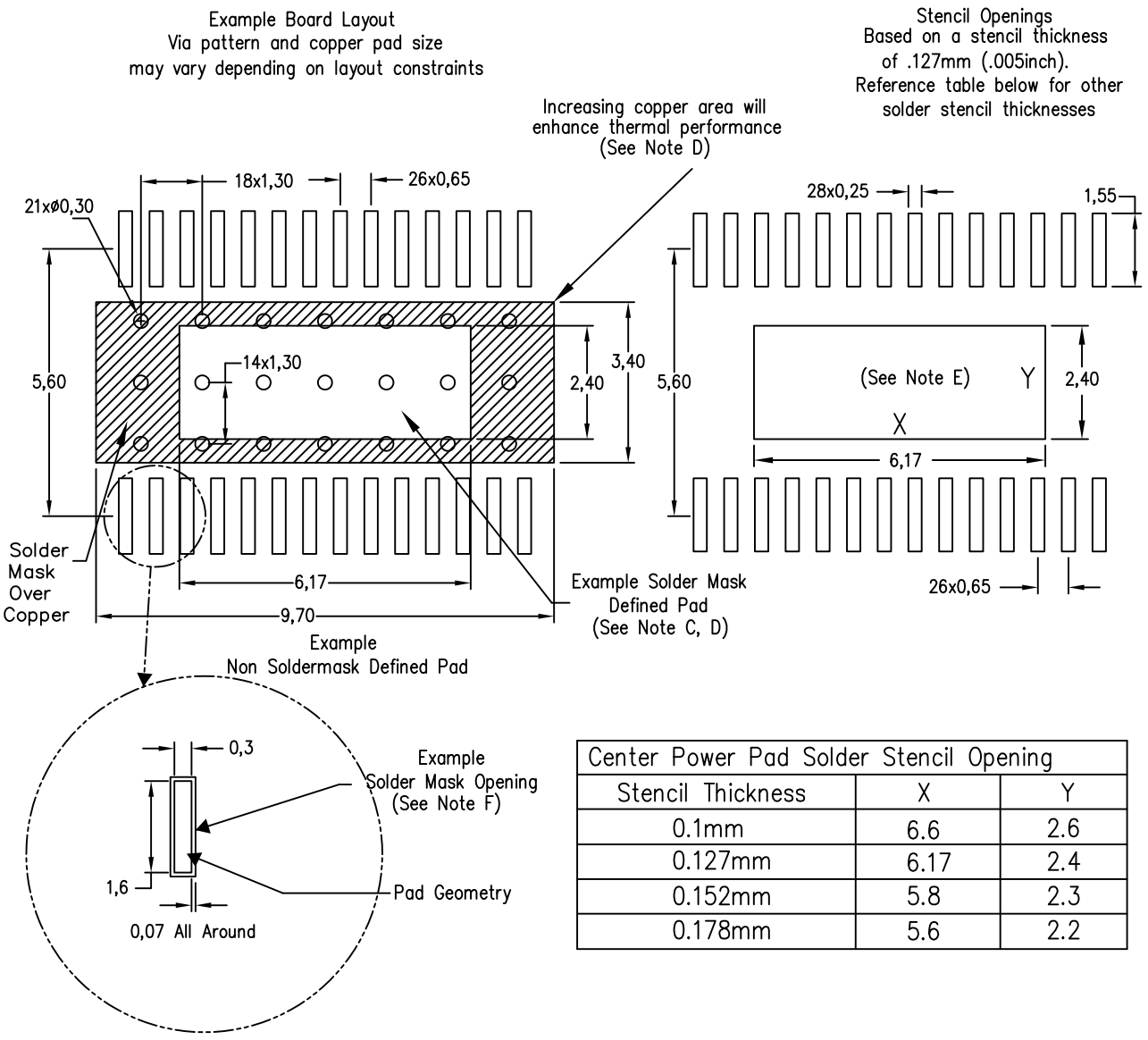
4206332–33/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 6.6 | 2.6 |
| 0.127mm | 6.17 | 2.4 |
| 0.152mm | 5.8 | 2.3 |
| 0.178mm | 5.6 | 2.2 |

4207609–19/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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