TEXAS INSTRUMENTS

TPS54614EVM, 1.8-V Swift™ Regulator Evaluation Module

User's Guide

September 2001 **PMP PD & PS**

SLVU053

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It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TPS54614 1.8-V SWIFT™ regulator evaluation module (EVM). The users guide includes a schematic diagram and bill of materials.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Inroduction
- Chapter 2—Setup and Test Results
- Chapter 3—Board Layout
- Chapter 4—Schematic and Bill of Materials

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Chapter 1

Introduction

This chapter contains background information for the TPS54614 and support documentation for the TPS54614 EVM evaluation module. The TPS54614 EVM performance specifications are given, as well as modification instructions if different preset output voltages are desired.

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1.1 Background

The TPS54614 evaluation module uses the TPS54614 synchronous buck regulator to provide a 1.8-V output. This voltage is maintained over an input range of 3.0 V to 6.0 V, and over a load range of 0 A to 6 A. The TPS54614 EVM circuitry contains only seven electrical components covering an area less than one square inch.

The TPS54614 has two key features that reduce the number of additional components compared to traditional synchronous buck controllers. The first feature is that the MOSFETs are incorporated inside the TPS54614 package. This eliminates the need for external MOSFETs and their associated drivers. The second feature is that the compensation components that stabilize the feedback loop are also incorporated inside the TPS54614 package.

Because the internal compensation of the TPS54614 is fixed, loop stability is assured by the proper selection of an output inductor and output capacitor. For guidelines on selecting an output inductor and output capacitor for a specific application, refer to Texas Instruments application report *SLVA105 – Designing With Internally Compensated SWIFT™ Regulators*.

1.2 Performance Specification Summary

A summary of the TPS54614EVM performance specifications is provided by Table 1–1. All specifications are given for an ambient temperature of 25°C, unless otherwise noted.

Table 1–1. Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Units
Input voltage range	I_O = 6 A	3	5	6	V
Output voltage set point			1.8		V
Output current range		0		> 6	A
Line regulation	I_O = 6 A	–5		+5	mV
Load regulation	V_{IN} = 5 V	–9		+9	mV
Load transient response	I_O = 1.5 A to 4.5 A, t_r = 16 µs		–80		mV_{PK}
			50		µs
	I_O = 4.5 A to 1.5 A, t_f = 12 µs		55		mV_{PK}
			50		µs
Loop bandwidth	V_{IN} = 5 V, I_O = 6 A		50		kHz
Phase margin	V_{IN} = 5 V, I_O = 6 A		46		°
Input ripple voltage				270	mV_{pp}
Output ripple voltage			10	18	mV_{PP}
Output rise time			3.6		ms
Operating frequency		440	550	660	kHz
Efficiency	V_{IN} = 5 V, I_O = 1.5 A		91%		

1.3 Modifications

The EVM can be modified for different preset output voltages by using other devices in the TPS5461x family. For output voltages less than 2.5 V, only U1 needs to be changed. For output voltages 2.5 V and higher, the output capacitor (C1) also needs to be changed. Table 1–2 lists the devices required for U1 and C1 for different output voltage options.

Table 1–2. Modification Table

Output Voltage (V)	SWIFT™ Device (U1)	Output Capacitor (C1)
0.9	TPS54611	Sanyo – 2R5TPB680M
1.2	TPS54612	Sanyo – 2R5TPB680M
1.5	TPS54613	Sanyo – 2R5TPB680M
1.8	TPS54614	Sanyo – 2R5TPB680M
2.5	TPS54615	Sanyo – 4TPB470M
3.3	TPS54616	Sanyo – 4TPB470M

Chapter 2

Setup and Test Results

This chapter describes how to properly connect, set up, and use the TPS54614 EVM. This chapter also presents the test results for the TPS54614, and covers efficiency, output voltage regulation, load transients, loop response, output ripple, and start-up.

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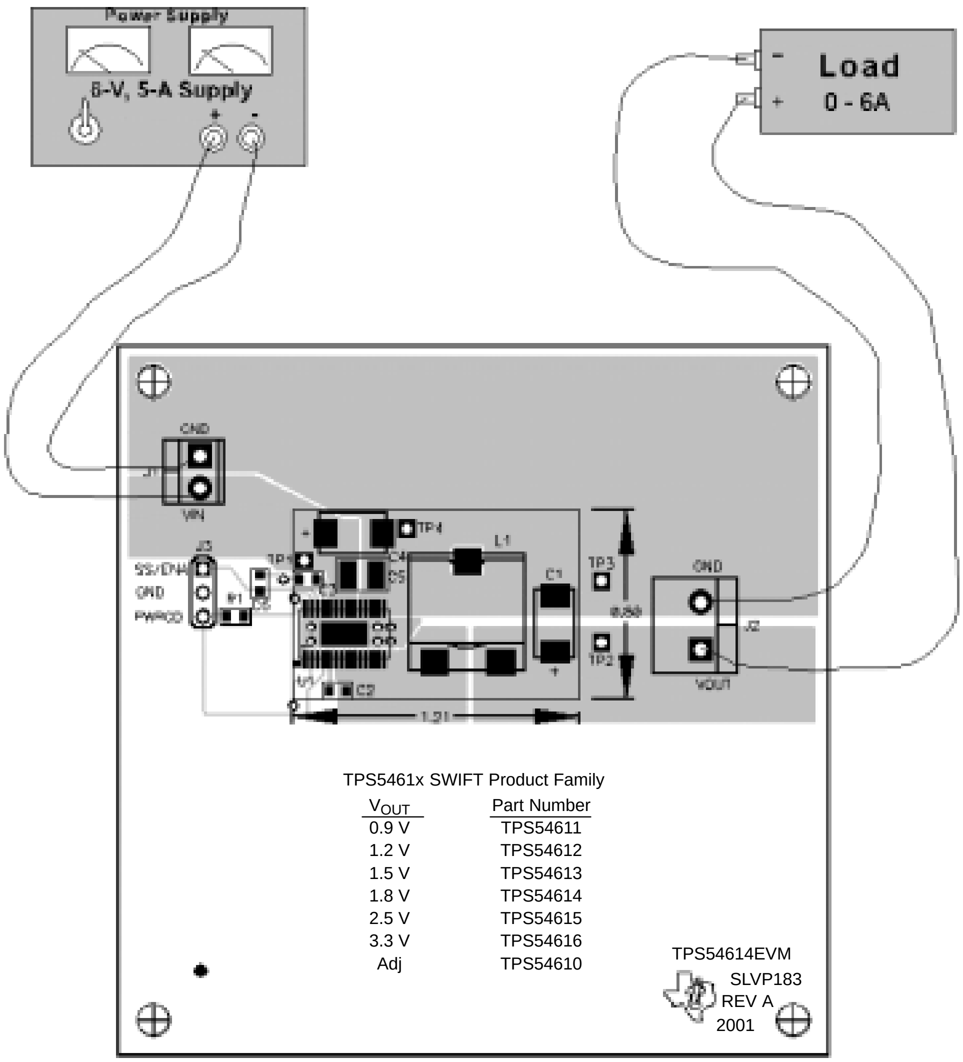
2.1 Input/Output Connections

The TPS54614 has the following four input/output connections: input, input return, output, and output return. A diagram showing the connection points is shown in Figure 2–1. Connect a power supply capable of supplying 5 A to J1 through a pair of 20 AWG wires. Connect the load to J2 through a pair of 16 AWG wires. Wire lengths should be minimized on both the input and output connections.

Figure 2–1. Test Setup Connection Diagram



NOTE: All wire pairs should be twisted.

2.2 Efficiency

The TPS54614 efficiency peaks at around 1.5 A of load current. At a full 6-A load the efficiency drops to around 83% with a 5-V input source. The efficiency shown in Figure 2–2 is typical for an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The total board losses are shown in Figure 2–3. The plots of Figure 2–4 and Figure 2–5 are extended out to current levels where the TPS54614 junction temperature reaches 125°C at 25°C ambient. When operating the TPS54614 past the 6-A maximum current rating, care should be taken to ensure that the maximum junction temperature does not exceed 125°C.

Figure 2–2. Measured Efficiency

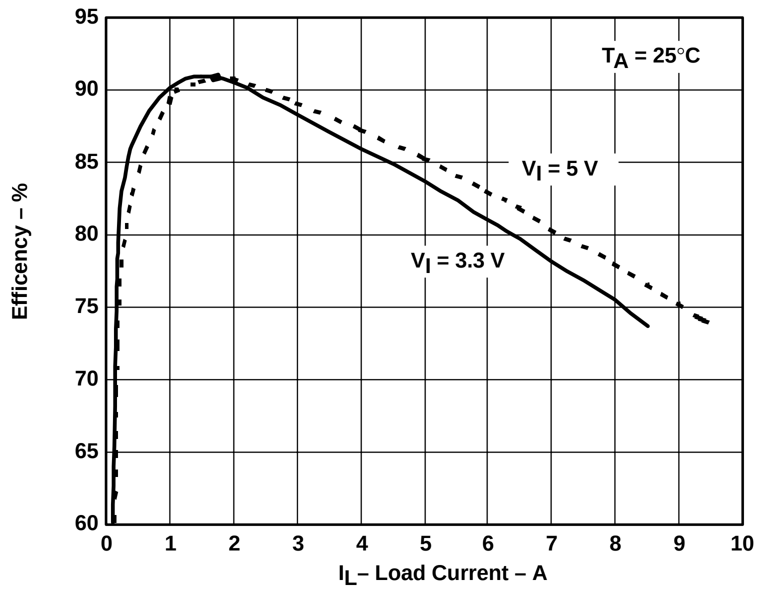
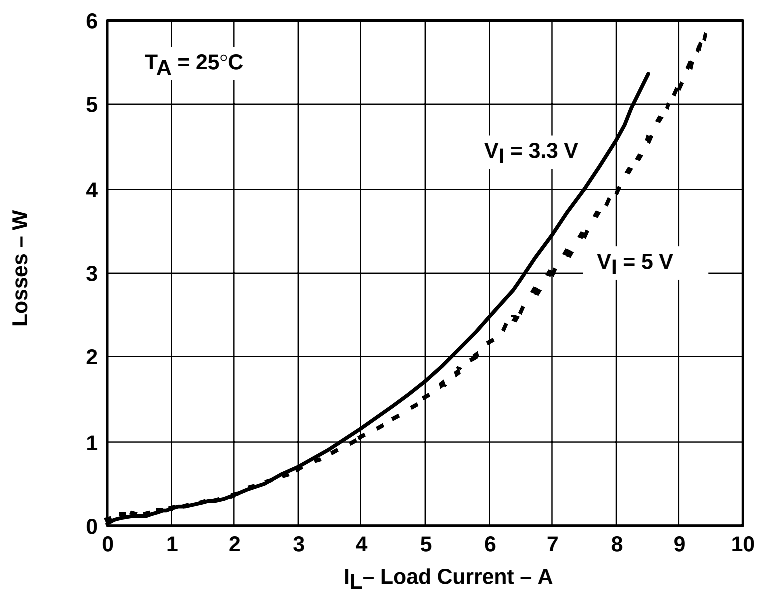


Figure 2–3. Measured Board Losses



2.3 Thermal Performance

The plot in Figure 2–4 shows the junction temperature versus the load current at 25°C ambient temperature. The case temperature is plotted in Figure 2–5. The low junction-to-case thermal resistance of the PWP package, along with a good board layout, helps to keep the junction temperature low at high output currents. With a 3.3-V input source and a 6-A load, the junction temperature is approximately 65°C, while the case temperature is approximately 59°C.

Figure 2–4. Measured Junction Temperature at 25°C Ambient

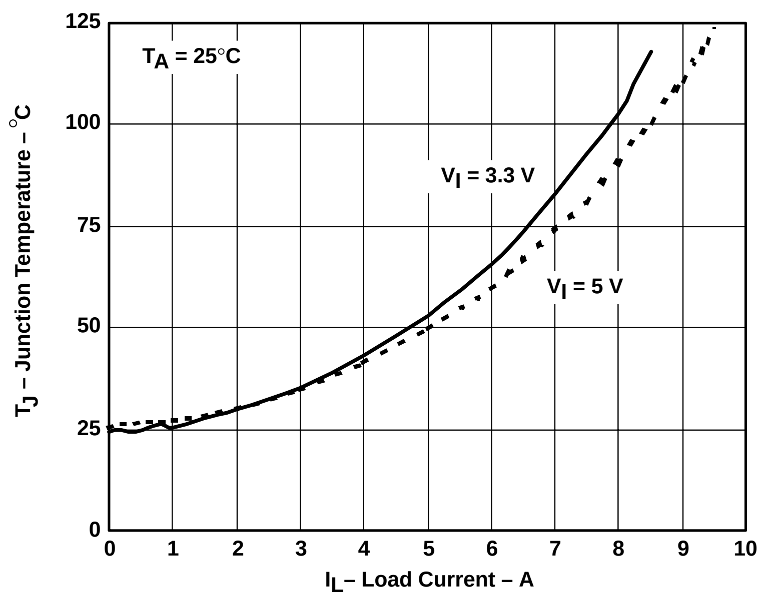
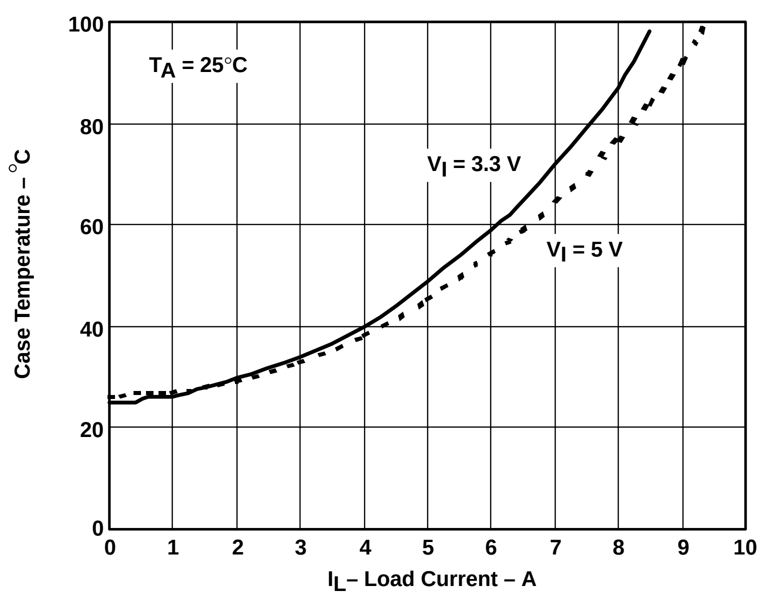


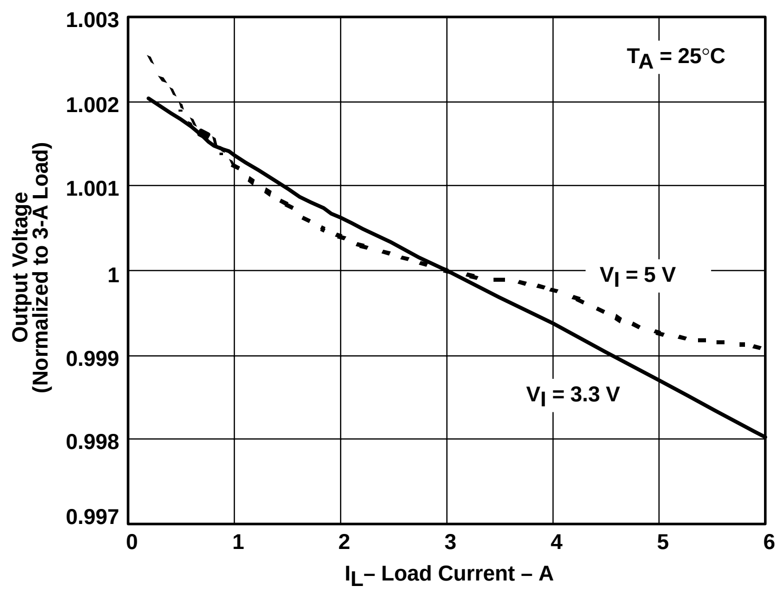
Figure 2–5. Measured Case Temperature at 25°C Ambient



2.4 Output Voltage Regulation

The output voltage load regulation at 25°C is shown in Figure 2–6. The output voltage varies less than 0.3% over the entire input voltage range of 3.3 V to 5.0 V, and load range of 0 A to 6 A.

Figure 2–6. Measured Load Regulation



2.5 Load Transients

The TPS54614 EVM response to load transients is shown in Figure 2–7 and Figure 2–8. The load transient in Figure 2–7 transitions from 1.5 A to 4.5 A in 16 µs, while the load transient in Figure 2–8 transitions from 4.5 A to 1.5 A in 12 µs. The transient response can be improved at the cost of adding additional capacitance to the output.

Figure 2–7. Measured Load Transient Response

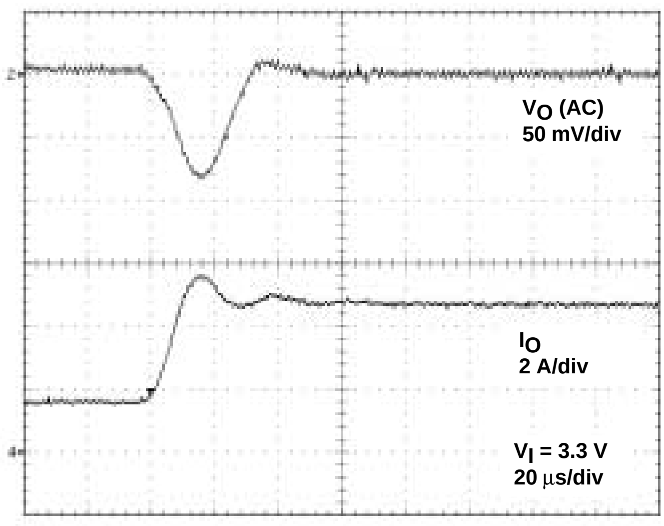
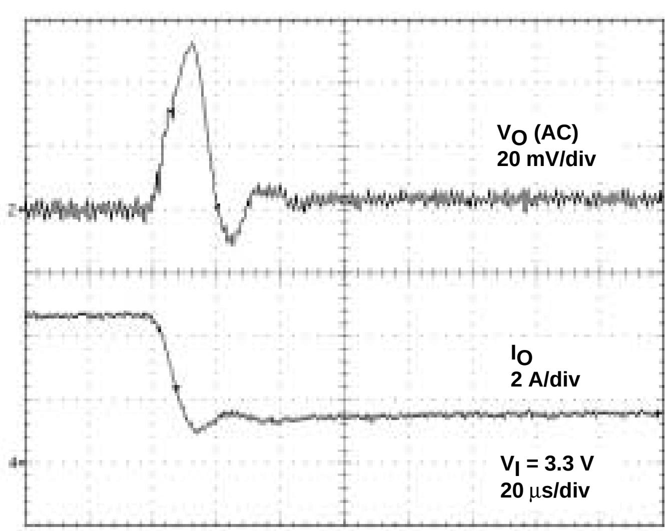


Figure 2–8. Measured Negative Load Transient Response



2.6 Loop Characteristics

The loop gain and phase for a 5.0-V input and a 6.0-A load are shown in Figure 2–9 and Figure 2–10. The loop crossover frequency is approximately 50 kHz, and the phase margin is approximately 46°.

Figure 2–9. Measured Loop Gain

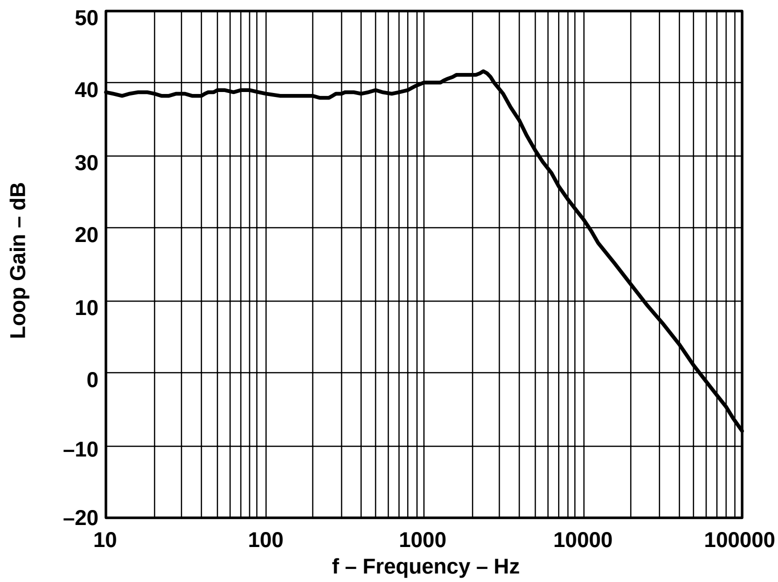
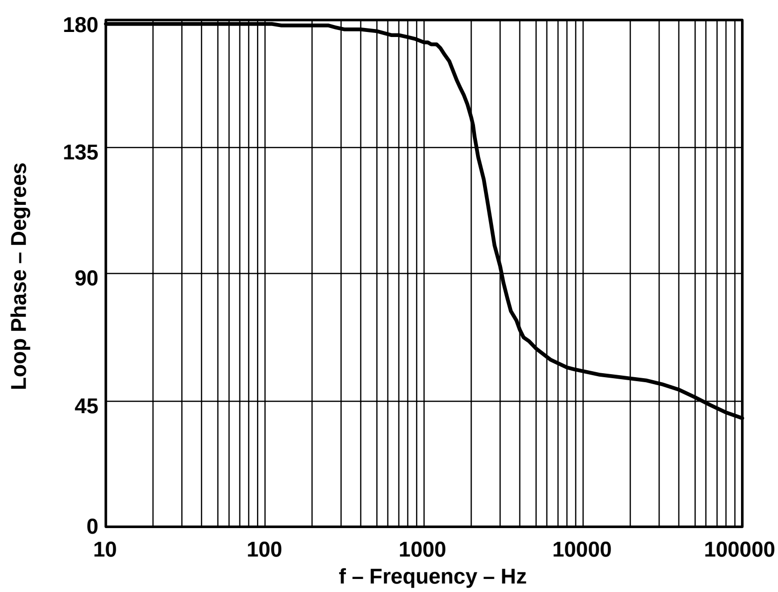


Figure 2–10. Measured Loop Phase



2.7 Output Voltage Ripple

The output ripple voltage is plotted in Figure 2–11 for a 3.3-V input, and in Figure 2–12 for a 5.0-V input. The TPS54614 has a typical output voltage ripple of less than 15 mV_{pp}.

Figure 2–11. Measured Output Voltage Ripple With 3.3-V Input

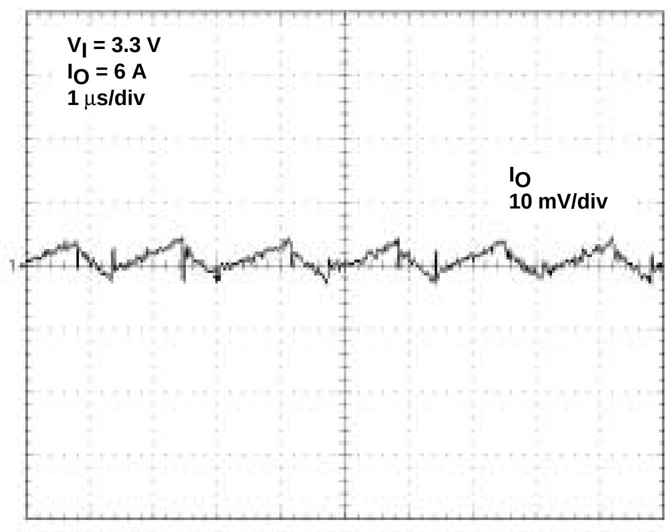
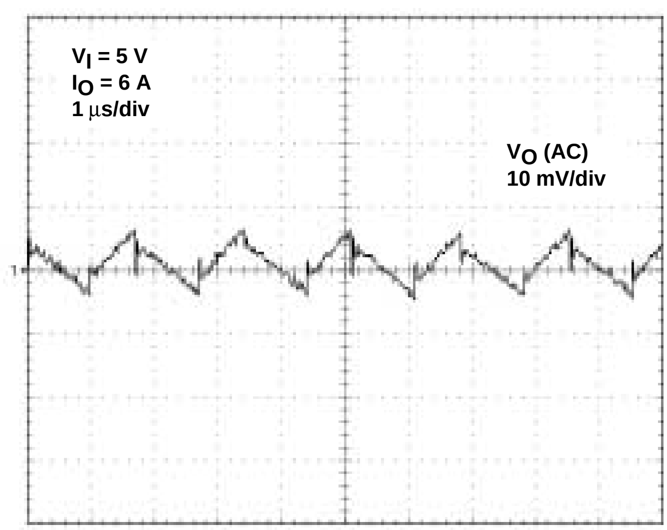


Figure 2–12. Measured Output Voltage Ripple With 5.0-V Input



2.8 Input Voltage Ripple

The input voltage ripple for a 6-A load is shown in Figure 2–13 for a 3.3-V input and in Figure 2–14 for a 5.0-V input. With a 5.0-V input, the ripple is approximately 260 mVpp. The input voltage ripple can be made lower by adding capacitance to the input.

Figure 2–13. Measured Input Voltage Ripple With 3.3-V Input

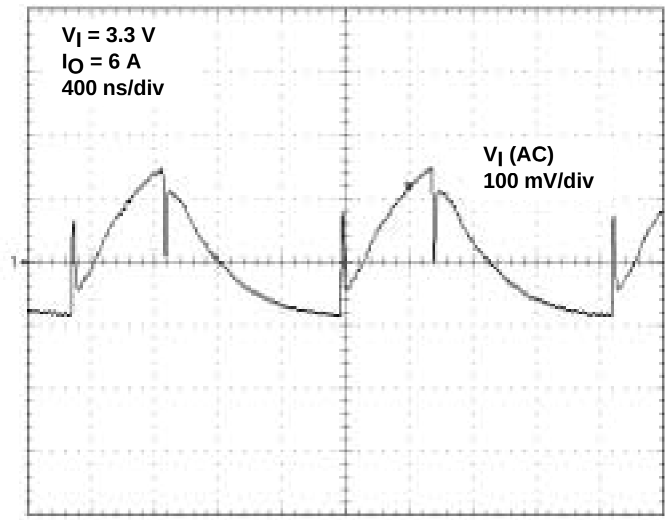
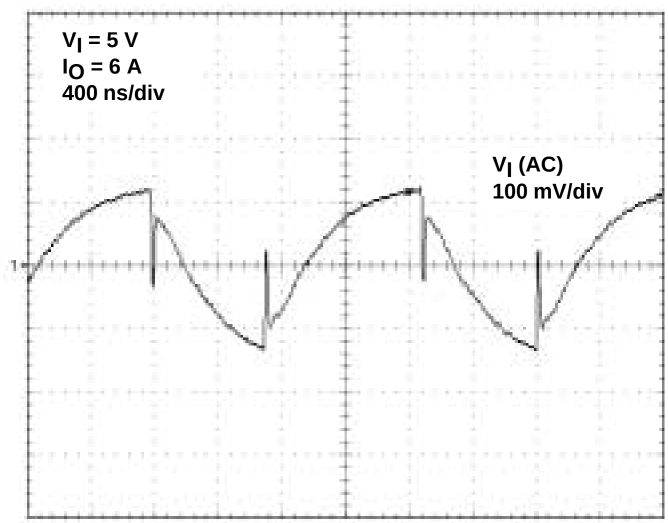


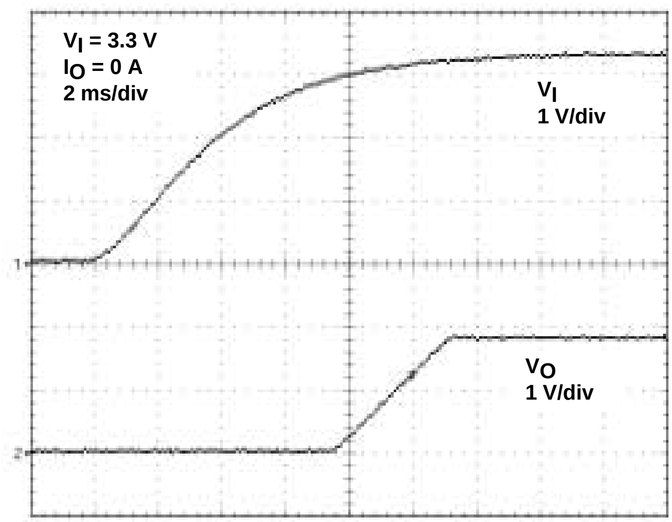
Figure 2–14. Measured Input Voltage Ripple With 5.0-V Input



2.9 Start-Up

The start-up voltage waveform of the TPS54614 EVM is shown in Figure 2–15. The TPS54614 output begins to rise when the input rises above the 3.0-V startup level. The output voltage then ramps linearly to 1.8 V in 3.6 ms. The start-up time is independent of input voltage and load. The slow start time can be made slower by using an external slow start capacitor (C6).

Figure 2–15. Measured Start-Up Waveforms



Chapter 3

Board Layout

This chapter provides the TPS54614 EVM board layout illustrations.

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3.1 Layout

The board layout for the TPS54614 EVM, shown in Figure 3–1 through Figure 3–4, resembles a layer stack-up encountered in a typical application. The top and bottom layers are 1.5 oz. copper, while the two internal layers are 0.5 oz. copper. The circuit components are confined to a small area of the circuit board. The two internal layers are identical and are used as *quiet* ground planes. The power ground plane is routed on the top layer, and is tied to the *quiet* (analog) ground planes at the output sense point (test point TP3). A wide power ground plane is used to keep the input ground current from injecting noise between the analog and power grounds. A total of 14 vias are used to tie the thermal land area under the TPS54614 to the internal ground planes and to the thermal plane on the back side of the board. The thermal plane on the back side occupies only the area directly underneath the regulator components, but should be made as large as possible in an actual application.

Figure 3–1. Top-Side Assembly

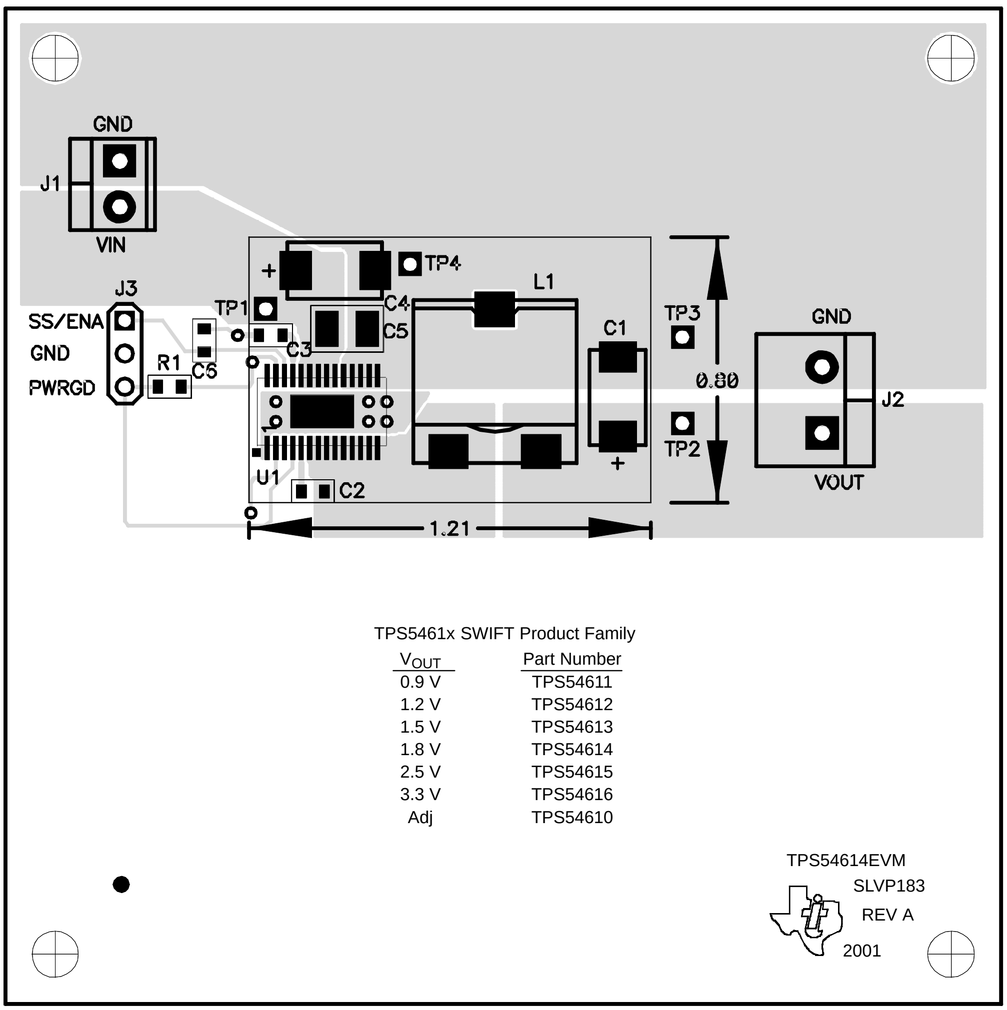


Figure 3–2. Top-Side Layout

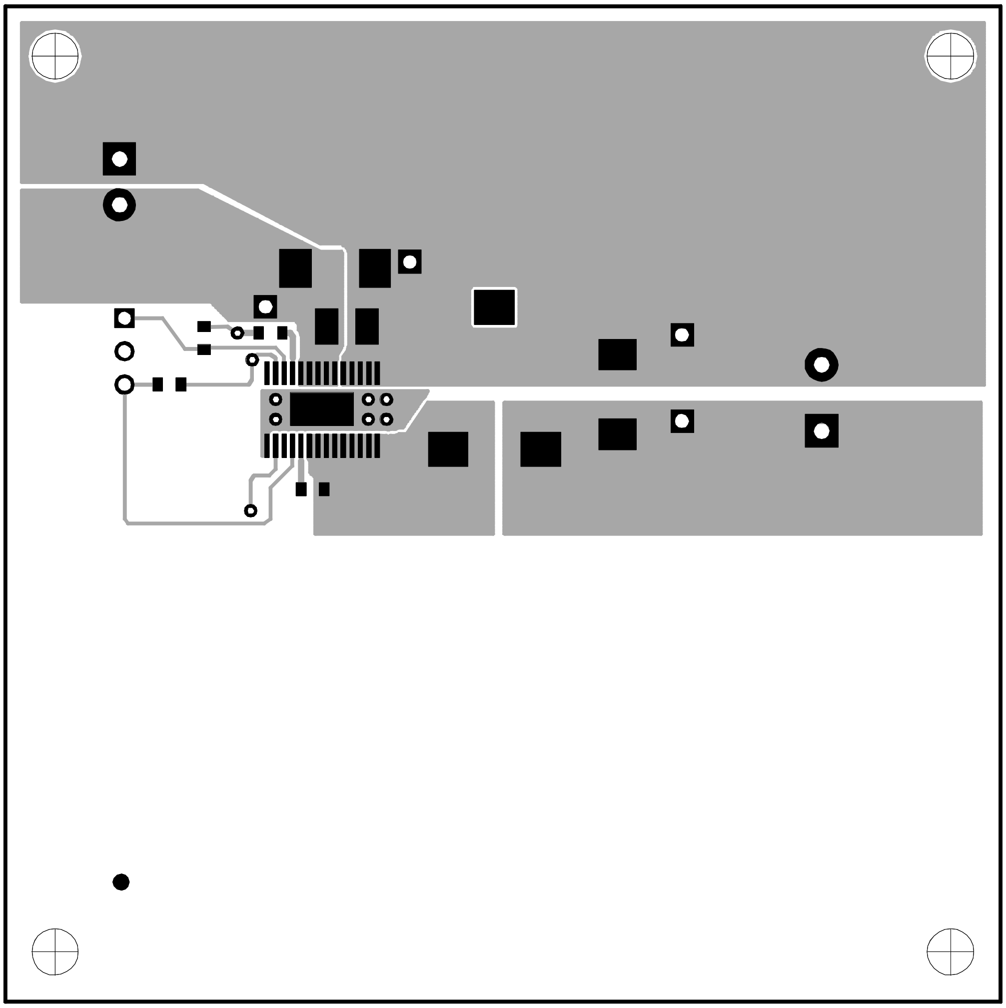


Figure 3–3. Internal Layers Layout

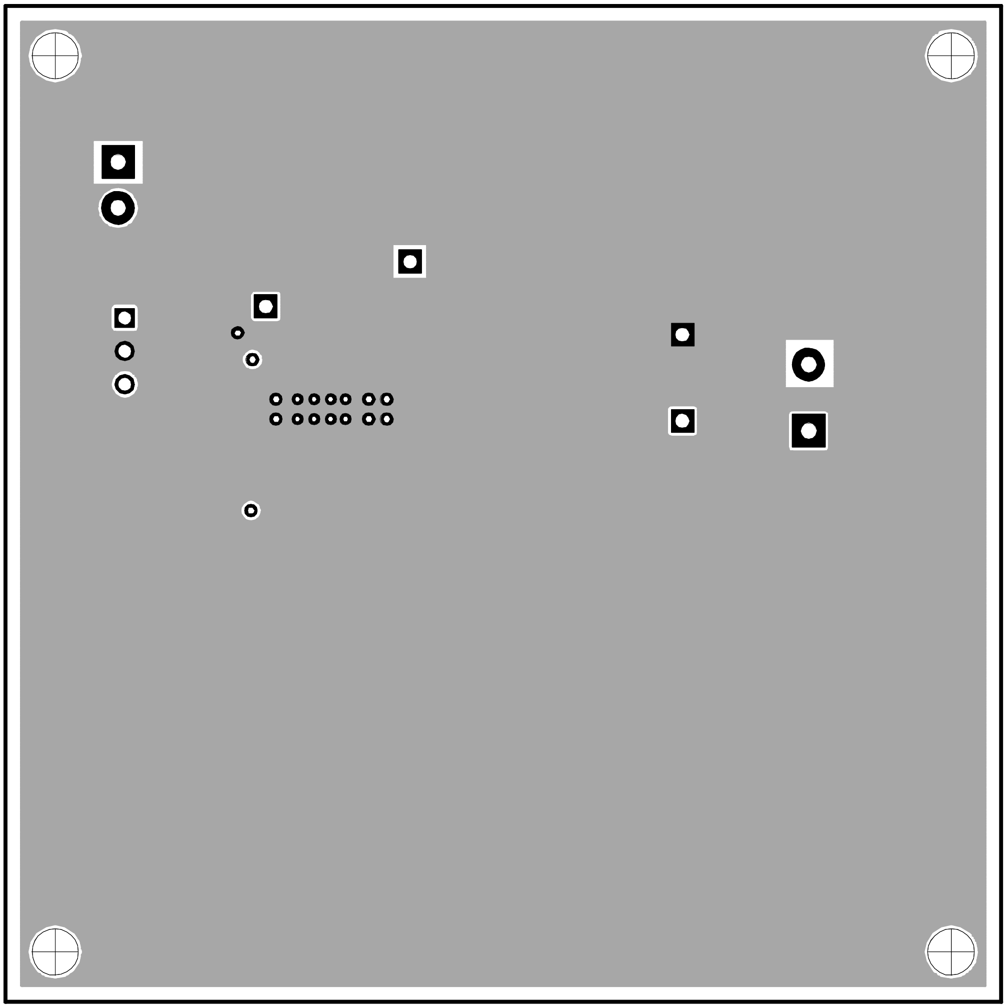
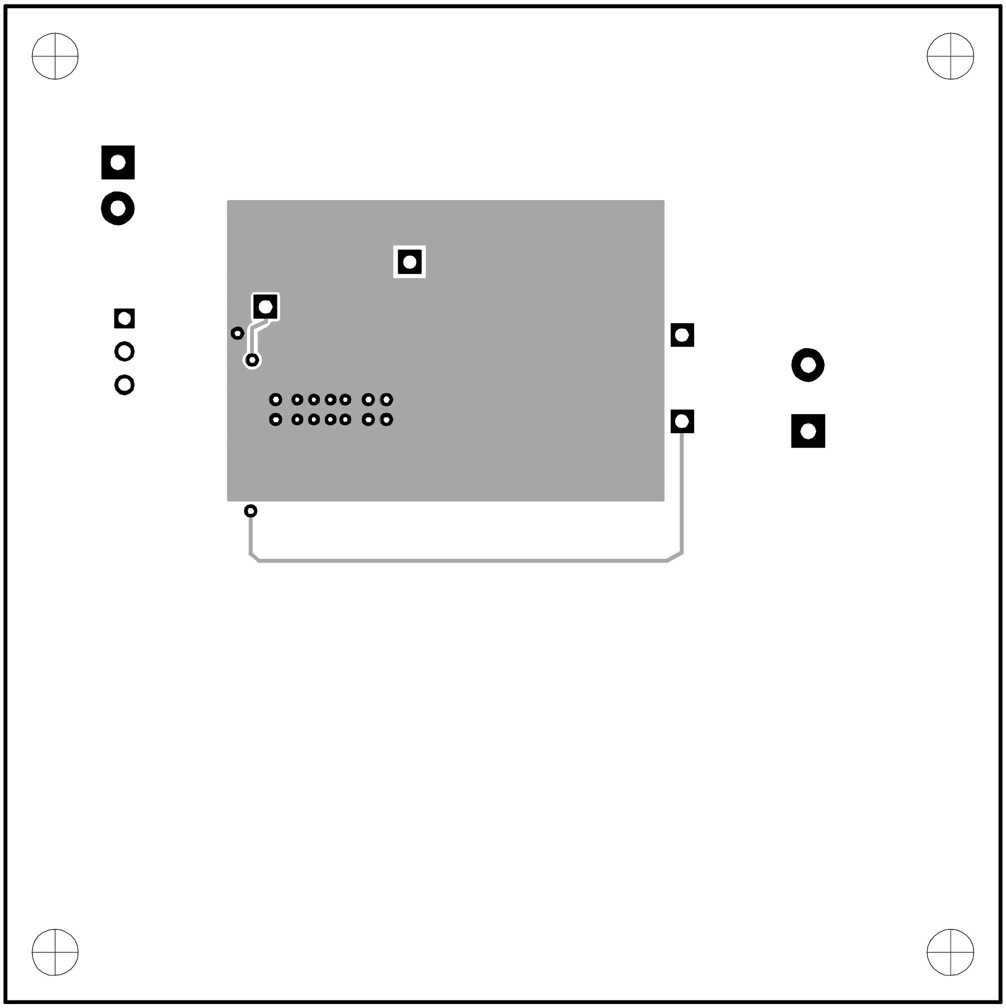


Figure 3–4. Bottom-Side Layout



Chapter 4

Schematic and Bill of Materials

This chapter provides a schematic diagram and bill of materials for the TPS54614 EVM.

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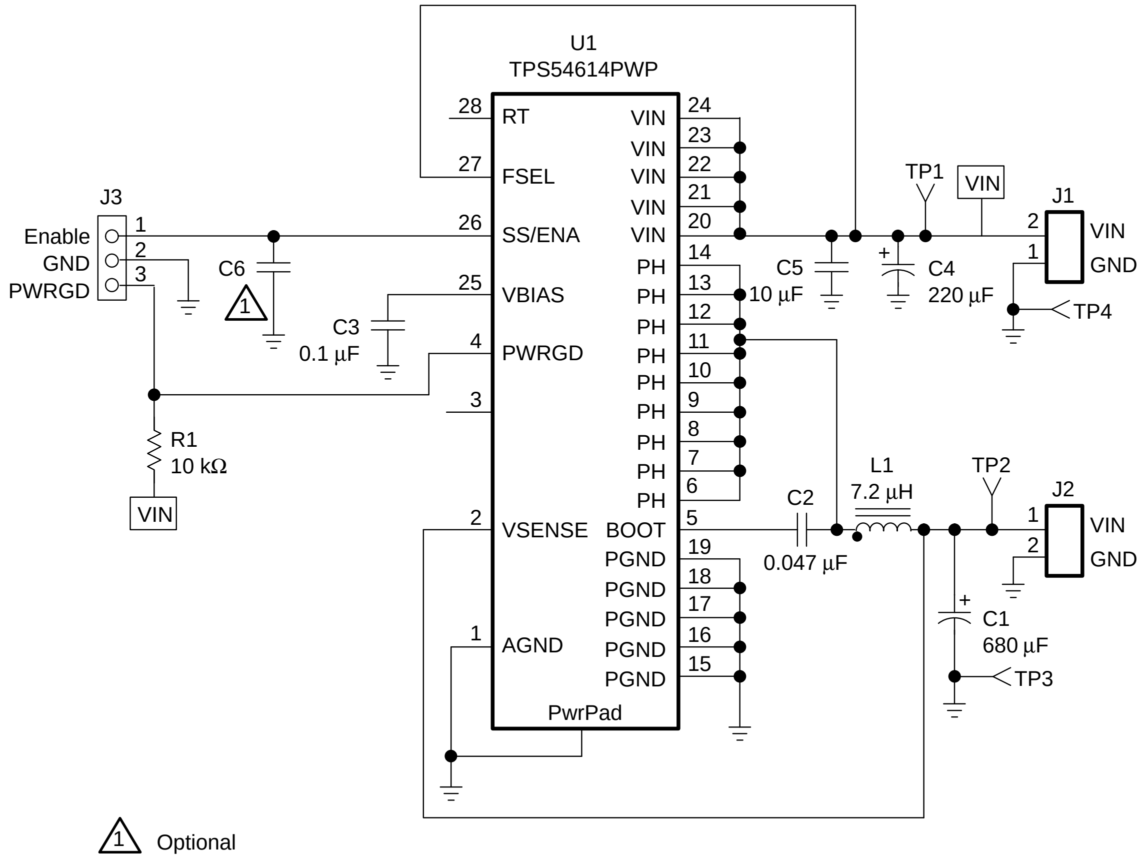
4.1 Schematic

Figure 4–1. EVM Schematic



4.2 Bill of Materials

Table 4–1. TPS54614 EVM Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, POSCAP, 680-µF, 2.5-V, 40-mΩ, 20%	7343 (D)	Sanyo	2R5TPB680M
1	C2	Capacitor, ceramic, 0.047-µF, 25-V, X7R, 10%	603	Murata	GRM39X7R473K25
1	C3	Capacitor, ceramic, 0.1-µF, 25-V, X7R, 10%	603	Murata	GRM39X7R104K25
1	C4	Capacitor, POSCAP, 220-µF, 10-V, 40 mΩ, 20%	7343 (D)	Sanyo	10TPB220M
1	C5	Capacitor, ceramic, 10-µF, 10-V, X5R, 20%	1210	Panasonic	ECJ–4YB1A106K
–	C6	Open (Unpopulated)	603		
1	J1	Terminal block, 2-pin, 6-A, 3,5 mm	0.27 × 0.25	OST	ED1514
1	J2	Terminal block, 2-pin, 15-A, 5,1 mm	0.40 × 0.35	OST	ED1609
1	J3	Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 7.2-µH, 7.8-A, 13.5 mΩ	0.492 sq	Sumida	CEP125(H)–7R2
1	R1	Resistor, Chip, 10 kΩ, 1/16-W, 1%	603	Std	Std
2	TP1, TP2	Test Point, red, 1mm	0.038	Farnell	240–345
2	TP3, TP4	Test Point, black, 1mm	0.038	Farnell	240–333
1	U1	IC, SWIFT™ power controller, 1.8-V, 6-A	PWP28	TI	TPS54614PWP
1	—	Shunt, 100-mil, black	0.100	3M	929950–00
1	NA	PWB, 4 layers, 1 1/2 ounce copper	3.00 × 3.00	Any	SLVP183