Application Report
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Designing a High-Efficiency WCDMA BTS Using TI GC5322 Digital Pre-Distortion Processor

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ABSTRACT

Efficiency is a primary concern in wireless communications and many other industries. Most often, this sought after efficiency comes at a financial cost. The cellular industry is no different from other business in its efforts to reduce cost by maximizing efficiency. In the cellular industry, a large portion of the costs are attributed to base stations. The base station is the infrastructure that is responsible for transmitting and receiving speech and data between cellular devices. A significant portion of the costs are attributable to the high power amplifiers (HPA) located within these infrastructures. When a power amplifier (PA) is operating at higher efficiency, the linearity of the PA is adversely affected. The motivation for this work is to maximize the efficiency and linearity of HPAs; thus, breaking the adverse relationship between the two.

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1 Introduction

The rapidly increasing number of mobile communication system users has driven the demand for spectrally efficient modulation schemes. In first-generation systems, constant envelope modulation techniques such as frequency modulation (FM) were employed because they allowed the power amplifier (PA) to operate near saturation with increased PA efficiency. These modulation techniques do not generate spectral regrowth or inter-modulation distortion (IMD) products in the nearby channels; however, they are spectrally inefficient with low data to bandwidth ratios. Wireless communication systems share a common transmission medium; thus, maximizing the amount of information that can be carried over a particular bandwidth will have a positive impact on overall profit margins. Second-generation systems addressed the problem with the introduction of time domain multiple access (TDMA) modulation schemes. These schemes allowed for multiple users to be multiplexed over a particular bandwidth, in Global System for Mobile Communications (GSM) as many as eight users were multiplexed. Finally, the growth in users stimulated the development of varying envelope modulation schemes that are now seen in third-generation (3G) systems. Non-constant envelope digital modulation techniques such as universal mobile telecommunications system (UMTS), code division multiple access (CDMA) and wideband CDMA (WCDMA) are spectrally more efficient [1]; however, they are subject to severe IMD when the PAs are

operated near saturation. The increase in channel capacity has driven the need for linear PAs; therefore, the increased spectral efficiency has resulted in less efficient PAs. Higher linearity is necessary because distortion is strictly limited by FCC and ETSI regulations that define maximum levels for adjacent channel leakage ratio (ACLR). A second type of distortion resulting from nonlinear operation is harmonic distortion, contrary to IMD, this appears far from the fundamental band and is easily filtered out.

The most recent advances in modulation techniques have also favored the trend towards multi-carrier power amplifiers (MCPA) in base station architecture. As opposed to single carrier power amplifier, which requires expensive combiners to achieve equivalent bandwidth, MCPAs are more cost effective and scalable. However, they are predisposed to the tradeoff between linearity versus efficiency. A simple method to maintain linearity is to operate the PA at a lower average power level; this technique is referred to as *backoff*. The term *headroom* is used to indicate the difference between average power and saturation level at the output of a PA. The backoff technique increases the amount of headroom, thus decreasing efficiency. A second obvious disadvantage to this technique is the increased cost of a more powerful amplifier with a higher saturation level. The inefficiency of these HPAs also contributes to cooling problems within the base stations due to high power dissipation.

There are linearization techniques [2]–[4] that allow a PA to be operated at higher power with minimal ACLR to meet efficiency and linearity requirements. Since power and cost are directly related, linearization allows for a lower-cost more-efficient PA to be used in place of a high-cost less-efficient PA. PAs in the field today are predominately linearized by some form of feed forward technology, a concept originally proposed by Black during the 1930's [5]. In recent years, there has been growing interest in linearization by digital pre-distortion (PD). Compared to feed forward, designs based on digital pre-distortion are showing higher efficiency at lower cost, and with recent advances in technology, digital pre-distortion can now support signal bandwidths in excess of 20MHz. Adaptive Pre-Distortion (PD) designs use a feedback signal to compensate for variations in the PA nonlinearity over time.

This work describes the system implementation of a high efficiency WCDMA basestation using a Doherty PA architecture and the TI DPD solution including the GC5322/5 (DUC-CFR-DPD), TMS320C6727, DAC5682Z, TRF3703-33, CDCM7005, TRF3761, and ADS61B49. The system used for testing is illustrated in Figure 1.

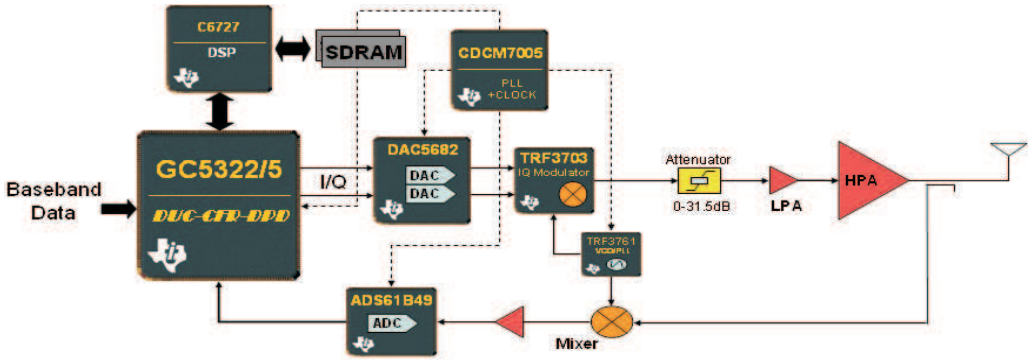


Figure 1. GC5322/5 Digital Pre-Distortion System

1.1 Power Amplifier Definition

A key element in the system definition is the power amplifier, there are numerous architectures preferred in the wireless infrastructure marketplace including: class A, class B, class AB, Doherty, envelope tracking, etc. It is important to understand the specific tradeoffs in selecting one architecture over another. The class A amplifier shows significantly high linearity but at lower efficiency – this PA is still suited for >40MHz signal bandwidth. Conversely, the Doherty PA offers a more challenging design and thus reduces the available signal bandwidth however significantly increases the PA efficiency. Additional PA design techniques but are not the focus of this investigation.

The PA architecture versus theoretical efficiency tradeoffs are illustrated in Figure 2, the tradeoffs are subject to the specific bias conditions for the given architecture.

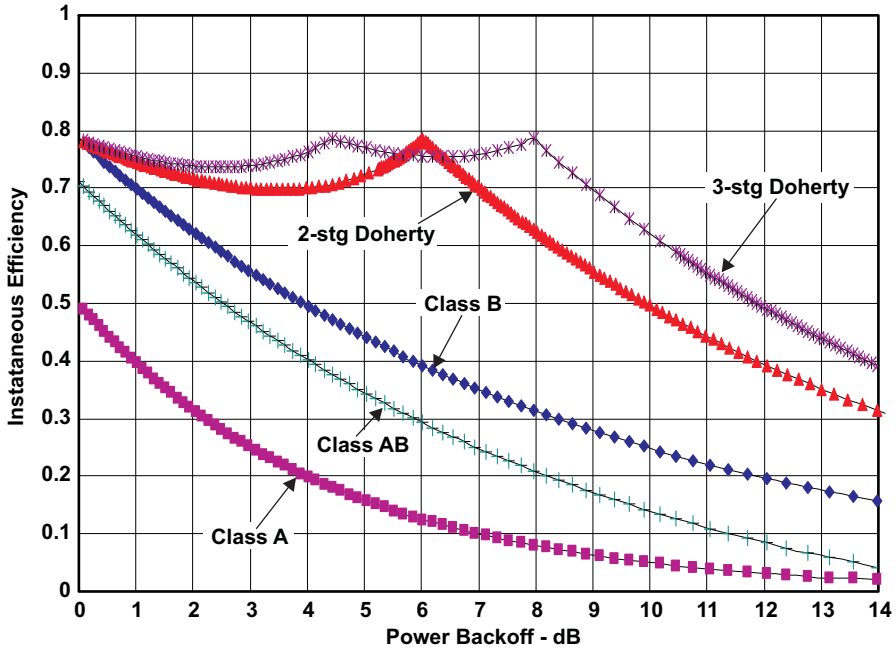


Figure 2. Instantaneous Efficiency vs Back-off for Different PA Architectures

While in theory, a 2-Stage Doherty PA can achieve beyond 65% efficiency, practical implementations fall short of this mark. Attached in Figure 3 are efficiency results achieved with a Doherty PA using a 2x BLF6G22LS-130 fixture provided by NXP Semiconductors. Additional testing reveals a peak power capability of 55dBm; therefore, the PA efficiency at 48.5dBm (6.5dB backoff) is approximately 40%.

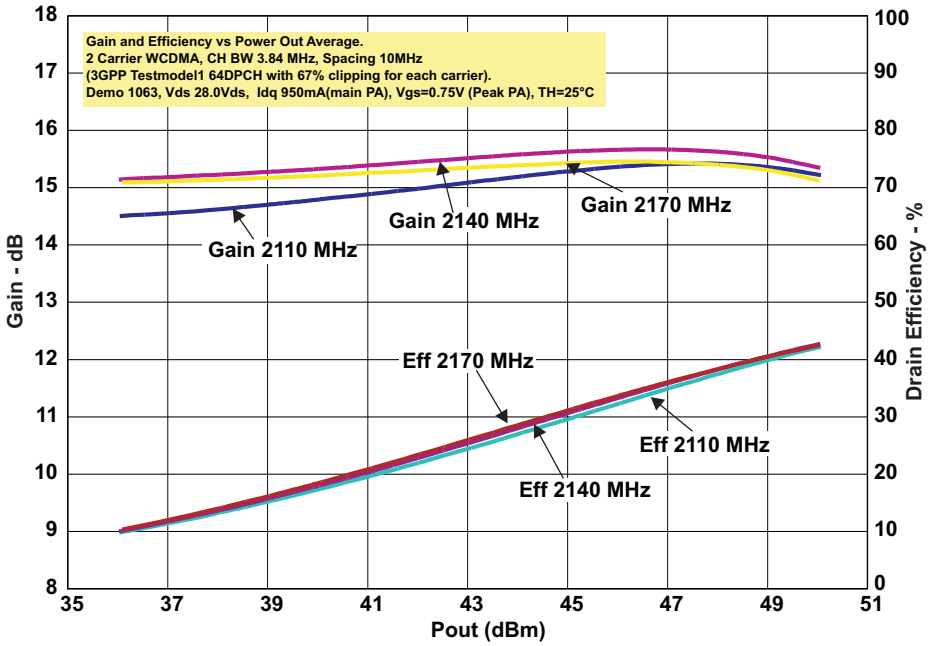


Figure 3. Efficiency and Gain vs Pout for a 2x130W Doherty LDMOS PA

1.2 WCDMA Specifications

The system is designed to meet and exceed WCDMA specifications as defined by Release 9 of the 3GPP specifications www.3gpp.org in TS 25.104 V9.1.0. The reader is encouraged to consult available documentation for additional conformance details. To meet base transceiver station (BTS) requirements, the system must maintain the following specifications:

Table 1. 3GPP Specifications for WCDMA

SPECIFICATION	TEST CONDITIONS	REQUIREMENT
EVM	TM1-QPSK / TM5-16QAM	≤17.5% / 12.5%
PCDE	TM3-32DPCH(1) w/ spread factor = 256	≤ –33 dB
RCDE	TM6-64QAM w/ spread factor = 16	≤ –21 dB
ACLR3	All transmission modes specified by the manufacturer.	≥45 dB
ACLR5		≥ 50 dB

(1) DPCH = dedicated physical channel

Emissions shall not exceed the maximum level specified in Table 2 for a BTS with maximum output power > 43dBm, in the frequency range from Δf = 2.5 MHz to Δf_{max} from the carrier frequency, where:

- Δf is the separation between the carrier frequency and the nominal –3dB point of the measuring filter closest to the carrier frequency.
- F_offset is the separation between the carrier frequency and the center of the measuring filter.
- f_offsetmax is either 12.5 MHz or the offset to the UMTS Tx band edge, whichever is the greater.
- Δf_{max} is equal to f_offsetmax minus half of the bandwidth of the measuring filter.

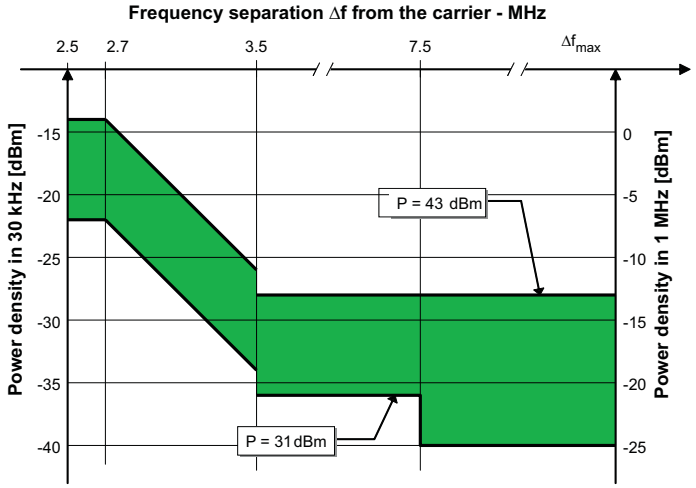


Figure 4. 3GPP Spectrum Emissions Mask for WCDMA

Table 2. 3GPP Specifications for WCDMA Spectrum Emissions with BTS Maximum Output Power P ≥ 43dBm

Frequency Offset of Measurement Filter –3dB Point, Δf	Frequency Offset of Measurement Filter Center Frequency, f_offset	Minimum Requirement	Measurement Bandwidth
2.5 MHz ≤ Δf < 2.7 MHz	2.515 MHz ≤ f_offset < 2.715 MHz	–14 dBm	30 kHz
2.7 MHz ≤ Δf < 3.5 MHz	2.715MHz ≤ f_offset < 3.515 MHz	$-14\text{dBm} - 15 \times \left(\frac{\text{f\_offset}}{\text{MHz}} - 2.715\right)\text{dB}$	30 kHz
See (1)	3.515 MHz ≤ f_offset < 4.0 MHz	–26 dBm	30 kHz
3.5 MHz ≤ Δf ≤ Δf_{max}	4.0 MHz f_offset < f_offset_{max}	–13 dBm	1 MHz

(1) This frequency range ensures that the range of values of f_offset is continuous.

2 System Architecture and Characterization for Pre-Distortion

2.1 Digital Up-Converter

The GC5322 processor includes digital up-conversion (DUC) filtering which allows the user to provide low-rate baseband data to the device which is then interpolated and filtered to a higher, more desirable rate. The block also includes numeric controlled oscillators (NCOs) used to tune the carrier frequency to the desired location.

There are 2 DUC blocks in the GC5322; each can be configured for 1, 2, or 6 channels. The DUC consists of a Programmable FIR Filter (PFIR), Compensating FIR Filter (CFIR), Cascade Integrator Comb Filter (CIC), Delay Filter, and Mixer. There is a sum chain at the output of the two DUC sections as shown in Figure 5. The DUC for WCDMA applications uses the 2 channels per DUC mode.

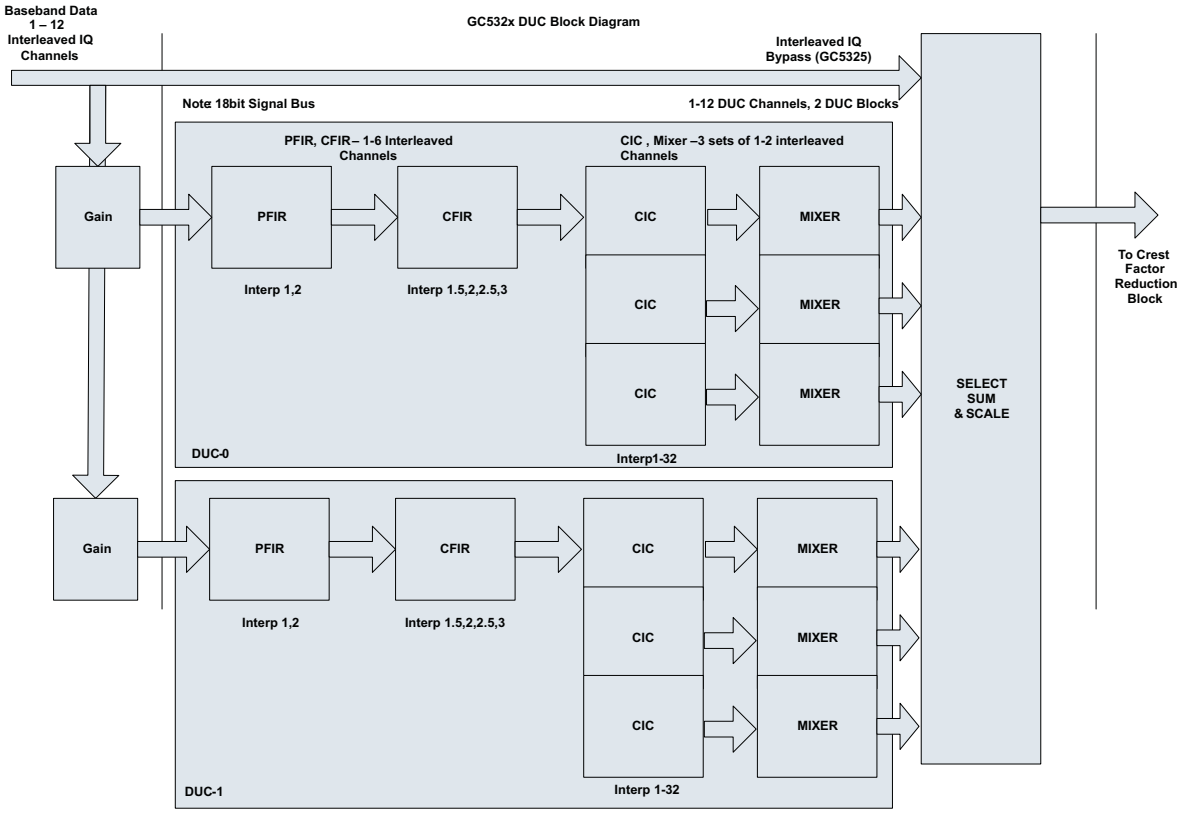


Figure 5. Digital Up-Converter Block Diagram

The WCDMA application interpolation is PFIR Interpolate by 2, CFIR Interpolate by 2, and CIC Interpolate by 4 resulting in a total interpolation ratio of 16. The channel filter is a convolution of the PFIR, CFIR, CIC, and Delay filters. The DUC spectral response is a combination of the channel filter and the baseband input spectral shape.

There are several methods to design the PFIR:

- Root Raised Cosine – pulse shaping filter (best Passband_ripple – lowest EVM)
- Root Raised Cosine – pulse shaping with window (improves ACLR, higher EVM)
- Root Raised Cosine – pulse shaping and Low Pass filter (worst passband_ripple, best ACLR, higher EVM)
- Root Raised Cosine – pulse shaping, and trailing zeros, to reduce latency (best Passband ripple, higher EVM, lower latency)

In the WCDMA application, the PFIR has symmetric coefficients for 123 taps, or an asymmetric filter with 62 taps. If the application would like less latency, at the expense of higher EVM, an asymmetric 62 tap PFIR can be used. Figure 4 shows the spectral response of the 3 methods; Figure 6 shows the Passband Ripple of the DUC channel. The PFIR can be evaluated for demodulator error by interpolating by 2, and demodulating the TM1 data. The RRC has the lowest composite EVM.

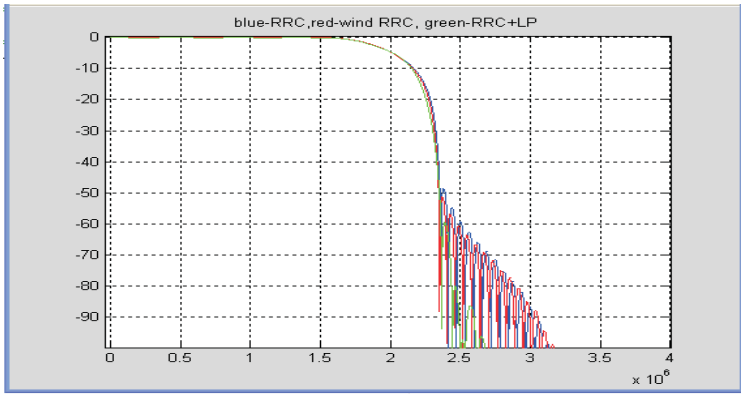


Figure 6. PFIR Filter Spectral Response

The PFIR RRC filter section is used to reduce Intersymbol Interference. The CFIR provides for CIC passband droop correction, and PFIR interpolation image suppression. The CFIR filter is designed as a low pass filter given the CFIR interpolate by 2, and the PFIR interpolation image. If the CFIR number of taps is lower, the slope becomes less. The selection of FPASS should be higher than the PFIR passband and the selection of FSTOP is within the valley of the null after the PFIR rolloff, and before the PFIR image as shown in Figure 7.

The PFIR RRC with the asymmetric PFIR is designed with enough RRC taps to meet the DUC EVM specification. Since there are up to 62 PFIR taps, we could have 59 RRC taps, followed by 3 zeros. The change in PFIR latency is estimated below:

PFIR Latency difference for Asymmetric 62 tap vs 123 tap symmetric filter, 4.1µsec.

Center tap time delay for symmetric filter ≥ 62 × $1/(7.68^6)$

Center tap time delay for asymmetric filter ≥ 30 × $1/(7.68^6)$

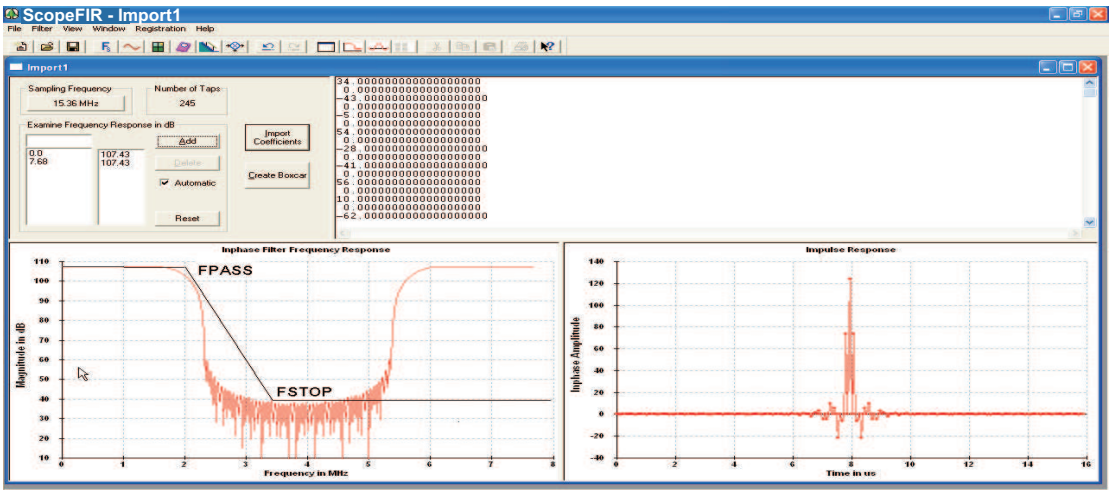


Figure 7. CFIR Filter Design

The CIC correction for the CFIR depends on the interpolation of the CIC filter, and how many comb stages use an M=2 factor. The M=2 stages have a higher stopband rejection, but also produce more droop at the PFIR and CFIR. In this application, 1 of the 6 CIC stages has an M2 = 1.

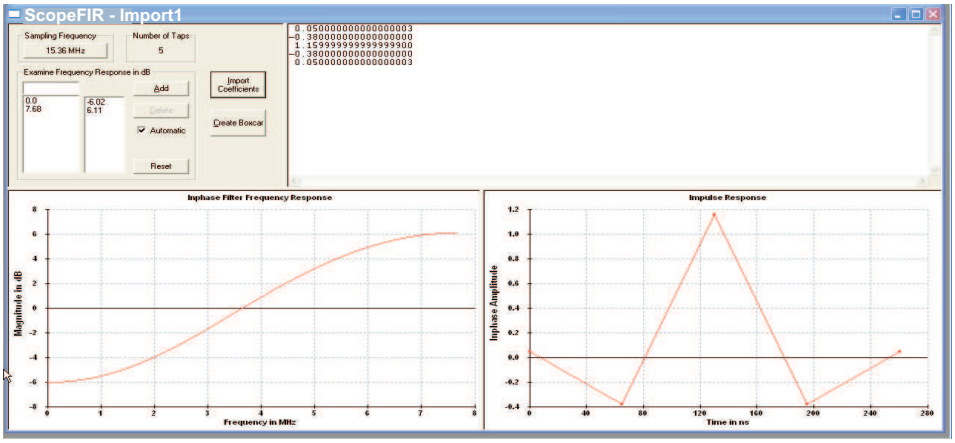


Figure 8. CFIR Filter including 5-tap CIC Correction

In the WCDMA application the CFIR interpolates by 2. The number of taps for the Low Pass Filter (LPF) is the total estimated number of taps – CIC Correction + 1. The CFIR filter hardware does not utilize symmetry. Figure 8 shows the DUC channel passband ripple which is directly affected by the CIC correction factor, interpolation, and M2 setting. Figure 9 shows the composite WCDMA channel, the CFIR FPASS and CFIR CIC Correction coefficients are used. In general, the CIC correction is done to keep the passband from 0 to 1.6MHz to within .5dB, also the 1.92MHz point between –2.5 and –3.5dB.

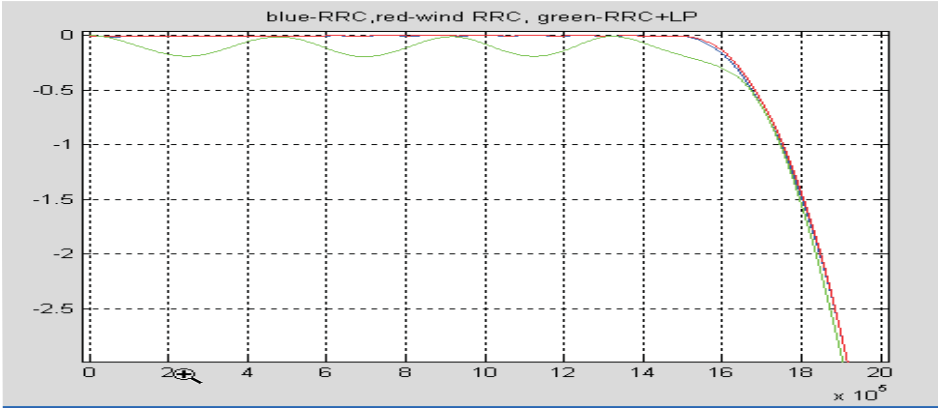


Figure 9. DUC Channel Passband Ripple

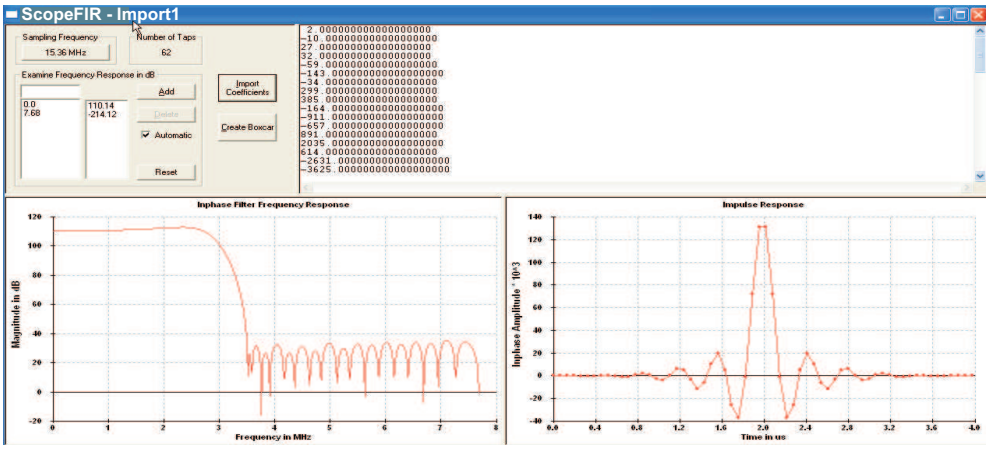


Figure 10. DUC CFIR Response

The Cascade Integrator Comb (CIC) filter is a bulk interpolation filter that utilizes differentiator and integrator stages. This implementation uses 6 stages, and the differentiator can have a delay (m) of 1 or 2 for each of the 6 stages. The number of stages with m2 enabled are the stages that have a delay of 2. The m2 enabled stages increase the stopband rejection of the CIC filter, but also requires more CFIR compensation for the CIC droop in the passband. Figure 11 shows the 6-stage CIC with m2 = 0 and interpolate by 4; Figure 12 shows the 5-stage CIC with m2 = 1. The CIC m2 = 1 is used for the CIC Correction coefficients in the above example.

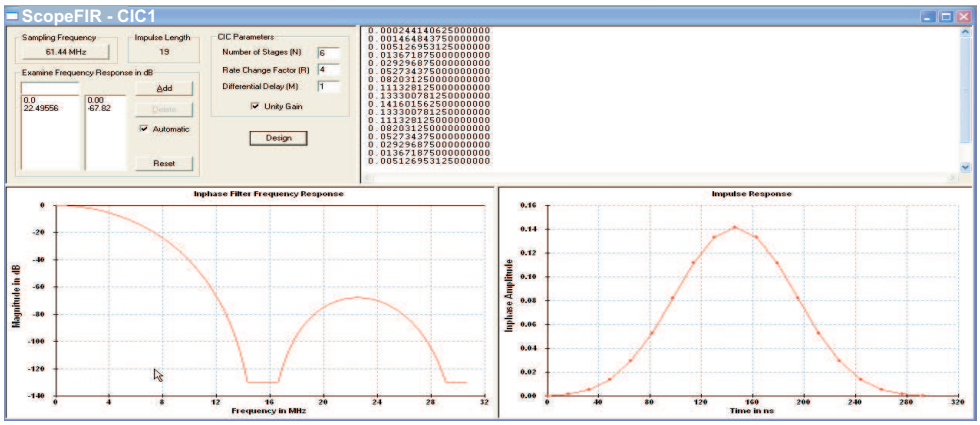


Figure 11. 6-Stage CIC Response (m2 = 0, Interpolate 4x)

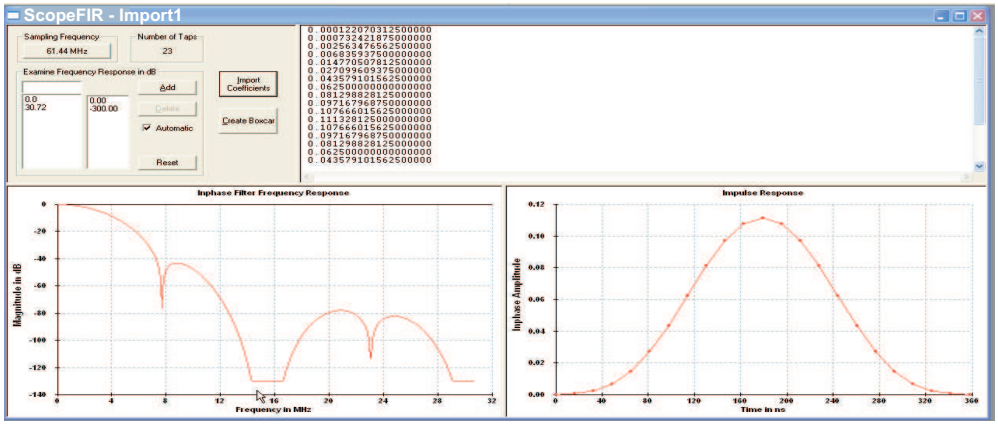


Figure 12. F6-Stage CIC Response (m2 = 1, Interpolate 4x)

The CIC also has channel specific offset controls that can be used to time-offset the DUC channels to decorrelate the peaks between carriers. The CIC has a cic_scale parameter that is used to shift the cic_differentiator value to the scale point for the cic integrator. The CIC must have an offset value that results in a gain <1. Reference 2 has a CIC gain equation that is used to set the cic_offset value. Usually the calculated value is lowered by 1 for delay filter compensation.

The delay filter is located between the CIC interpolation filter and the mixer. This filter is used in wideband DUC applications (interpolation <8) to increase the channel stopband rejection. In this application, the delay filter is set to 0.5, 0.5. Figure 13 shows the DUC channel response. It is important to verify the channel filter response as the ACLR value for WCDMA is directly related for the adjacent and alternate channel ACLR. Figure 14 shows the reduced latency DUC channel response, with the 62-tap PFIR. The only difference between the filters represented in Figure 13 and Figure 14 is the PFIR, this affects the close-in response.

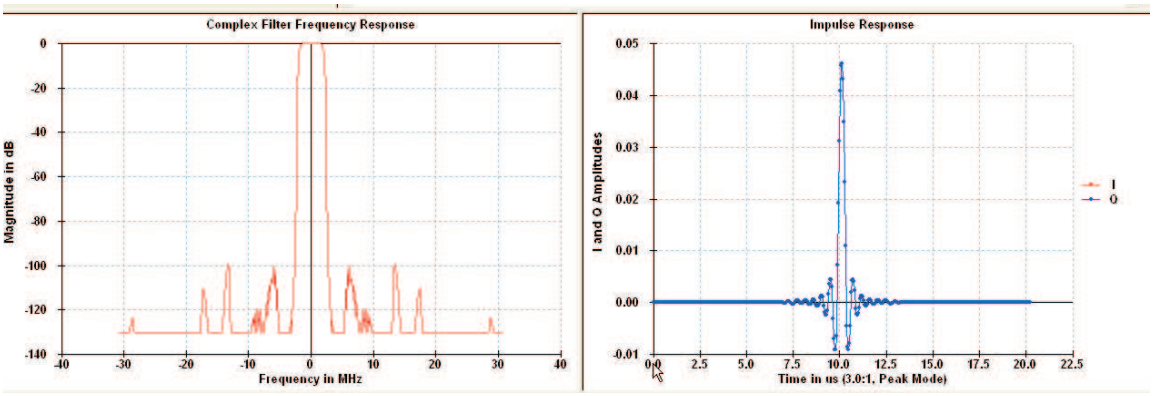


Figure 13. DUC Channel Response for PFIR2 123tap, CFIR2, CIC4m2=1

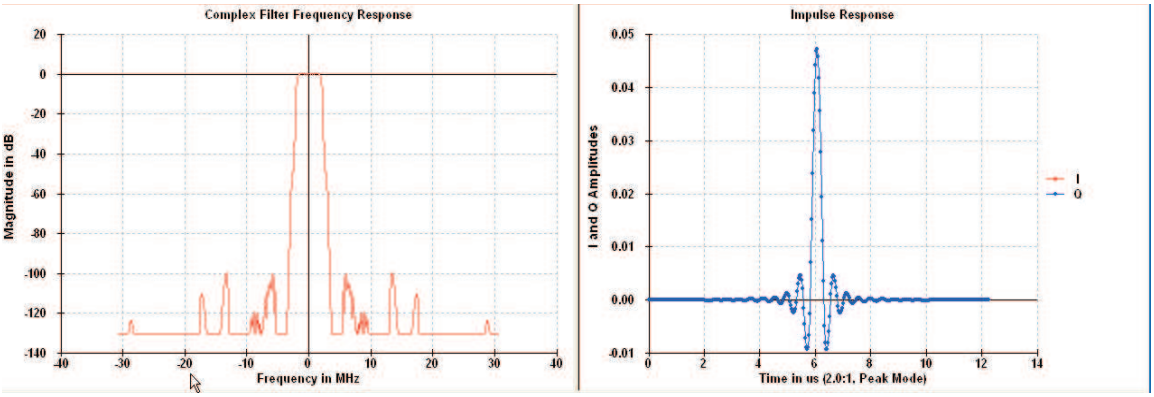


Figure 14. DUC Channel Response for PFIR2 62tap, CFIR2, CIC4m2=1

The sum chain is used to add the active DUC channels. When adjusting the gain for multicarrier DUC examples, the transmit behavior of each carrier should be individually observed before enabling all carriers. The sum chain has a compensation gain scale which ranges from +3 to –4. It is typically set to +1 for one carrier, 0 for two carriers, –1 for four carriers, –2 for 8 carriers as a starting value.

Several 2-carrier signals were generated to show that TM1-64, TM3-32, and TM5-30 have different peak-to-average power P(PAR) values as shown in Figure 15, Figure 16, and Figure 17. The setting of the baseband gain, sum scale gain, and CFR settings are discussed in the next section. The CFR settings in the next section, are used to reduce the peak PAR of the DUC signal. The three test model signals have different signal statistics, depending on the number of users, base modulation, coding, and scrambling code offsets. In Figure 15, Figure 16, and Figure 17 the DUC output was normalized to –1dB peak. This is the initial suggested value, the value can be lowered further due to the peak reduction in CFR, as the CFR output peak must be < –6.2dB.

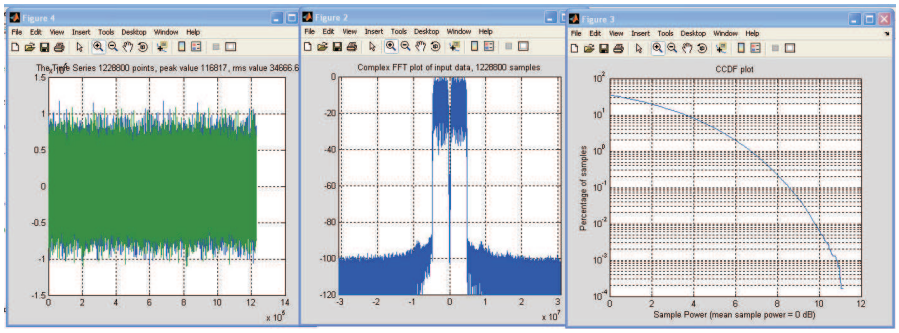


Figure 15. DUC Interpolate by 16, TM1

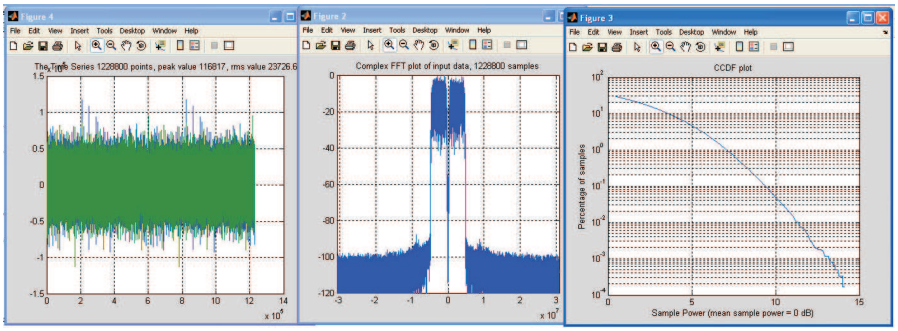


Figure 16. DUC Interpolate by 16, TM3-32

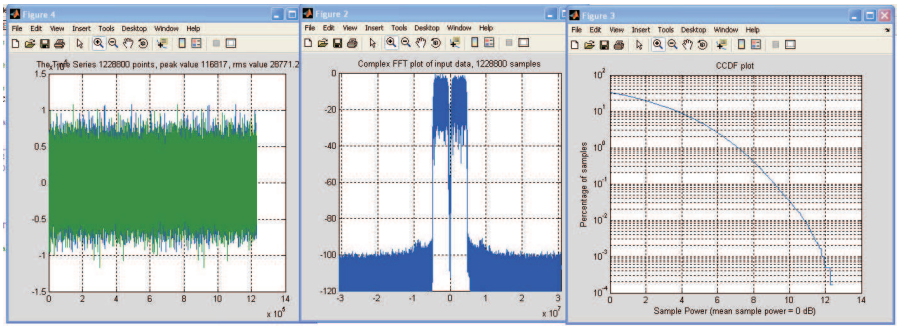


Figure 17. DUC Interpolate by 16, TM5-30

2.2 Crest Factor Reduction

As was illustrated in Section 1.1, the amount of back-off is critical to the expected efficiency from the PA. Signals with higher peak-to-average ratio (PAR) require additional analog headroom to avoid PA saturation. Alternately, the signal can be clipped to reduce the PAR and consequently reduce the required analog headroom.

The PAR of a given signal can be calculated using Equation 1 and typical mathematical manipulations where $\sigma(x)$ is the standard deviation of the signal x.

$$PAR = 20 \times \log_{10}(\max |x| / \sigma(x)) \quad (1)$$

The PAR of the transmitted signal is also often referred to as the crest-factor (CF) of the signal calculated as the peak-to-rms voltage. There exist numerous clipping techniques each with respective benefits and tradeoffs, Texas Instruments has implemented a subtracted time domain technique which effectively applies distortion to the signal without altering the spectral shape of the signal. The implemented technique does, however, degrade the error vector magnitude (EVM) of the original signal which can have equally negative consequences.

The CFR signal processing is applied following the DUC filtering, this allows a PAR reduction to be applied to the combined signal reducing the impact of peak regrowth occurring inside the DUC. The CFR block adds inband noise to the wideband signal from the DUC in order to reduce the peaks. The CFR block shown in Figure 18 has four stages of cancellation each sharing a pool 24 cancellers. The power meter can be used to monitor the integrated complex magnitude squared of the CFR input or output.

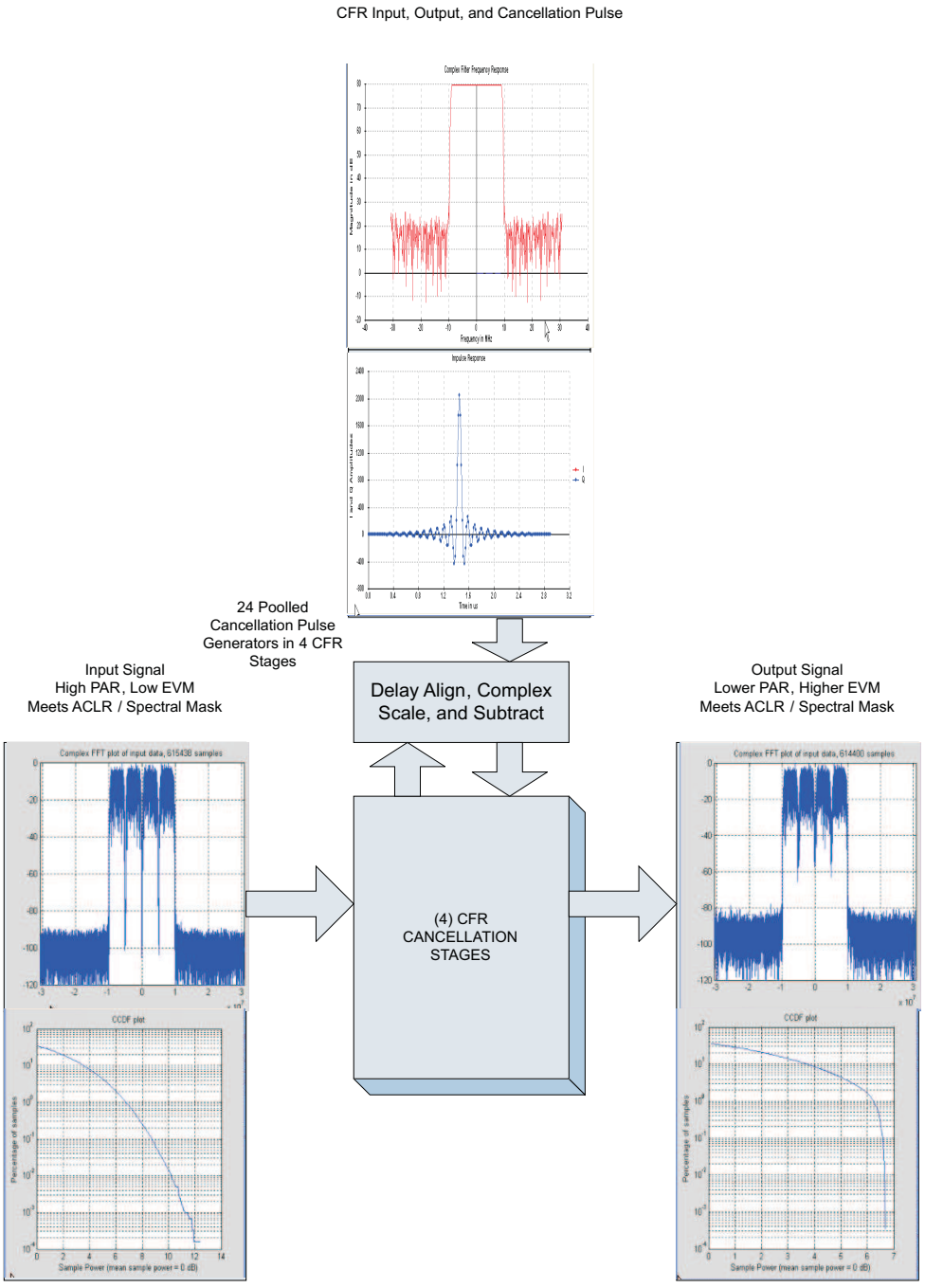


Figure 18. CFR Block Diagram

The configuration of the CFR settings can be divided into four tasks:

- Mode selection
- Coefficient bank utilization and dynamic coefficient updates
- Cancellation pulse design
- Peak detection and cancellation (PDC) setpoint and timeout setting

The CFR block has four operating modes: real unique, real mirror, complex unique and complex mirror. The real mirror mode is used for zero-IF based carrier configuration, it can support up to 509 coefficients. The complex mirror mode is used for multicarrier configurations with frequency gapped carriers, or if a single carrier is not centered at zero-IF. The complex mirror mode can have a maximum of 255 coefficients.

The CFR block has four coefficient RAM banks each used to store unique cancellation coefficients. The normal bank of coefficients is bank 0. There is an additional bank called the shadow coefficient bank which allows any of the four banks to be updated dynamically after the initial coefficients are loaded. A new set of CFR coefficients (in the same mode, with the same number of coefficients) could be updated without signal interruption. Under normal operating conditions, the filter bank selection can be used to toggle between dynamically varying signals and their respective cancellation filters.

The cancellation pulse design is based on creating a set of real or complex filter coefficients whose passband and transition band nearly mirror the input signal, the filter design has several considerations:

- The length of the cancellation pulse affects how often a pulse canceller is available. If the cancellation pulse is 503 taps in real mirror mode, it would take 509 clock cycles before the canceller could be reused; short cancellation pulses can make filter design challenging. The cancellation pulse stopband rejection needed is also a function of the clipping level; if the ACLR requirement is 55dB, and the canceller amplitude is applied at –15dB, the stopband rejection of the cancellation filter design should be at least 40dB.
- The cancellation pulse is typically designed as a low pass filter, or windowed sync pulse. In special configurations for multicarrier systems it can be a multiband filter. In complex mirror mode, the base filter is a low pass or sync filter, which is modulated by the mixer frequencies of the carriers, and the accumulated complex cancellation pulse (up to 247 taps) is used. In the multiband real filter and the complex filter, the amplitude in different sections of the cancellation pulse can be modified to optimize CFR further.

A cancellation pulse design is done with a real prototype filter for a single or combination of contiguous carriers. The cancellation pulse design needs to consider the ACLR of the desired signal in multicarrier contiguous positive spectrum. In Figure 20 a low pass filter design of 179 taps is shown, for a single WCDMA carrier with a stopband rejection of 45dB and the passband ripple of 1dB. The passband frequency is adjusted to the maximum allowed, while meeting all other constraints. The filter clock is 61.44MHz, scaled so the center tap is 2047 and the coefficients are rounded. Figure 20 shows the two carrier adjacent real mirror. Figure 21 shows the complex mirror mode used with an asymmetric carrier, using the prototype filter illustrated in Figure 19.

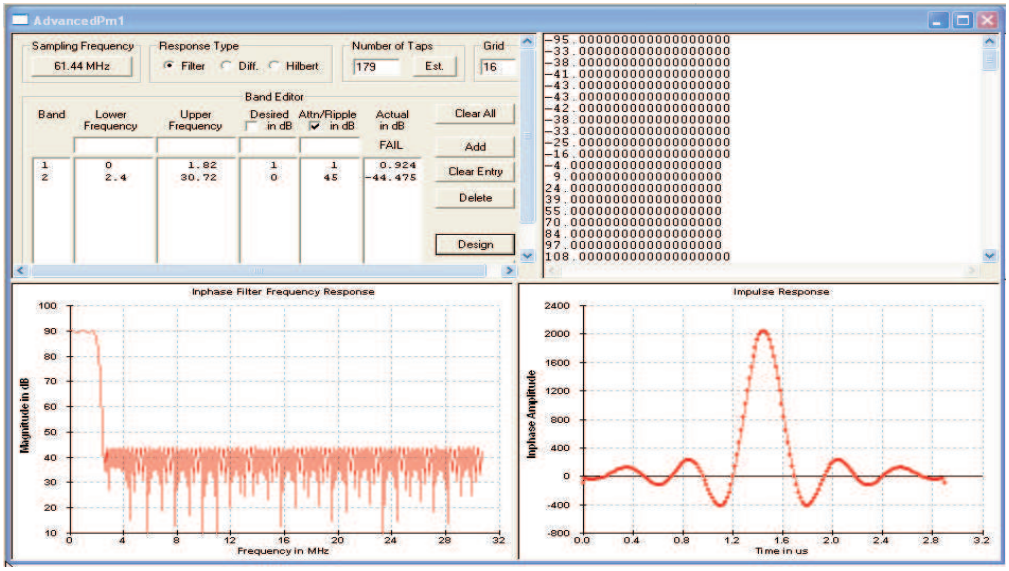


Figure 19. Real Cancellation Filter for Single-Carrier WCDMA at Zero-IF

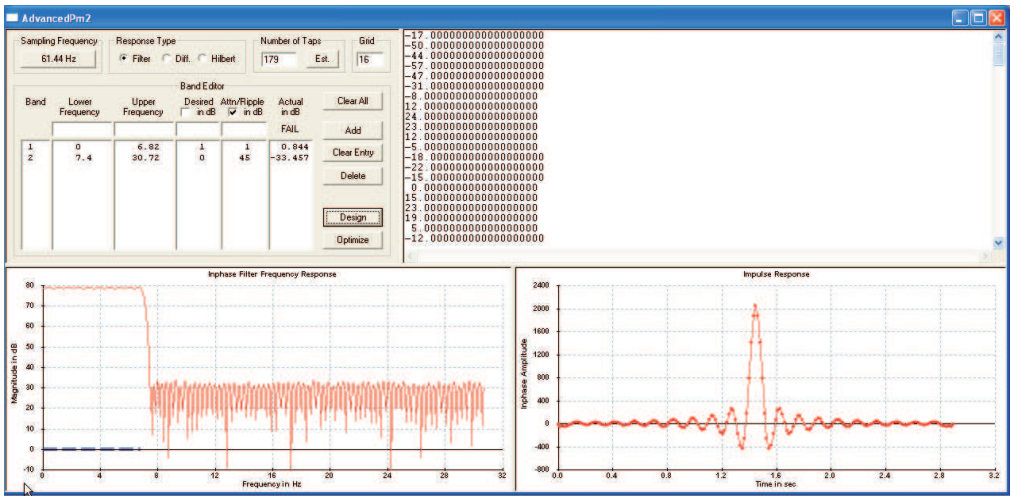


Figure 20. Real Cancellation Filter for Two-Carrier WCDMA at Zero-IF

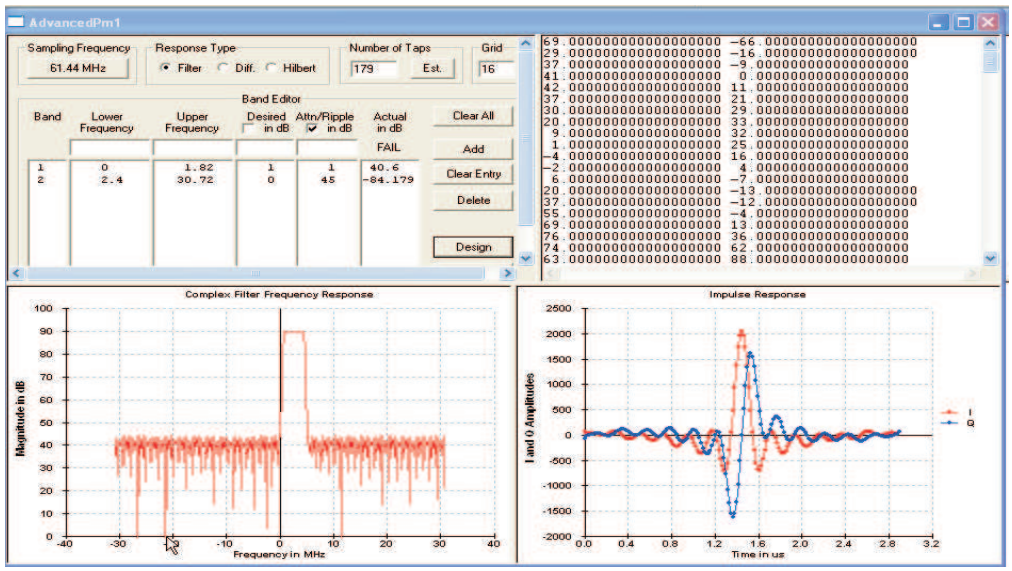


Figure 21. Complex Cancellation Filter for Single-Carrier WCDMA at 2.5MHz-IF

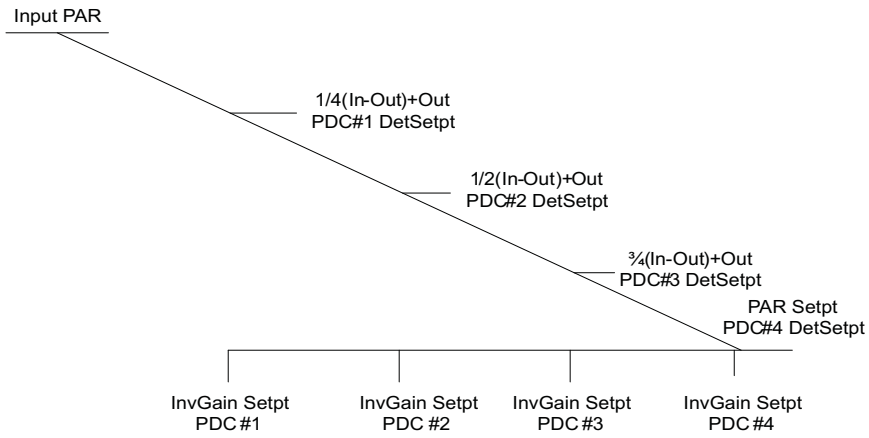
The CFR peak detection logic needs an oversampling ratio of >1.6 (typically 2x) from the input signal total bandwidth for optimal operation. For WCDMA, we have a bandwidth of 20MHz and a sampling rate of 61.44MHz thus a ~3:1 ratio. The peak detection and PAR reduction is divided into four stages each progressively reducing the PAR of the input signal to achieve the target output PAR. For WCDMA applications, the CEVM or PCDE specifications for a TM3-32 or TM5-30 are the limiting cases restricting the typical PAR output between 6.5 and 7dB. The four PDC stages have a threshold slope, and the PAR setpoint for the inverse gain value described in the equations below and Figure 22.

K[1-3] = (4-n)/4 × (InputPAR-PAR setpoint) + PAR setpoint,
K[4] = PAR setpoint.

An alternate setting used for CFR threshold calculation is:

K[1-2] = (3-n)/3 × (InputPAR-PAR setpoint) + PAR setpoint,
K[3,4] = PAR setpoint.

For an input TM1-64 signal of ~9.5dB PAR and target output PAR of 6.5dB, the alternate threshold calculation produces 8.5, 7.5, 6.5, and 6.5dB for the K[1.4] values.



NOTE: The CFR threshold adjustments and inverse gain add in-band noise which raises the EVM. The input RMS power level is important to calibrate the thresholds.

Figure 22. CFR Detection Setpoint and Inverse Gain Setting

Measuring the ACLR, CEVM, PCDE, and CCDF are important to determine the best tradeoff values; the TM1-64 example is illustrated in Figure 23 and Figure 24.

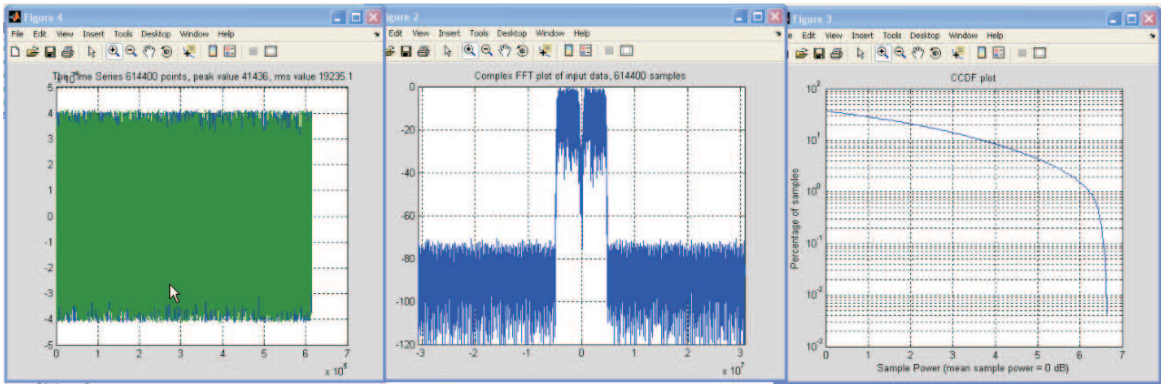


Figure 23. CFR TM1-64 Output (time series, FFT, and CCDF)

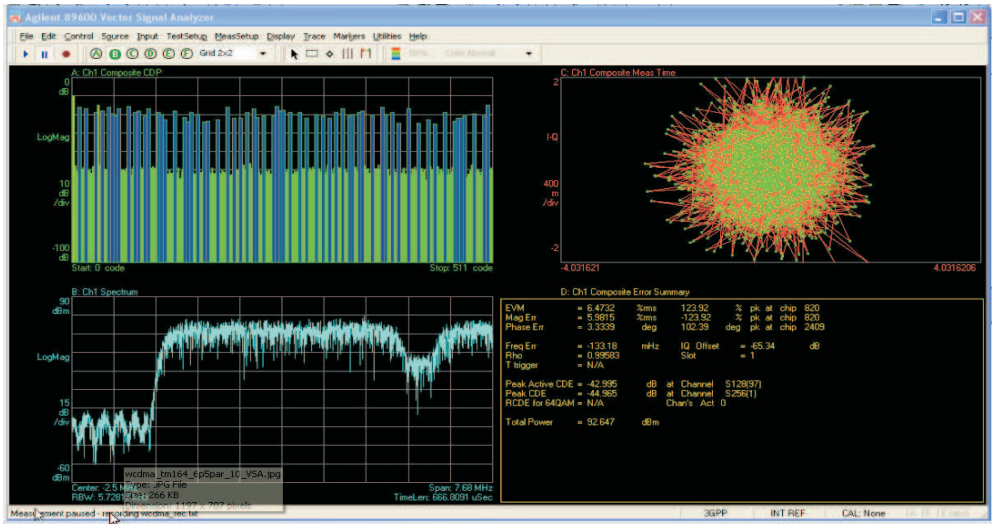


Figure 24. VSA output for CFR of TM1-64 carrier

For WCDMA applications, test models are defined to be used for compliance testing both for spectral and EVM quality. Since CFR uses EVM as its primary system tradeoff Table 3 shows the signal quality following CFR processing for a PAR of 6.5dB. The requirements are provided in Section 1.2 of this document.

Table 3. WCDMA Measurements for EVM and Peak EVM

	Carrier #0 Scramble Offset 0		Carrier #1 Scramble offset 1	
SLOT #	**EVM %**	**Peak EVM %**	**EVM %**	**Peak EVM %**
0	10.6	123	10.7	121
1	10.3	86	10.2	88
2	9.2	90	9.9	100
3	9.6	89	9.6	82
4	10	96	10.3	100
5	10	96	9.6	96
6	9.6	98	10.2	102
7	10	84	10.3	90
8	9.6	106	10	107
9	10	82	9.9	88
10	9.7	100	9.7	78
11	10.2	86	10.1	97
12	10	96	10.5	89
13	9.3	88	9.8	88
14	10	102	9.9	107

2.3 Digital Pre-Distortion

To maintain linearity and efficiency, one can apply linearization to the PA through several techniques such as feedback, feedforward, and pre-distortion. A pre-distortion system effectively performs a mathematical inversion of the PA using a Volterra model or similar mathematical approximation. The implementation of a DPD-PA cascade is illustrated in Figure 25.

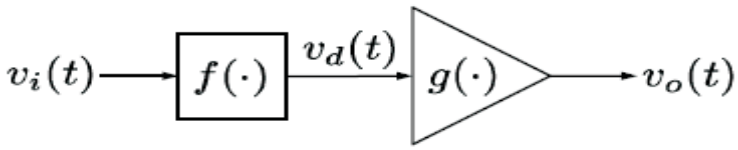


Figure 25. Cascaded DPD-PA Block Diagram

The DPD output is $v_d(t)$ and the output of the cascaded system is described by the following equation:

$$v_o(t) = g\left(f\left(|v_i(t)|^2\right)v_i(t)|^2\right)f\left(|v_i(t)|^2\right)v_i(t) \quad (2)$$

A pre-distorter applies distortion to the input signal in order to drive the PA harder. The PD-PA cascade attempts to combine two nonlinear systems into one linear result which allows the PA to operate closer to saturation. Beyond this point, no increase in power will suffice to linearize the PA. The PAR of the signal greatly restricts optimal performance of the DPD system. A WCDMA signal, for example, may have a PAR as high as 13dB. A PA transmitting such a signal must operate with significant back-off to prevent peaks from occurring beyond saturation. There are two common types of DPD implementations, the first is an analog implementation using a physical nonlinear device. The second and often the more popular choice, is a digital signal processor (DSP) hardware implementation where the DPD function is defined algorithmically through software [6, 7]. The PA operating near saturation can be quantified by the amount of gain compression (GC) as illustrated in Figure 26. The concept of PA operating near saturation is further illustrated in the time domain by Figure 27.

$$GC = 10 \log_{10}\left(\frac{V_2}{V_1}\right)$$

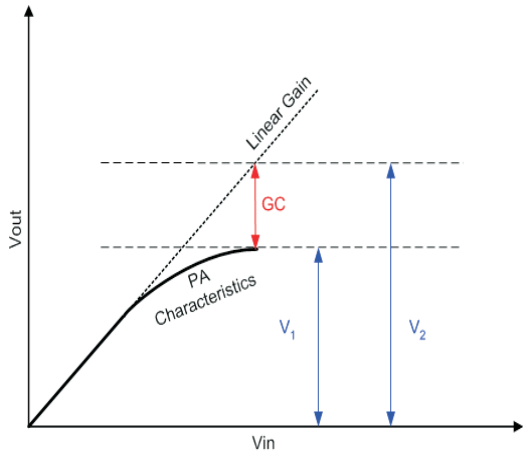


Figure 26. PA Operation with Gain Compression (voltages)

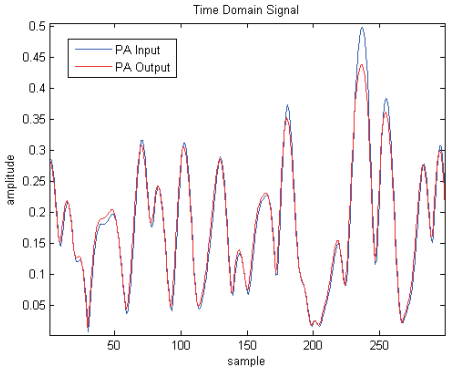


Figure 27. PA Operation with Gain Compression (time domain)

To correct for high-ordered nonlinearities the DPD system must operate at a sufficient oversample rate. In this application, the CFR rate was 61.44MHz, the signal is interpolated 2x to 122.88MHz which allows for greater than 5th order correction of a 20MHz signal. The concept of expansion bandwidth is illustrated in Figure 28.

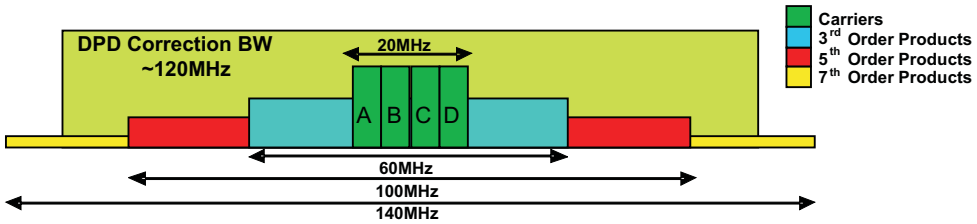


Figure 28. DPD Expansion/Correction Bandwidth (frequency domain)

2.4 Data-Converters and Clocking

The linearization system includes TI's digital-to-analog (DAC) and analog-to-digital converters (ADC) as illustrated in Figure 1. The system requirements on the DAC for a digital pre-distortion system are important, specifically the device must have enough dynamic range to support the difficult system requirements and, more importantly the device must support the extended pre-distortion bandwidth along with sufficient margin. The DAC5682Z meets both of these requirements by supporting 16-bit resolution and a 1-GSPS maximum data-rate. To utilize the inherent capabilities of the DAC and increase the system margins, the data-rate is increased by 1.5x up to 184.32MHz after DPD signal conditioning. This increase

in sample rate prevents the DAC interpolation filters from affecting the DPD signal. The DAC is used to interpolate the data 4x up to 737.28MHz and also apply an Fs/4 mix to the signal shifting the complex output up to an intermediate frequency (IF) of 184.32MHz. The complex data is then upconverted to RF by TI's TRF3703-33 IQ modulator as described in the next section. The "I" (or in-phase) portion of the DAC output signal under DPD operating conditions for PAR and back-off is illustrated in Figure 29.

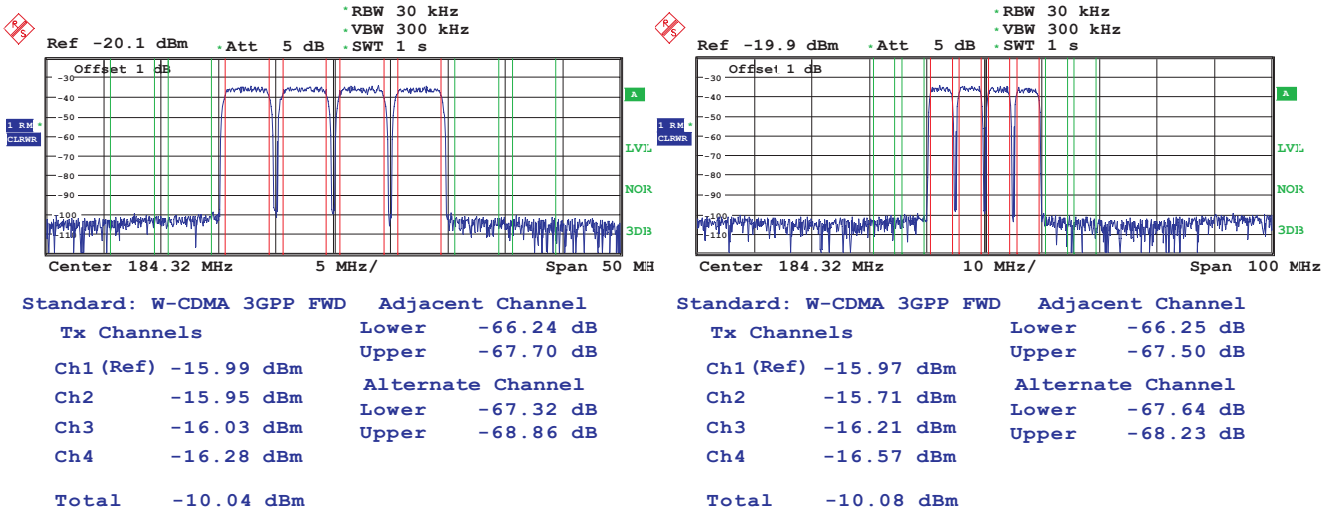


Figure 29. In-Phase Output of the DAC5682Z

The overall PA performance relies on the quality of the feedback path and specifically the feedback ADC which in this case is TI's ADS61B49 which delivers 14-bit resolution at up to 250MSPS. The ADC also features an internal input buffer which eases the design of IF filters used to condition the signal before the ADC; the buffer maintains constant input impedance across a wide frequency range a critical design requirement in DPD systems. The linearization algorithm cannot differentiate non-linearities between the transmitter path (TX) and DPD feedback path (FB) paths, as such the feedback path linearity should exceed that of the TX, specifically the ADC linearity is also critical to maintain optimal DPD performance; the intermodulation (IMD) performance of the ADC is shown in Figure 30. The ADC is operated at 245.76MHz to maximize the feedback signal bandwidth (Fs/2 or 122.88MHz) which should match the DPD rate for optimal performance, the signal is sampled at the same IF of the TX (184.32MHz) allowing the design to use a single LO for TX and FB.

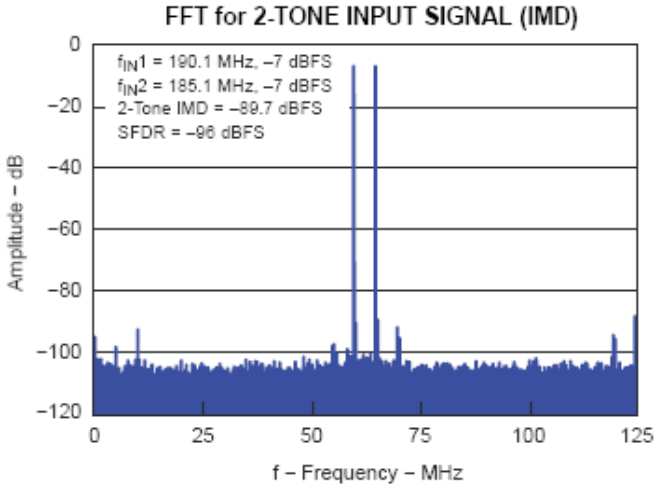


Figure 30. IMD Performance for ADS61B49 under system operating conditions

The actual performance of the ADC is dependant on the quality of the clock used to drive the device. For

this purpose, the system uses a high frequency VCXO of 737.28MHz in combination with a CDCM7005 phase-lock loop (PLL) / clock jitter cleaner product from TI. This device provides all of the clocks for the system including the digital devices, DAC5682Z and TRF3761 (RF PLL and voltage controlled oscillator). The measured jitter of the ADC clock is measured to be 236.3fs as illustrated in Figure 31. The theoretical SNR performance of the ADC at 184.32MHz IF is calculated from:
20×log (2π × jitter (s) × IF frequency (Hz)) to be ~71.3dB.

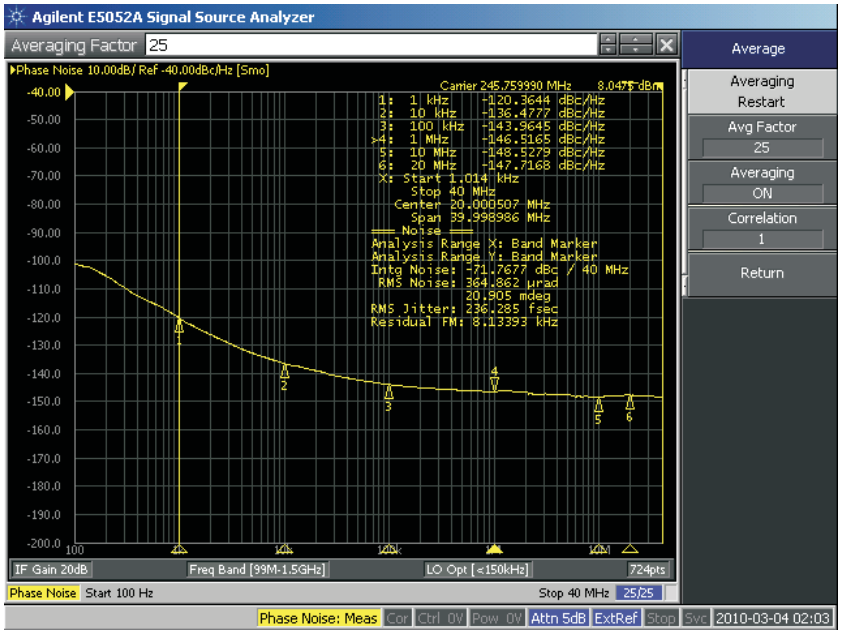


Figure 31. Measured Jitter of ADC clock at 245.76MHz

The detailed frequency plan and data-rate for the system is illustrated in Figure 32. From this figure, one can observe the data processing from the baseband DPD input up to RF and back through the feedback processing to baseband feedback.

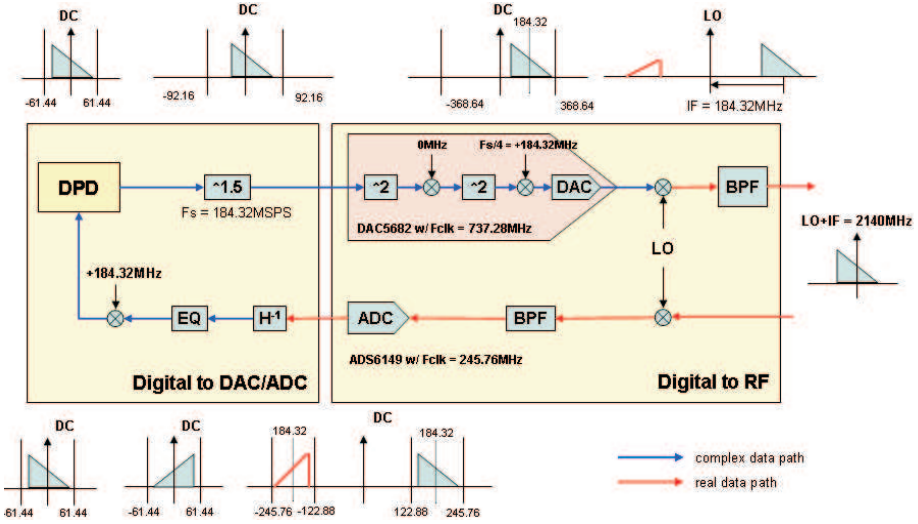


Figure 32. Signal Processing Flow from Digital to RF

2.5 RF Performance

The diagram illustrates the use of the TRF3703-33 to translate the signal from a complex IF of 184.32MHz up to 2.11–2.17GHz – the downlink allocation of the WCDMA frequency band. Also shown are the undesired presence of LO feedthrough and IQ imbalance; both artifacts typically produced in IQ modulators. These can be reduced using digital techniques or using a simple bandpass filter. The removal of these undesired products is also important to achieve maximum DPD performance. Figure 33 illustrates the performance of the TX signal chain including the DAC5682Z and the TRF3703-33 under typical DPD operating conditions for PAR and signal backoff.

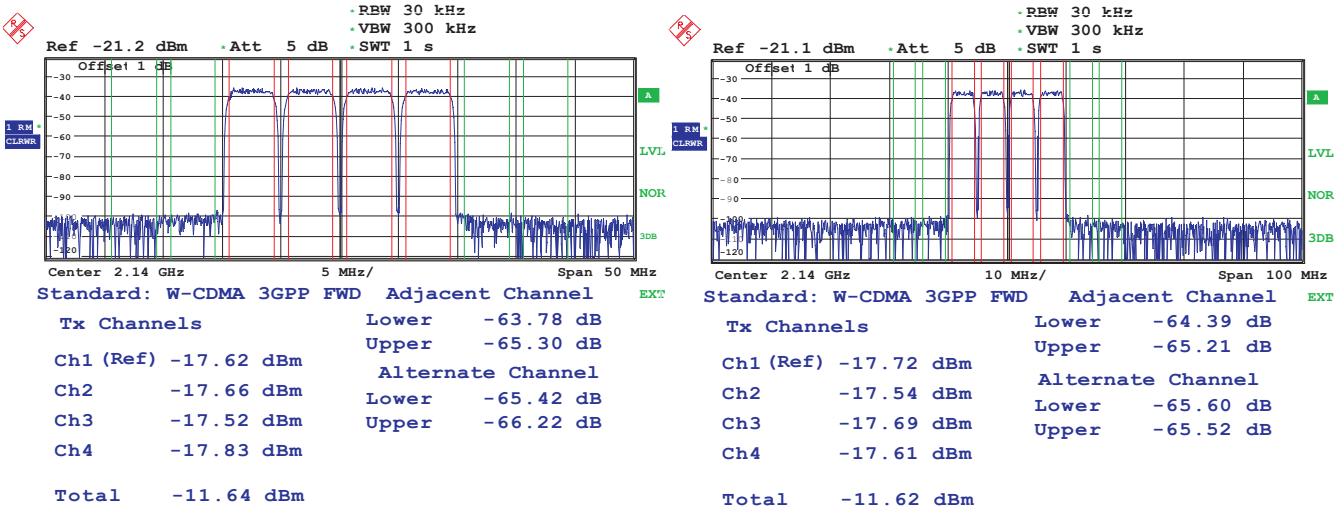


Figure 33. Measured Performance of the TRF3703-33 Output at 2.14GHz

The final analog impairment for the system is caused by the quality of the local oscillator (LO), in this system the TRF3761-G (TI's highly integrated VCO/PLL) is used. The measured phase noise of the device is shown in Figure 34.

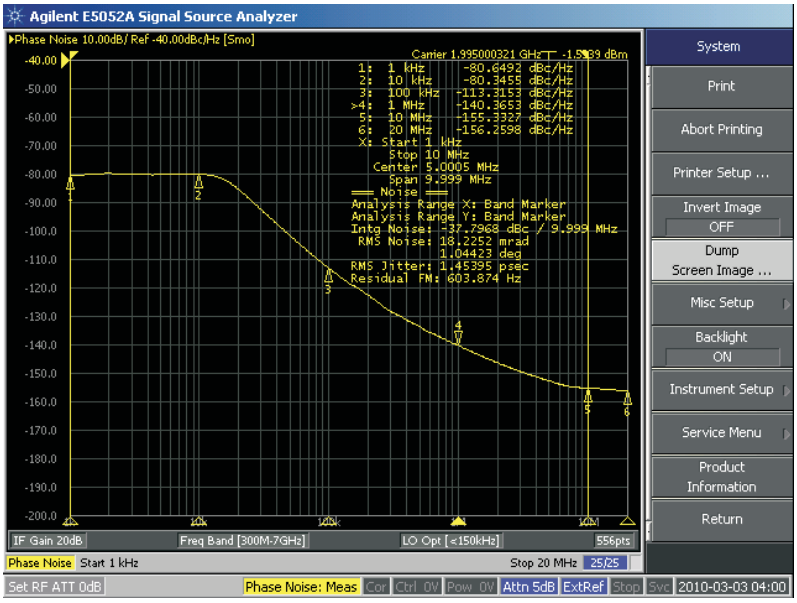


Figure 34. Measured Phase Noise of the TRF3761-G at 1.995GHz

3 System Linearization Performance

3.1 WCDMA '1111' Test Case

While the most popular WCDMA band occupies from 2110–2170MHz for downlink (BTS to mobile) and 1920–1990MHz for uplink (mobile to BTS), most transmitters only occupy 20MHz of instantaneous signal bandwidth. In WCDMA, 20MHz translates to a four carrier deployment scenario – often called the '1111' test case. For test purposes, the TM1-64DPCH signals were used for DPD performance validation. To validate system performance across the complete allocation bandwidth, the system was tested at the center, upper and lower bounds of the spectrum translating to carriers centered at 2.12, 2.14 and 2.16GHz. Figure 35, Figure 36 and Figure 37 illustrate a summary of spectral performance before an after DPD with respect to input power levels.

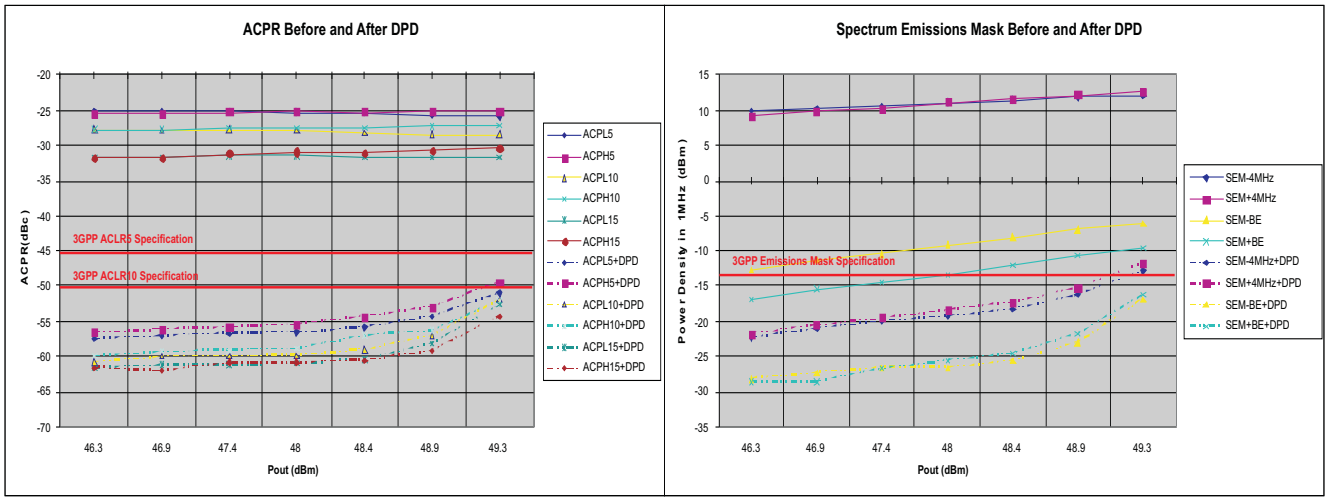


Figure 35. WCDMA '1111' Performance at 2.12GHz

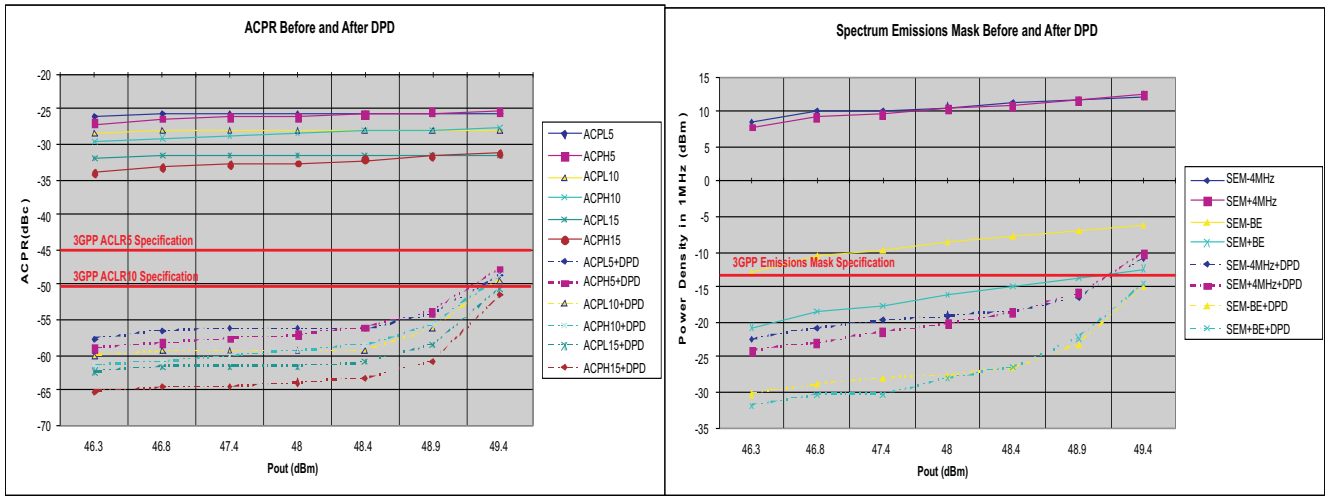


Figure 36. WCDMA '1111' Performance at 2.14GHz

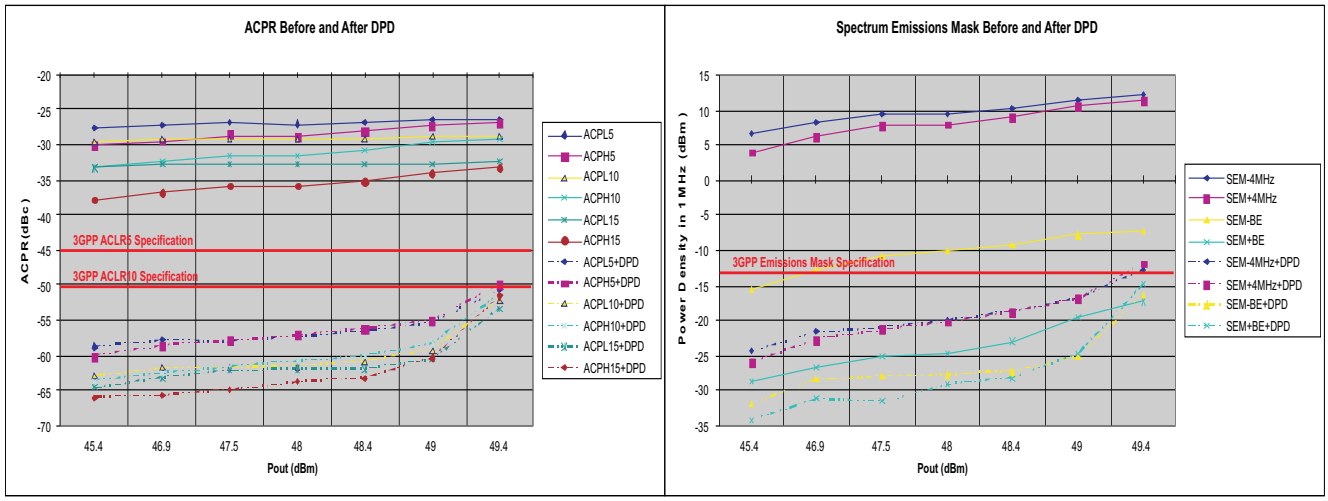


Figure 37. WCDMA '1111' Performance at 2.16GHz

The test equipment screen captures for the 2.14GHz '1111' test case at 48.9dBm are illustrated in Figure 38.

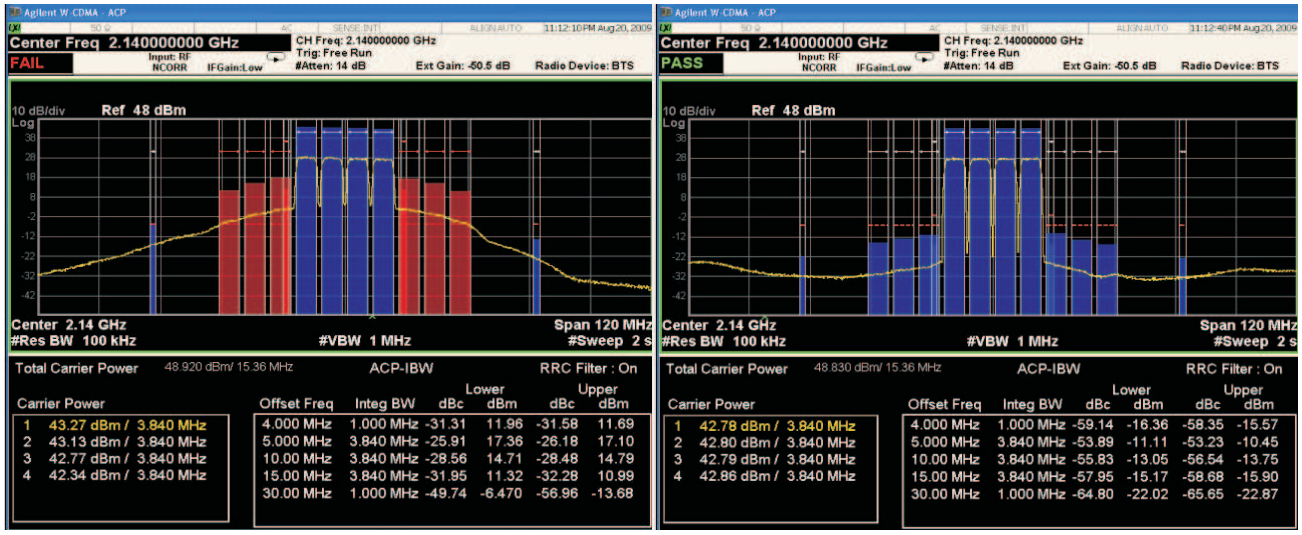


Figure 38. WCDMA '1111' Spectral Performance at 2.14GHz and 48.9dBm

3.2 WCDMA '1001' Test Case

The previous test case highlights a wideband deployment scenario however the most difficult DPD test case is often considered to be the two carriers with 15MHz center-to-center spacing – this is the '1001' test case.

This scenario is used to highlight DPD performance degradation due to unmitigated memory effects present in the PA that can be attributed to the video bandwidth of the transistors and/or PA design often due to input and output matching issues. The results are summarized in Figure 39, Figure 40, and Figure 41.

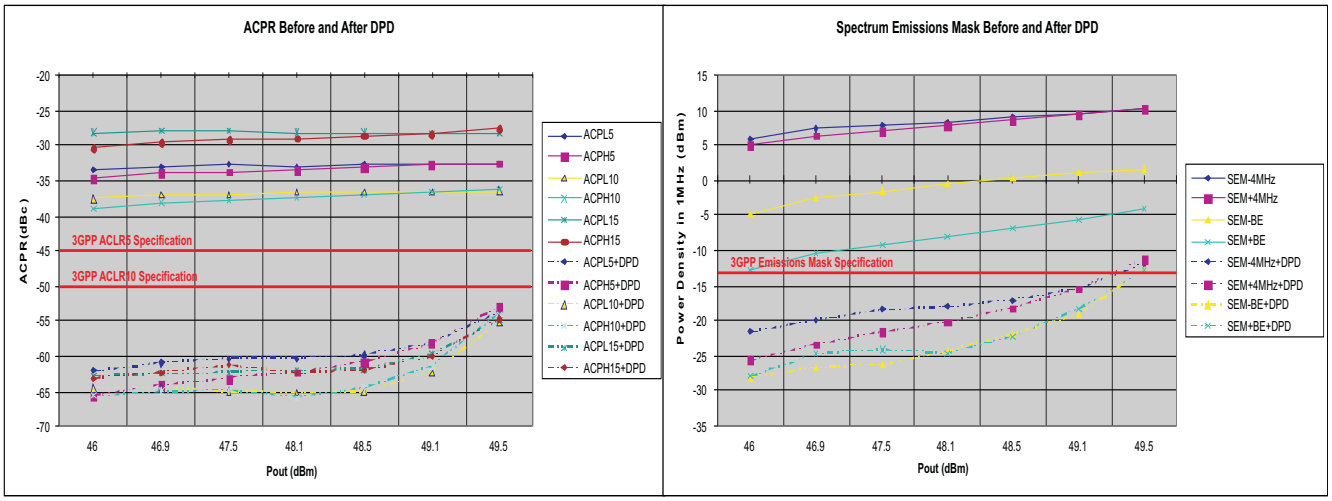


Figure 39. WCDMA '1001' Performance at 2.12GHz

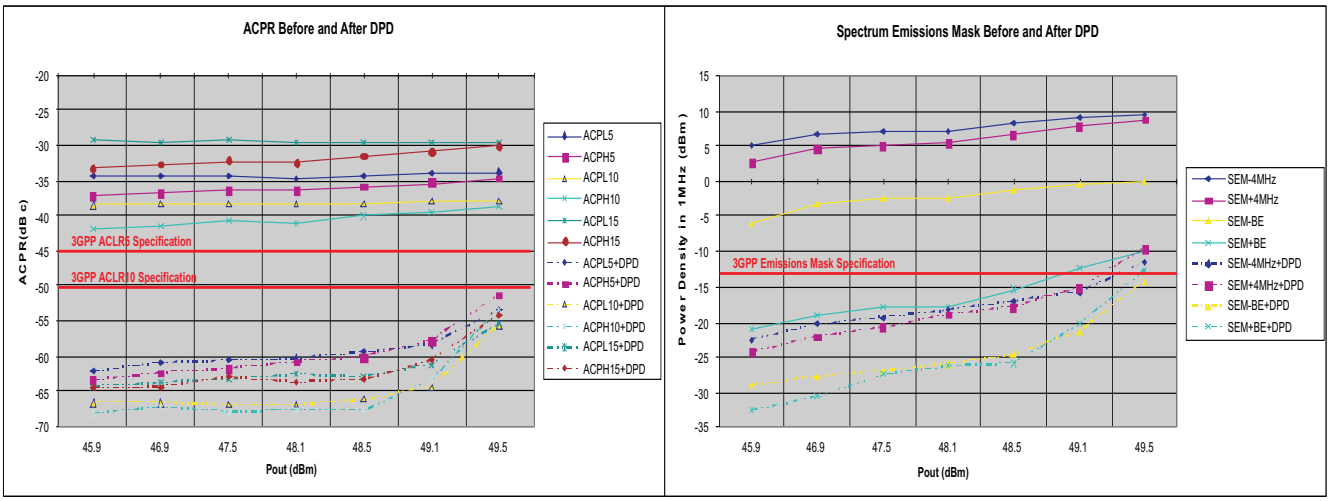


Figure 40. WCDMA '1001' Performance at 2.14GHz

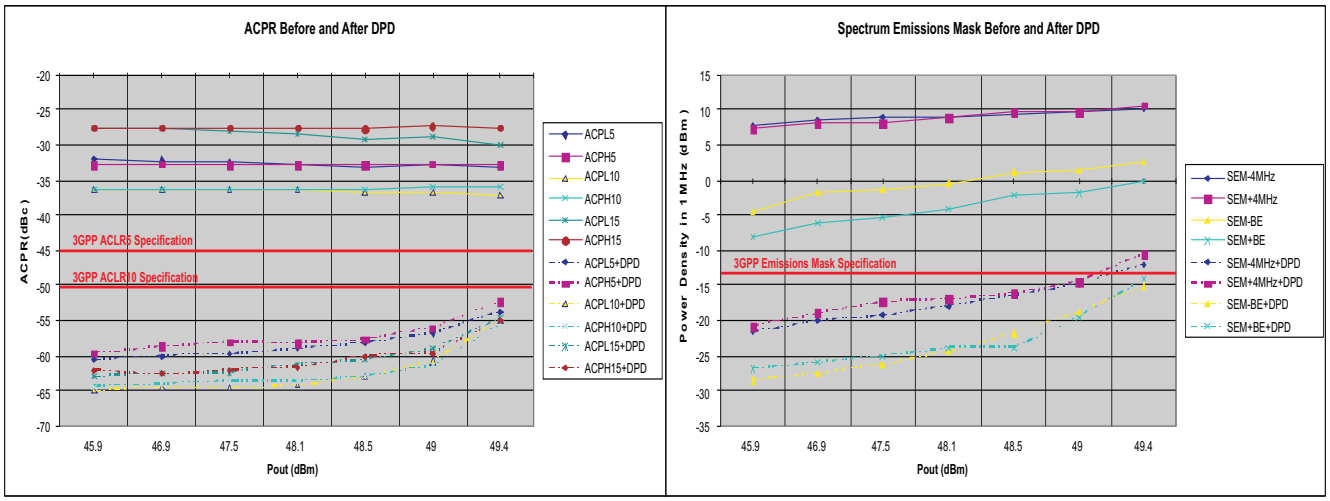


Figure 41. WCDMA '1001' Performance at 2.16GHz

The test equipment screen captures for the 2.14GHz '1001' test case at 48.9dBm are also illustrated in Figure 42.

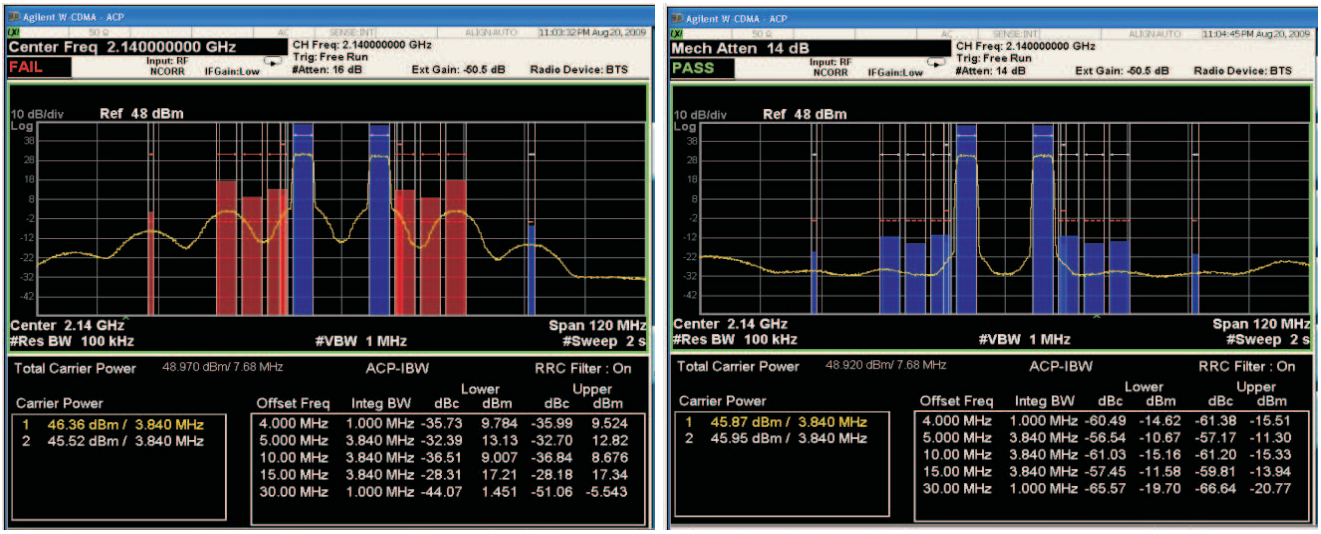


Figure 42. WCDMA '1001' Spectral Performance at 2.14GHz and 48.9dBm

4 Conclusions

In the past, several different techniques have been proposed to handle the problem of PA linearization. Previous implementations and techniques have been shown to achieve significant efficiency improvements. The most effective systems utilized either analog feed forward, analog feedback, or digital pre-distortion with wideband feedback. Although each successive method has achieved noticeable performance at a continually decreasing cost, the trend for cost reduction remains. This trend along with the ongoing desire to push the digital domain closer to analog favors digital pre-distortion. Performance and cost of DPD implementations is driven by the performance requirements, upgradeability and system margins. These tradeoffs are even more prevalent with the increasing bandwidth of 3.5G and 4G systems which operate under orthogonal frequency-domain modulation (OFDM) schemes. This further illustrates the limitations of DPD algorithms that require wideband feedback to achieve efficiency improvements

In this work, a system was designed using state-of-the-art high-speed products from Texas Instruments capable of implementing pre-distortion on both wideband and widely spaced carrier configurations. The system closely represents a typical base station implementation for DPD including memory effects. The implementation confirmed the combined benefits of DPD and CFR with greater signal bandwidths. The system performance was indicated through increased output power and efficiency such that at 48.9dBm (6.5dB backoff) the PA achieved approximately 40% while meeting regulatory requirements. The closed-loop hardware results for the adaptation of a memory polynomial have shown performance improvements on an amplifier with memory effects suggesting that this technique can be employed as a high performance solution to meet ACP requirements when compared to typical system implementations.

5 References

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