Estimating available application power for Power-over-Ethernet applications*

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Introduction

Many existing Ethernet devices are being converted from wall-adapter power sources to utilize the newly released IEEE 802.3af Power-over-Ethernet (PoE) standard. Power-system efficiency formerly was not much of an issue with a wall adapter—but PoE changes that. Applications whose functional circuits begin to draw power in the 10-W range need close control of their power usage. This article helps the designer determine how much power is available when an application operates from a PoE source.

First we will determine the net power available once the functions required by the 802.3af standard are performed. Then a method of modeling the usual DC/DC converters to compute the power available for the applications circuits will be presented, with two example topologies for comparison. The modeling process allows the designer to identify topology and technology issues before the first circuit is designed. In this discussion, application circuits are considered to be everything in the powered device (PD) except the PoE front end and DC/DC converters.

PoE front-end losses

Figure 1 is a basic block diagram that shows the interconnection of the power-source equipment (PSE) through the

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DC/DC converter and application circuits. Calculations yielding the results in Table 1 assume that the PSE output (44 V minimum) is connected through 20 Ω of cable into a PD. The PD front end has a transformer (1 Ω total, with

Table 1. Analysis of PoE distribution and front-end losses

PARAMETERS	MIN	TYP	MAX
PSE output (V)	44	—	57
Distribution resistance (Ω)	—	—	20
Source power (W)	—	—	15.4
PD average current (A)	—	—	0.35
Constants			
Diode forward drop (V)	—	0.8	—
Transformer resistance (Ω)	—	—	1
PD-controller switch resistance (Ω)	—	1	—
PD-controller bias power (A)	—	0.0012	—

LOSS SOURCE	LOSS (W)	AVAILABLE POWER (W)
		15.40**
Distribution	2.45	12.95
Input diode	0.56	12.39
Input transformer	0.06	12.33
PD-controller switch	0.12	12.21
PD-controller bias	0.04	12.16

**Total PoE power available

Figure 1. Basic PoE block diagram
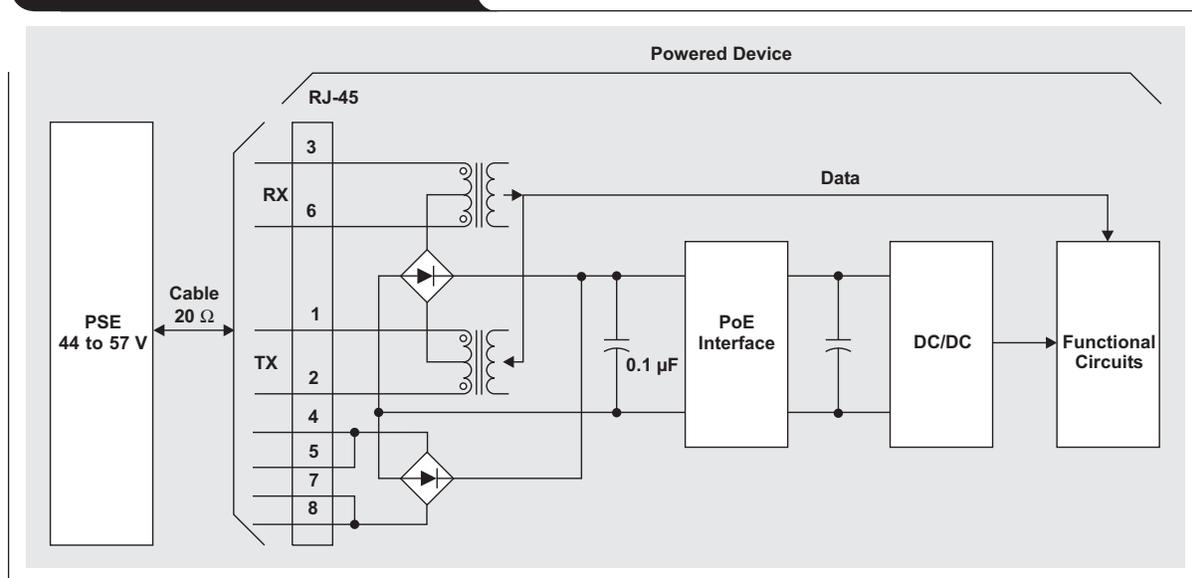
0.5 Ω each side to the center tap), a full-wave bridge, and a hot-swap controller (or PD controller) with a 1-Ω switch (FET) in series.

There is a maximum of 12.16 W available for PD functional circuits. The 802.3af standard defines the 2.45-W worst-case cable loss, and the input diode bridge dominates the additional front-end losses of 0.78 W.

Modeling of power-conversion stage

Simple modeling techniques allow the designer to understand the effects of different topology and technology choices before an actual design is done. Simple efficiency assumptions give quick, qualitative results to allow topology comparison and optimization. The end results will be only as good as the assumptions, so the designer should always allow some margin by specifying the available power below these results.

First, let's look at the baseline of a single-stage conversion to one output voltage. A single 3.3-V output converter at 90% efficiency will yield an available output power of $0.9 \times 12.16 = 10.9$ W. Although the 90% efficiency may be viewed as optimistic, it does provide a baseline for comparison to other topologies.

Next we will estimate the output power available from a more complex power supply. A simple modeling technique is used to study how the topology and technology for each regulator affect output power. Output voltages of +5 V at 0.2 A, 3.3 V at 2 A, 2.5 V at 0.25 A, and 1.8 V at 0.25 A are assumed. These add up to a reasonable 9.6 W.

Figure 2 shows two possible supply architectures and technology choices. Topology 1 represents adaptation of an

existing appliance design that had a 12-V wall adapter, which was replaced with a 48-V to 12-V front end. Topology 2 attempts to maximize the available power.

To evaluate the model, start at the right-most regulators, calculating their loss and total input power, and then use these results to evaluate the next regulator to the left. For simplification, assume 90% efficiency for a switcher and no bias current for linear regulators. These calculations are summarized for the regulator types as follows.

Definitions

I_{OUT} = application load current
$P_{IN\_Next\_Stage}$ = power drawn by a downstream converter or linear regulator

Linear regulator stage

$$P_{OUT} = \left(V_{OUT} \times I_{OUT}\right) + P_{IN\_Next\_Stage}$$

$$P_{IN} = V_{IN} \times \frac{P_{OUT}}{V_{OUT}}$$

$$P_{Loss} = P_{IN} - P_{OUT}$$

Switching regulator stage

$$P_{OUT} = \left(V_{OUT} \times I_{OUT}\right) + P_{IN\_Next\_Stage}$$

$$P_{IN} = \frac{P_{OUT}}{Efficiency}$$

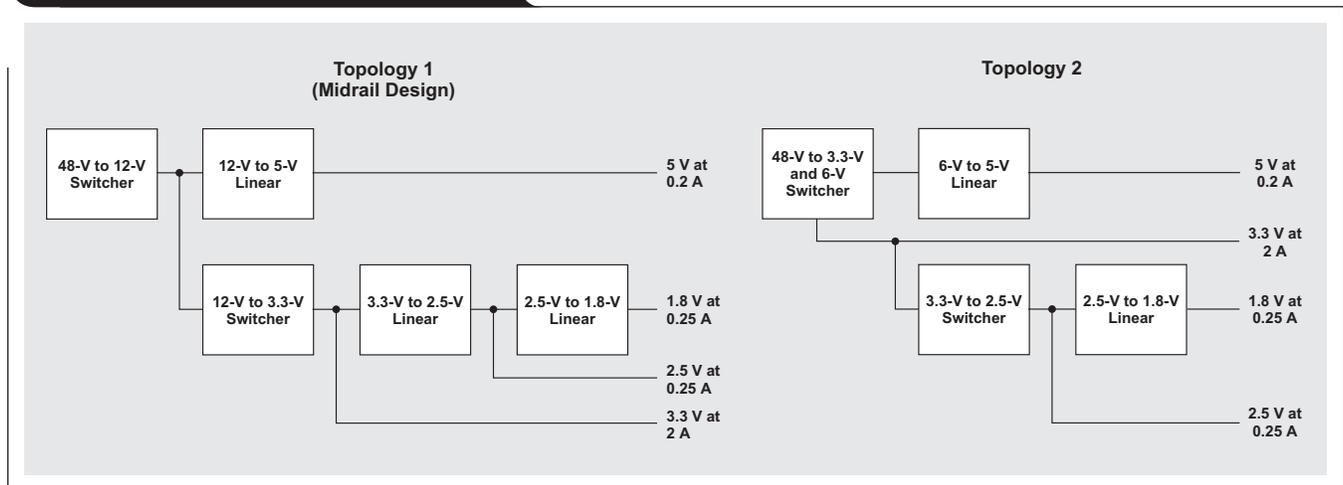$$P_{Loss} = P_{IN} - P_{OUT}$$

Figure 2. Alternative supply topologies

Table 2. Topology 1 model

MODEL COMPONENTS	OUTPUT VOLTAGE (V)	REGULATOR TYPE	INPUT VOLTAGE (V)	REGULATOR EFFICIENCY (%)	APPLICATION CURRENT (A)	ADDITIONAL OUTPUT LOAD (W)	COMPUTED INPUT POWER (W)	STAGE LOSS (W)
Chain 1	1.8	Linear	2.5	—	0.25	0.00	0.63	0.18
	2.5	Linear	3.3	90	0.25	0.63	1.65	0.40
	3.3	Switcher	12	90	**1.83**	1.65	**8.54**	**0.85**
Chain 2	5	Linear	12	—	0.2	0.00	2.40	1.40
First-stage input power	—	Switcher	48	90	0	**10.94**	**12.16**	**1.22**
Total loss								4.05
Apparent efficiency = **67%** Available output power = **8.11 W**								

Table 3. Topology 2 model

MODEL COMPONENTS	OUTPUT VOLTAGE (V)	REGULATOR TYPE	INPUT VOLTAGE (V)	REGULATOR EFFICIENCY (%)	APPLICATION CURRENT (A)	ADDITIONAL OUTPUT LOAD (W)	COMPUTED INPUT POWER (W)	STAGE LOSS (W)
Chain 1	1.8	Linear	2.5	—	0.25	0.00	0.63	0.18
	2.5	Switcher	3.3	90	0.25	0.63	1.39	0.14
	3.3	—	—	100	2.532	1.39	9.74	0.00
Chain 2	5	Linear	6	—	0.2	0.00	1.20	0.20
First-stage input power	—	Switcher	48	90	0	10.94	12.16	1.22
Total loss								1.73
Apparent efficiency = 86% Available output power = 10.43 W								

Using data in Table 2, let's go through the calculations for the Topology 1 model shown in Figure 2. Looking at the lower branch, Chain 1, data in Table 2, start with the 1.8-V regulator's input power and loss; notice that there is no next-stage power. The 2.5-V regulator is computed similarly, with the output power now comprised of the 0.25 A to the load multiplied by 2.5 V, plus the 1.8-V regulator's input power previously computed. The 3.3-V switching regulator's input power is the total output power divided by the efficiency of this stage (0.9%). The power loss of the 3.3-V regulator is still the input power minus the output power. The upper branch is computed in a like manner with the Chain 2 data. The 48-V to 12-V regulator's parameters are calculated like those of the 3.3-V regulator, where the total output power is the sum of the upper- and lower-branch input powers. To get a handle on the topology's performance, the individual losses are summed and the apparent efficiency is computed as

$$\text{Efficiency} = 1 - \frac{\text{Total\_Losses}}{\text{Input\_Power}}.$$

The available output power in Table 2 is the input power minus all the computed individual losses.

Topology 1's input power exceeds the amount available. To provide a more interesting result, the 3.3-V load shown was adjusted until the input power was 12.16 W. Bold values in Table 2 reflect the reduction of the 3.3-V supply load from 2 A to 1.83 A.

Topology 2 is modeled with data in Table 3 much as Topology 1, with a small wrinkle. A dummy 3.3-V regulator is modeled with an efficiency of 1 for proper totaling of the power and loss.

The efficiency of 90% used for the 48-V to 3.3-V converter in Topology 2 is a fairly optimistic number for a practical, synchronous output-rectifier circuit.

Conclusion

After the 802.3af standard functions are considered, 12.16 W is the maximum power available for other electronics, including regulator losses.

The effects of topology and technology choices for PoE applications are quite startling. Topology 1 makes only 8.11 W available to the application's circuits, while Topology 2 makes 10.43 W available. This is an increase of 28%. The baseline single-output converter provided 10.9 W, so all the processing represented by the additional three outputs in Topology 2 cost only 0.47 W! Using a diode output converter (85% efficiency) instead of a synchronous rectifier for the 3.3-V converter drops the available power by 0.61 W.

This modeling technique allows the designer to calculate available output power rapidly based on topology and technology choices. The designer can use this information to trade off available power, complexity, and cost.

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