High-Performance Analog Products

Analog Applications Journal

First Quarter, 2007

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

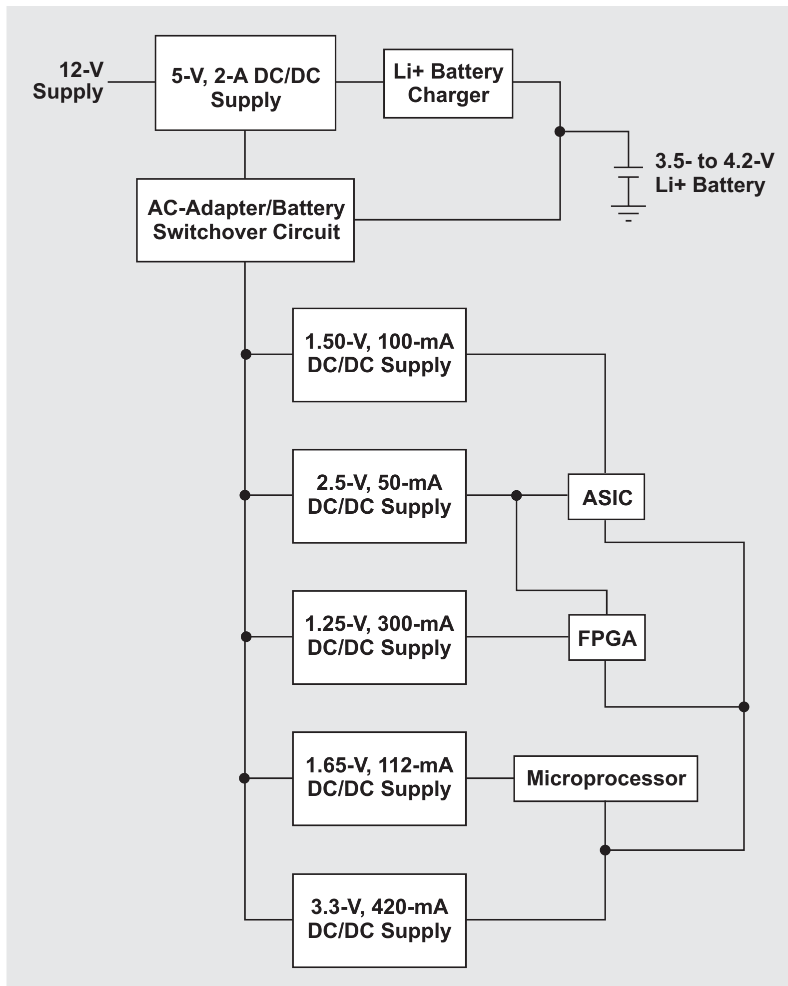
Selecting the correct IC for power-supply applications

By William Hadden (Email: willhadden@ti.com)
Applications Engineer, High Performance Analog, Low Power dc/dc

Selecting the proper integrated circuit (IC) for a power-supply application may seem like an easy task. However, as newer consumer electronics come out that require multiple voltage rails, the task becomes more complex. To select the correct IC(s) for the job, many factors such as cost, solution size, power source, duty cycle, and required output power must be weighed. These factors must be ranked by importance and the power supplies selected accordingly. In this article, we will determine the best solution for the application shown in Figure 1.

Our example application is portable, requires the lowest possible battery consumption and a small form factor, and operates from a single-cell Li-ion battery that is charged whenever the 12-V supply is available. We want to keep the cost to a minimum; but this can be sacrificed for space considerations, which are the most important requirements, followed by the highest efficiency possible to extend battery life.

Figure 1. Power-supply application



Selecting the best topology

First, let's examine the power requirements of each rail to determine what kind of dc/dc converter should be used (i.e., inductive switcher, linear regulator, or charge pump).

Inductive switchers are usually the best choice for highest efficiency. The inductive switcher circuits require a switching element, rectifier, inductor, and input and output capacitors. For many applications, the solution size can be reduced by choosing a device where the IC switching element and rectifier are internal. These circuits have typical efficiencies ranging from 80 to 96%, depending on the load. Switching converters usually require more space due to the size of the inductor and are generally more expensive. The switching converter also causes electromagnetic interference (EMI) radiation from the inductor and noise on the output due to the switching.

Low-dropout linear regulators (LDOs) step down dc voltages by dropping the input voltage across a pass element. The benefit of this topology is that it requires only three parts (pass element and input/output capacitors). LDOs are usually a cheaper solution and are much less noisy than inductive switchers. The device input current is equal to the load current, so the efficiency of the solution is equal to the output-to-input voltage ratio. The drawback of this solution is the low efficiency for high input-to-output voltage ratios. All of the power is dissipated by the pass element, which means that an LDO is not an ideal solution for high-current applications where the input-to-output difference is large. These high-power applications require heat sinking, which increases the solution size.

Charge pumps step up/down or invert dc voltages using “flying” capacitors as storage elements and use internal switches to connect the capacitors in such a way as to perform the desired dc/dc conversion. Charge pumps are generally cheaper than inductive switchers and do not emit EMI, but the output ripple is usually greater than that of inductive switchers. Charge pumps are limited in their output power, and the transient response is limited to the rate at which the flying capacitors can charge. Additionally, efficiency is usually very low in applications where the input voltage is near the output voltage.

To further reduce the solution size, many multi-output ICs are available. These ICs usually contain internal MOS field-effect transistors (MOSFETs) and require a minimum of external components. These ICs alone may be more expensive, but the savings gained by the reduction of external parts that must be placed during production will, in many cases, offset the higher cost.

What topology should we use?

Due to the space constraints of this application, LDOs would be our best choice. However, this is not always possible due to power dissipation and efficiency constraints. Beginning with the 5-V, 2-A rail, it is clear that we should choose a switching converter. The power dissipated by an LDO, in this case 14 W, is excessive. For this rail, an inductive step-down converter is the best choice.

Next we move on to the battery charger. This battery is charged from the 5-V rail. Our application is for a single-cell Li-ion battery that has a charging voltage of 4.2 V. With the space constraints of our application, a linear charger is a good choice. The charging efficiency is not as much of a concern because the only time this device will operate is when the 12-V power adapter is available. However, when selecting the peak charge current of a battery deeply discharged to 3 V, we must take care to limit the thermal dissipation of the device.

- For the 1.50-V rail, either a switching step-down converter or an LDO would be acceptable. With the latter, our efficiency would be in the 25% range and would require an input current of 100 mA. If we substitute a switching step-down converter, we could get efficiencies higher than 90%, which requires an input current of 30 mA. There are many very small switching-converter solutions that can supply the required output power, so the size increase over an LDO circuit is not appreciable. To maximize battery life, the step-down converter is a better choice.
- For our 2.5-V rail, again, either topology is acceptable. Due to the low current requirements and lower input/output differential, an LDO is the best choice for the smallest size.
- For our 1.25-V rail, a switching converter is the best choice. With the high (300-mA) load requirement and the large input/output differential, an LDO would dissipate too much power and is too inefficient.
- For the 1.65-V rail, again, either topology is acceptable. Using the same logic as for the 1.50-V case, we could choose a switching converter; but other factors discussed later require that this be an LDO.
- For the final 3.3-V rail, a switching converter is the best choice due to the large output current required.

Selecting the best IC(s) for the job

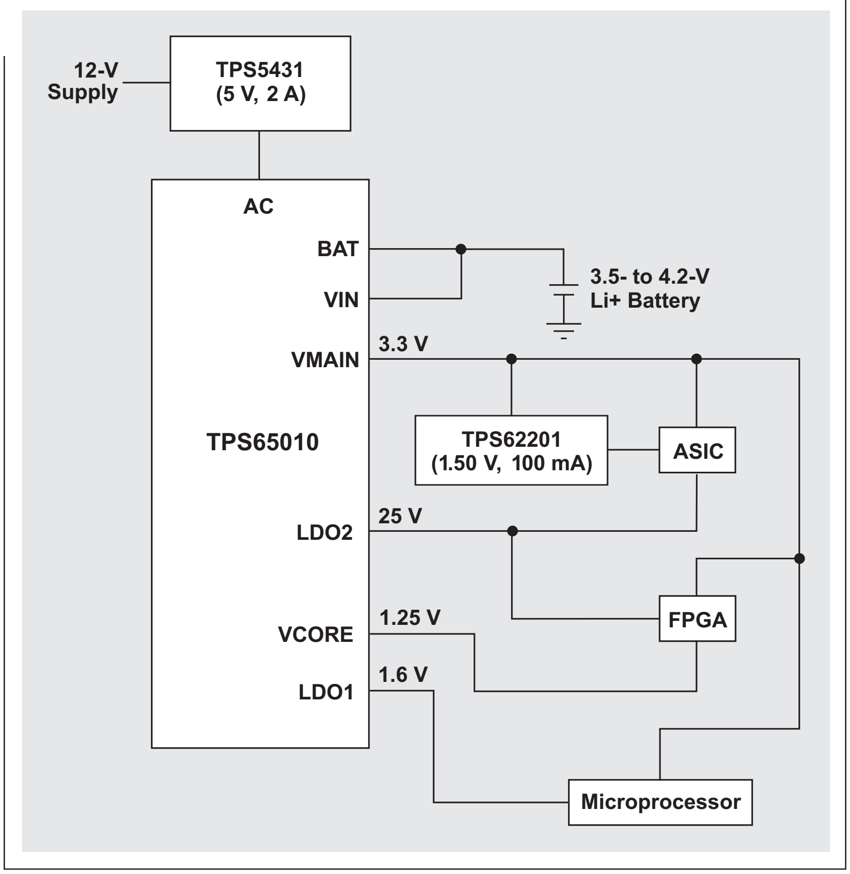
Taking into consideration our size and cost constraints, the chosen ICs should be as highly integrated as possible. All of the selected ICs contain internal MOSFETs. This saves on solution size as well as on production costs. In addition to a reduced bill of material, the reduced component count reduces the cost to assemble each board for further cost savings. There are also multi-output ICs available that decrease our solution size even further.

If we start again with the 5-V rail, the best solution for this is the TPS5431. Its wide input range (5.5 to 23 V) will accept our 12-V, ±10% input. The TPS5431 also provides up to 3 A with an adjustable output voltage down to 1.2 V. The switching MOSFET and the compensation components are integrated, and the 95% efficiency meets our battery-power demands. The device comes in the SO-8 package for a very small solution size.

Proceeding to the battery charger, we have several choices. The bq24010, a small battery charger IC in the 3 × 3-mm QFN package, is a good choice. Its solution size is very small and requires only three external components, but there is a better solution for our application. The TPS65010 is a power- and battery-management IC for Li-ion-powered systems. This device is an excellent fit for our application, as it integrates two switching converters (VMAIN and VCORE), two LDOs (LDO1 and LDO2), and a single-cell Li-ion battery charger. In addition to these rails, the IC also eliminates the need for a switchover circuit when the 12-V power adapter is connected. In our application, VMAIN powers the 3.3-V rail, VCORE powers the 1.25-V rail, LDO1 powers the 1.65-V rail, and LDO2 powers the 2.5-V rail. Using the TPS65010 drastically reduces our solution size as well as the external component count.

The remaining 1.50-V rail can be powered from a step-down switcher such as the TPS62201. This device comes in a five-lead SOT-23 package and requires only three external components (input/output capacitors, inductor, and two feedback resistors). This translates to a very small solution size. To increase efficiency, the input of this device should be connected to the 3.3-V MAIN output of the TPS65010.

Figure 2. Power-supply solution



The final solution

The final solution, based on the preceding discussion, is shown in Figure 2.

No I²C interface available?

If our application did not have an I²C interface available, we would not be able to use the TPS65010. In this situation, the TPS75003 would be useful. It contains two 3-A switching dc/dc step-down converters as well as one 300-mA LDO. This adjustable output device would integrate the three highest current rails. The 1.25- and 3.3-V rails would be supplied by the switching converters. The LDO would supply the 1.65-V rail because of the lower current requirement. The remaining 2.5-V rail is easily supplied by a small LDO circuit. The TPS71525, which comes in an SC-70 package and is stable with ceramic output capacitors, provides a very small solution size.

A larger but less expensive solution is the TPS76925 to power the 1.65-V rail. The TPS76925 control circuitry requires a minimum equivalent series resistance on the output for stability, so this may interfere with the size constraints.

Calculating the system efficiency difference

For this discussion, we have assumed that all of the voltage rails are on 100% of the time, which is rarely the case. Sometimes, where an inductive switcher would typically be used, an LDO may be an acceptable choice to minimize solution size. We can determine which to use by calculating the efficiency difference between each topology.

Using the percentage of time that an output is enabled (the duty cycle), we can determine the effect of each rail on the total solution efficiency. First, the effective total output power is calculated by summing up the effective power for each rail:

$$P_{OUTEFFTOT} = \sum_{i=1}^{n} D_i \times P_i,$$

where P_i is the output power from one output rail and D_i is the duty cycle for the same rail. Next, we calculate the power lost by each rail:

$$P_{LOSS} = D \times P_{RAIL}\left(\frac{1}{\eta_{RAIL}} - 1\right)$$

We then sum up the power loss for all of the rails to get the total power loss:

$$P_{LOSSTOTAL} = \sum_{i=1}^{n} D_i \times P_i \left(\frac{1}{\eta_i} - 1 \right),$$

where η_i is the efficiency of the individual output rail. We then calculate the effect of each rail on the overall system efficiency:

$$\eta_{SYSRAIL} = \frac{D \times P_{RAIL}}{P_{LOSSTOTAL} + P_{OUTEFFTOT}}$$

By summing all of the rail system efficiencies or by using the following equation, we can determine the total system efficiency:

$$\eta_{SYS} = \frac{P_{OUTEFFTOT}}{\sum_{i=1}^{n} \frac{D_i \times P_i}{\eta_i}}$$

For example, if the 3.3-V, 420-mA rail we previously decided should be powered from a switching converter was enabled for only 10% of the operation time, then using an LDO instead of a switcher would result in a drop of less than 0.75% in overall efficiency. This is illustrated more clearly in Table 1.

If the 3.3-V output was on all the time, using an LDO instead of an inductive switcher would reduce the overall efficiency by nearly 4%. These two cases are clearly extremes but illustrate how the duty cycle affects the overall efficiency. As the duty cycle for an output increases, the calculation of solution size versus efficiency must be examined to determine the optimal solution.

Conclusion

Selecting between the many different options available for dc/dc conversion can be a daunting task. Requirements such as available space, available input power, output power, duty cycle, and cost all must be examined to choose the best solution. We can start by ranking the requirements by importance, then select the topology for each output based on the requirements. Finally, we can choose the most cost-effective solution for each output. Following these simple steps should take the difficulty out of power-supply design.

Related Web sites

power.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with bq24010, TPS5431, TPS62201, TPS65010, TPS71525, TPS75003, or TPS76925

Table 1. Effective efficiency calculations*

POWER RAIL	LDO OR SWITCHER?	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	POWER (W)	DUTY CYCLE (%)	EFFECTIVE POWER (W)	EFFICIENCY (%)	POWER LOSS (W)
P_1	Switcher	1.35	0.106	0.1431	100	0.1431	90	0.016
P_2	LDO	2.5	0.05	0.125	100	0.125	63	0.075
P_3	Switcher	1.25	0.3	0.375	100	0.375	90	0.042
P_4	LDO	1.65	0.112	0.1848	100	0.1848	41	0.263
P_5	Switcher	3.3	0.42	1.386	10	0.1386	90	0.015
			TOTALS	**2.2139**		**0.9665**		**0.411**

System Efficiency: 70.15%

POWER RAIL	LDO OR SWITCHER?	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (A)	POWER (W)	DUTY CYCLE (%)	EFFECTIVE POWER (W)	EFFICIENCY (%)	POWER LOSS (W)
P_1	Switcher	1.35	0.106	0.1431	100	0.1431	90	0.016
P_2	LDO	2.5	0.05	0.125	100	0.125	63	0.075
P_3	Switcher	1.25	0.3	0.375	100	0.375	90	0.042
P_4	LDO	1.65	0.112	0.1848	100	0.1848	41	0.263
P_5	LDO	3.3	0.42	1.386	10	0.1386	83	0.029
			TOTALS	**2.2139**		**0.9665**		**0.425**

System Efficiency: 69.45%

Difference: 0.71%

*Assuming 4-V battery operation and switching-converter efficiency of 90%

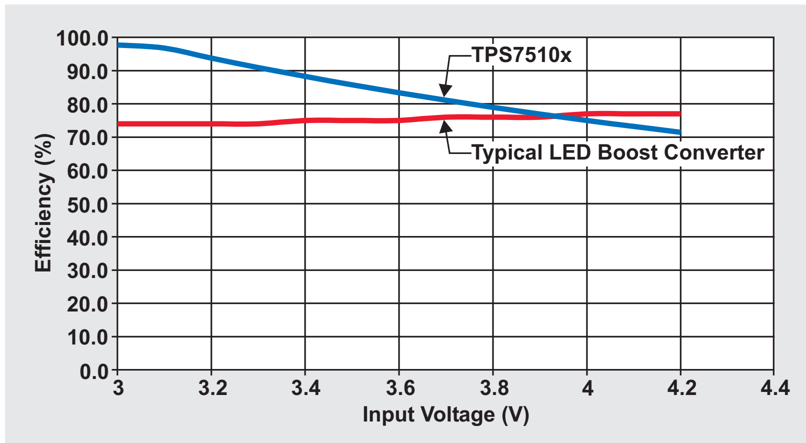
LDO white-LED driver TPS7510x provides incredibly small solution size

By William Hadden (Email: willhadden@ti.com)
Applications Engineer, High Performance Analog, Low Power dc/dc

Introduction

Use of white-LED drivers has increased in recent years due to the popularity of color LCD screens on most portable electronic equipment. The white backlight required to bring out the color in these screens is most often provided by white LEDs. In applications powered by a one-cell Li-ion battery, charge pumps or boost converters have been required to drive these LEDs because of their high forward voltage (4 V typical). As white-LED technology has advanced, the forward voltage required has significantly dropped. Today, white LEDs such as Nichia's NHSW046 or NSSW100C are available with a typical forward voltage of less than 3 V. The lower forward voltage eliminates the need for voltage boosting, permitting the use of linear regulation topologies that reduce costs and solution size and increase efficiency across the battery-discharge range. Figure 1 compares the efficiency and battery voltage of the Texas Instruments TPS7510x and a typical series LED boost converter.

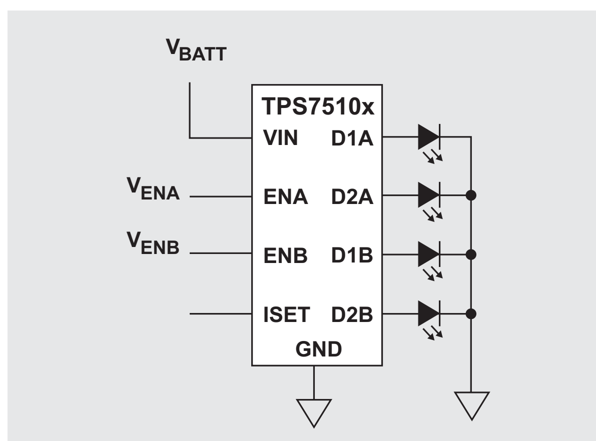
Figure 1. Efficiency versus battery voltage of TPS7510x and typical LED boost converter



TPS7510x family

The TPS7510x low-dropout (LDO) matching LED current source is a highly integrated white-LED driver optimized for low-power keypad and navigation pad LED backlighting applications. The device provides a constant, matched current for up to four unmatched LEDs organized into two banks of two LEDs, each in a common-cathode topology. Inputting a PWM signal on each EN pin allows brightness to be varied from off to full brightness. Each bank has independent enable control, but all four channels are concurrently current-matched. The input supply range is ideally suited to single-cell Li-ion battery supplies and provides up to 25 mA of current per LED over the entire input range. The typical 70-mV dropout voltage allows the circuit to drive the white LEDs from a standard one-cell Li-ion battery. No internal switching signals are used, eliminating troublesome EMI. The TPS7510x is offered in an ultra-small 9-ball, 0.4-mm ball-pitch wafer chip scale package (WCSP) and a 3 × 3-mm QFN package. The package size coupled with the high integration yields a very small solution footprint. Figure 2 shows the typical operating circuit for the TPS7510x.

Figure 2. TPS75105 LDO white-LED driver



The output of each LED is regulated independently, and all of the outputs are typically within 2% of each other. The ISET input allows the user to program any LED current up to 25 mA. If ISET is unconnected, the TPS7510x uses the factory default current setting. The default current settings available in the general catalog are 3 mA (TPS75103) and 5 mA (TPS75105). Default settings are available between 1 and 10 mA in 1-mA increments but may require minimum order quantities.

The TPS7510x does not require input or output capacitors for stability. If the default current setting is used, no external parts other than the LEDs are required. This results in a solution size of less than 1.5 mm^2. A photograph of the EVM layout, including pads for the optional set resistor and input capacitor, is shown in Figure 3. The solution size for this layout with the extra components is still only 25 mm^2.

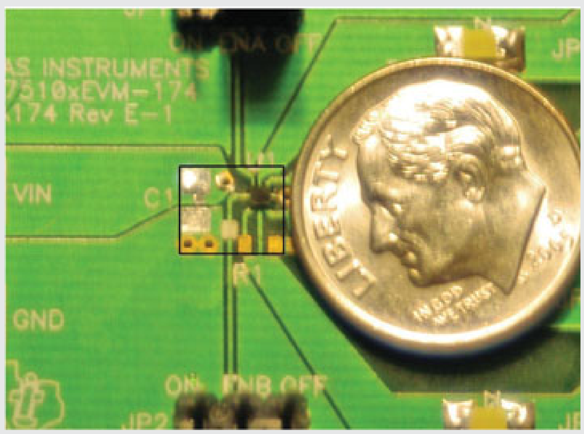
Conclusion

Historically, charge pumps or inductor boost converters have been used to drive white LEDs in most backlighting applications. As the LED technology has improved, forward voltages have dropped. In many low-power applications, the LED forward voltage is less than 3 V. In these applications, the TPS7510x LDO white-LED driver IC provides an excellent solution. The LDO topology eliminates EMI and, with no required external components and the ultrasmall WCSP or QFN package, the total solution size is drastically reduced to just 1.5 mm^2 or 9 mm^2, respectively.

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS75103
www.ti.com/sc/device/TPS75105

Figure 3. EVM solution layout (25 mm^2)



Power management for processor core voltage requirements

By Adrian Harris (Email: aharris@ti.com)
Applications Specialist

Introduction

Today's high-performance processors have very stringent power requirements. Typically, the power requirements consist of at least two supply voltage requirements. One voltage requirement is for the processor core voltage, V_{CORE}, while the others are input-output voltage requirements, V_{IO}.

The core-voltage requirement ranges from 0.9 to 1.3 V and is usually defined by specific processor performance criteria. The latest core-supply voltage tolerance requirements are typically ±3%. The presence of large current transients makes the task of delivering reliable processor power even more challenging.

To meet these challenges, Texas Instruments (TI) introduces its plug-in power series of fast-transient-response power modules. These high-performance products have been designed to deliver reliable processor core power that is compact and cost-effective.

TMS320TCI648x digital signal processor power requirements

An example of a high-performance processor is TI's new TMS320TCI648x digital signal processor. Upon inspection of this product's datasheet and the associated power requirements, we find the following information.

Voltage tolerances, noise and transients

The voltage tolerances specified in the datasheet include all DC tolerances and the transient response of the power supply. These tolerances include the absolute maximum and minimum levels that must be maintained at the pins of the TCI6488 under all conditions. Special attention to the power supply solution is needed to achieve this level of performance, especially the 3% tolerance on the core power plane (V_{CORE}). In order to maintain the 3% tolerance at the pins, the tolerance must be a combination of the power supply DC output accuracy and the effect of transients. A reasonable goal for the DC power supply output accuracy is 1.5%, leaving 1.5% for the transients. At a nominal 1.0-V V_{CORE}, 3% tolerance is ±30 mV. This allows 15 mV of DC accuracy from the output of the power supply and another 15 mV due to transients.

With large current transients, a core-voltage requirement of ±3% tolerance and 1 V is nearly impossible to meet using a traditional solution. Usually, a custom-designed power module or an entirely discrete solution with an application specific-control design is required.

Second generation PTH series (T2) power modules

The new T2 series of plug-in power modules shown in Appendix A has a new patent-pending feature called TurboTrans™. TurboTrans technology allows the designer to customize the power module's control design to meet a target voltage-deviation specification. These T2 products offer the following three primary benefits.

Up to 8× reduction in output capacitance — Fewer capacitors means lower cost and saves board space. In applications with high load transients, these savings could easily be as much as the cost of the module itself.

Faster response to load transients — For a given value of output capacitance, the designer will see up to a 50% reduction in the peak deviation of the output voltage following a load transient.

Enhanced stability when used with ultra-low ESR capacitors — Designers can safely use the latest Oscon®, polymer tantalum or *all-ceramic* output capacitors without stability concerns.

As part of the second-generation PTH products, a new line of ultra-fast-transient-response versions has been developed. These products were designed to meet the challenging power requirements of high-speed processors such as the TMS320TCI648x family. The control design is aggressively compensated beyond that of a standard T2 module. This provides an additional improvement in transient response and the lower cost associated with reduced output capacitance.

For example, let's examine the requirements of the TMS320TCI648x DSP above.

- Core voltage (V_{CORE}) = 1 V
- V_{CORE} tolerance = 3% (1.5% for DC tolerance and 1.5% for AC transients)
- Maximum current transition = 5 A
- Maximum peak voltage deviation with transients = V_{CORE} × 1.5% = 15 mV
- **Output impedance requirement = 15 mV ÷ 5 A = 3 mV/A**

In order to meet the voltage tolerance requirement for the TMS320TCI648x, the power supply must have an output impedance of 3 mΩ or less. This requirement is beyond the capability of any standard, "off-the-shelf" power module.

Figure 1 shows that the competitive module cannot meet the 3-mΩ requirement. Even with a standard PTH08T240W module, the low-impedance requirement cannot be achieved without a large amount of capacitance. The PTH08T240F module, however, can meet the requirement with only 3000 µF of external output capacitance. Typical designs are shown in Appendix B.

Summary

TI's new line of ultra-fast-transient-response modules was designed to meet the challenging supply-voltage requirements of the latest system processors. These modules permit system designers to optimize transient performance while minimizing the need for output capacitance, thus optimizing board space and reducing system cost.

Related Web sites

power.ti.com
dsp.ti.com
www.ti.com/sc/device/PTH08T240F
www.ti.com/sc/device/PTH08T240W

Figure 1. Transient response versus capacitance chart

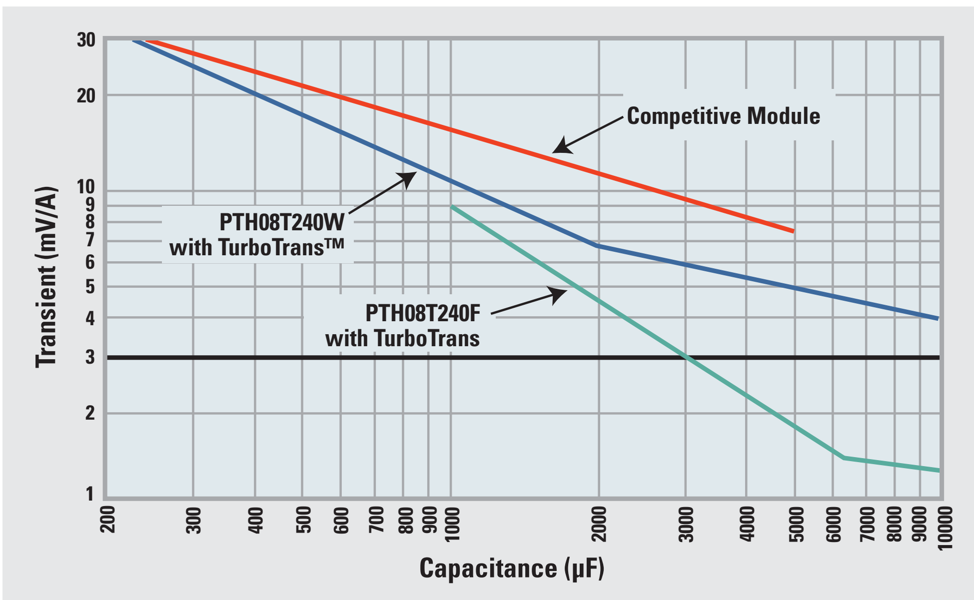


Figure 1 compares the output impedance characteristics of a standard T2 module, PTH08T240W; a fast-transient-response module, PTH08T240F; and a similarly rated competitive product.

Appendix A: T2 product selection tables

Standard – T2 non-isolated point-of-load modules

V_{IN} (V)	DESCRIPTION	3 A	6 A	10 A	16 A	30 A	50 A
+3.3	T2 PTH	**PTH04T260W**	**PTH04T230W**	**PTH04T240W**	**PTH04T220W**	PTH04T210W	
+5	T2 PTH	**PTH04T260W**	**PTH04T230W**	**PTH04T240W**	**PTH04T220W**	**PTH05T210W**	
		PTH08T260W	**PTH08T230W**	**PTH08T240W**	**PTH08T220W**		
+12	T2 PTH	**PTH08T260W**	**PTH08T230W**	**PTH08T240W**	**PTH08T220W**	**PTH08T210W**	**PTV08T250W**

Released products are listed in **bold red**.

Ultra-fast transient response – T2 non-isolated point-of-load modules

V_{IN} (V)	DESCRIPTION	3 A	6 A	10 A	16 A	30 A	50 A
+3.3	T2-F PTH	PTH04T260F	PTH04T230F	PTH04T240F	PTH04T220F	PTH04T210F	
+5	T2-F PTH	PTH04T260F	PTH04T230F	PTH04T240F	PTH04T220F	PTH05T210F	
		PTH08T260F	PTH08T230F	**PTH08T240F**	PTH08T220F		
+12	T2-F PTH	PTH08T260F	PTH08T230F	PTH08T240F	PTH08T220F	PTH08T210F	PTV08T250F

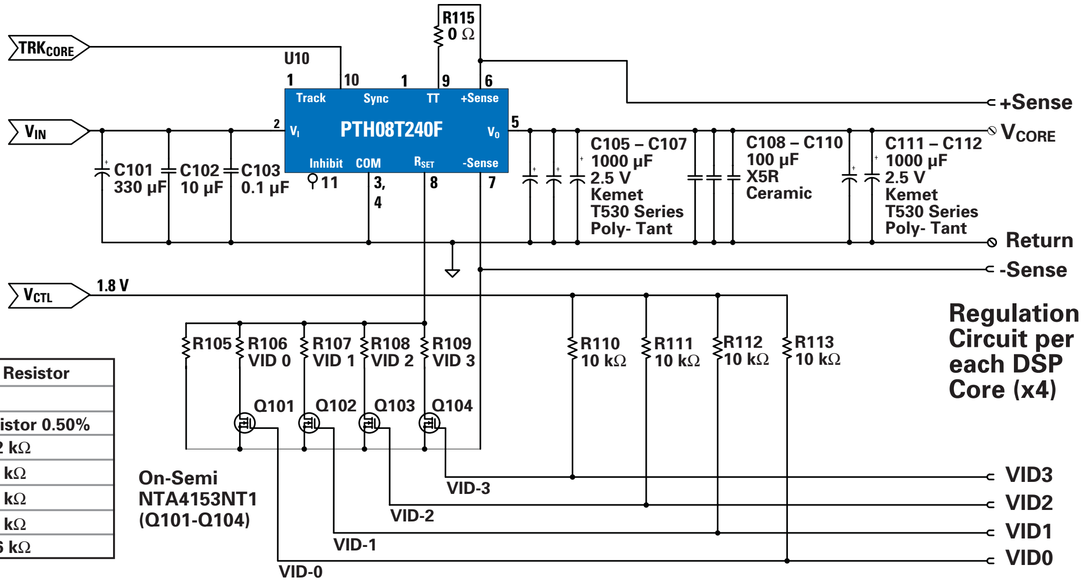
Released products are listed in **bold red**. Depending on the business opportunity and system requirements, additional products may be developed upon request.

Appendix B: Faraday DSP's scaled core expanded designs

PTH08T240F Transient Performance Data (Kemet T530 Series - Polymer Tantalum Bulk Capacitors)

Output Voltage Truth Table				
VID3	VID2	VID1	VID0	V_{CORE}
0	0	0	0	0.900 V
0	0	0	1	0.913 V
0	0	1	0	0.927 V
0	0	1	1	0.940 V
0	1	0	0	0.953 V
0	1	0	1	0.967 V
0	1	1	0	0.980 V
0	1	1	1	0.993 V
1	0	0	0	1.007 V
1	0	0	1	1.020 V
1	0	1	0	1.033 V
1	0	1	1	1.047 V
1	1	0	0	1.060 V
1	1	0	1	1.073 V
1	1	1	0	1.087 V
1	1	1	1	1.100 V

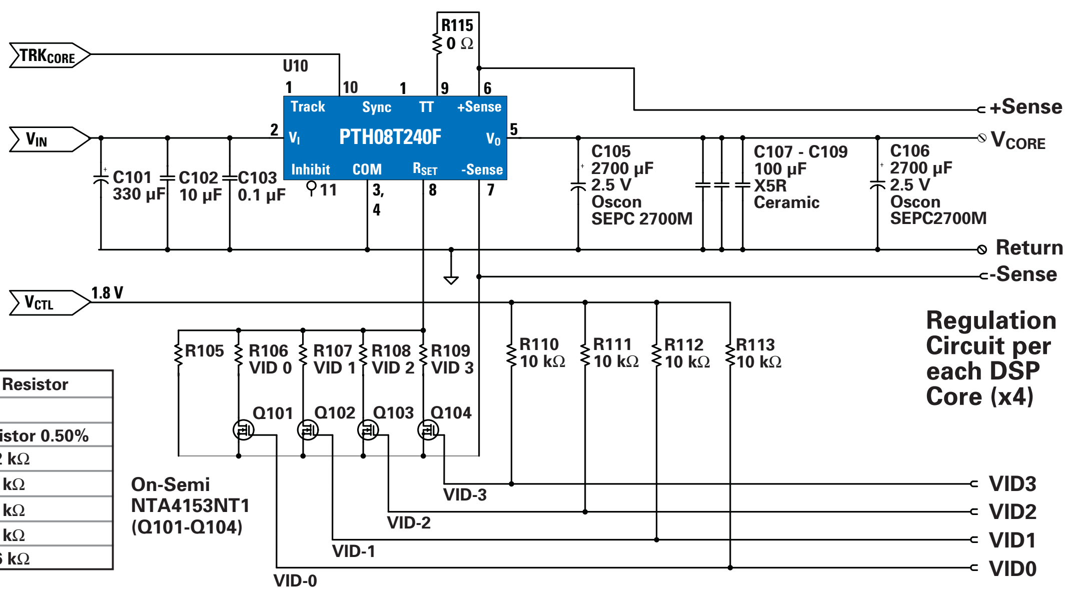
	VID Identification Resistor Component	
VID Code	Designator	Resistor 0.50%
no code	R105	31.2 kΩ
VID 0(LSB)	R106	453 kΩ
VID 1	R107	229 kΩ
VID 2	R108	117 kΩ
VID 3(MSB)	R109	57.6 kΩ



PTH08T240F Transient Performance Data (OSCON SEPC Series Bulk Output Capacitors)

Output Voltage Truth Table				
VID3	VID2	VID1	VID0	V_{CORE}
0	0	0	0	0.900 V
0	0	0	1	0.913 V
0	0	1	0	0.927 V
0	0	1	1	0.940 V
0	1	0	0	0.953 V
0	1	0	1	0.967 V
0	1	1	0	0.980 V
0	1	1	1	0.993 V
1	0	0	0	1.007 V
1	0	0	1	1.020 V
1	0	1	0	1.033 V
1	0	1	1	1.047 V
1	1	0	0	1.060 V
1	1	0	1	1.073 V
1	1	1	0	1.087 V
1	1	1	1	1.100 V

	VID Identification Resistor Component	
VID Code	Designator	Resistor 0.50%
no code	R105	31.2 kΩ
VID 0(LSB)	R106	453 kΩ
VID 1	R107	229 kΩ
VID 2	R108	117 kΩ
VID 3(MSB)	R109	57.6 kΩ



Accurately measuring ADC driving-circuit settling time

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Introduction

Many modern data acquisition systems consist of high-speed, high-resolution ADCs.[1] CMOS-switched, capacitor-based ADCs are often chosen for such designs due to their low cost and low power dissipation. These ADCs use an unbuffered front end directly coupled to the sampling network. To effectively minimize noise and signal distortion, it is necessary to drive the ADC with a high-speed, low-noise, low-distortion operational amplifier.[2] To achieve minimal distortion it is important for the op amp output to settle to the desired accuracy within the acquisition time of the ADC. Normally the op amp settling time is either calculated from the frequency response specified in the datasheet or measured by probing the output with an oscilloscope that has a limitation on resolution. Sometimes the difference between the op amp input and output is amplified to achieve better accuracy. These methods are limited by the oscilloscope resolution or circuit parasitic. Moreover, the settling time of the op amp is affected by the parasitic capacitance and inductance introduced by the oscilloscope probe. In another method, the difference between output and input is amplified to increase the resolution of the measurement. None of these methods includes the parasitic capacitance and inductance present in the ADC sampling circuit and package.

Definition of settling time

Settling time is the time elapsed from the application of an ideal instantaneous step input to the time at which the closed-loop amplifier output has entered and remained within a specified symmetrical error band. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of the final value, recover from the overload condition associated with slewing, and finally settle to within the specified error. For high-resolution ADCs, the specified error band is usually one fourth of one least significant bit (LSB) of the ADC.

Basic setup

The ADC used here is the Texas Instruments (TI) ADS8411, which is a 16-bit, 2-MSPS successive approximation register (SAR) ADC. The driver op amp is the TI THS4031. Figure 1 shows the evaluation setup.

The instantaneous step input is generated with an analog multiplexer (MUX) (the TI TS5A3159) by switching its two channels. A dc voltage, V, is applied to channel 2, and channel 1 is connected to ground; so this setup can produce a step input rising to V from 0 or falling to 0 from V. Alternatively, the step input can be generated from any step generator. The step generator should settle much faster than the op amp settling time.

Explanation

Step 1

ADC samples channel 1 (connected to ground) first. A long sampling time is provided to make sure that the input capacitor of the ADC is fully discharged.

Step 2

The analog MUX is switched to channel 2 from channel 1 at instant A in Figure 2. This diagram shows the voltage at point S (Figure 1) when the MUX switches over to channel 2 from channel 1. The settling time of the MUX is denoted by t_s. It is assumed that t_s is much shorter than the op amp settling time.

Figure 1. Settling time evaluation setup

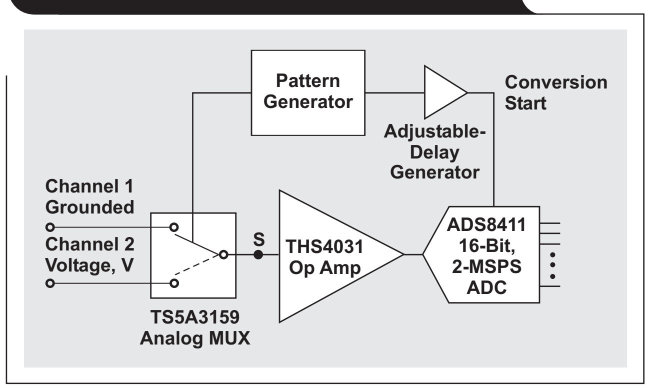
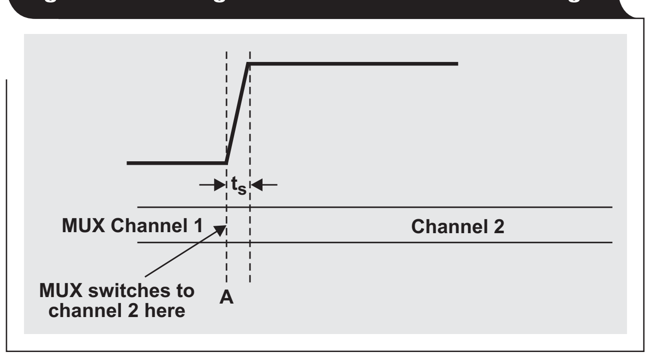


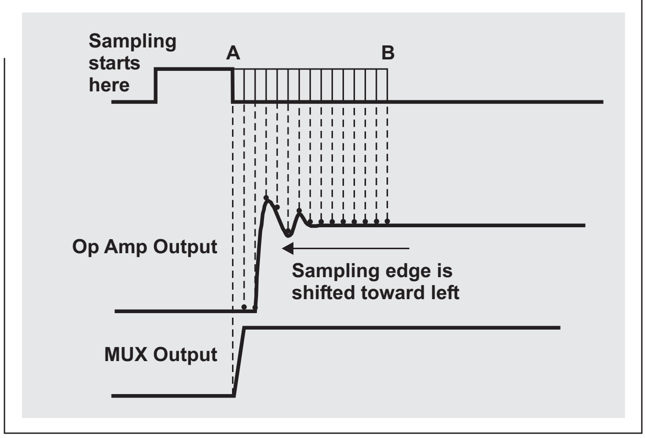
Figure 2. Settling time for MUX channel change



Step 3

Once the analog MUX is switched at instant A, the input of the op amp starts changing. The output of the op amp starts changing after a very brief propagation delay after instant A. The op amp settling time (t_{ideal}) is approximately calculated from the slew rate and bandwidth specified in the op amp datasheet. The method proposed here plots the op amp output from instant A to instant B (Figure 3). The time difference between instant B and instant A is $2t_{ideal}$.

Figure 3. Averaging n samples from B to A increases accuracy



Step 4

The first ADC sampling edge appears at instant B, and n number of readings (digital outputs from the ADC) are taken. The n number of readings are averaged for better accuracy (discussed later). Next the sampling edge is shifted to the left by 1 ns (Figure 3) with the help of a pattern generator and an adjustable-delay generator (Figure 1), and again n number of readings are taken. This way the sampling edge is shifted toward the left from instant B to instant A in 1-ns steps. At each sampling edge the average is stored in an element of an array. The array is plotted against the time to get the true picture of the op amp output settling (Figure 3).

Averaging to achieve better resolution

Input of an n-bit ADC should settle to at least n+2 bits, but measured output is an n-bit digital code from the ADC. The resolution can be increased by repeatedly sampling the same input and taking multiple (n) readings from the ADC. Finally an average is taken on the n digital output codes. It can be shown that for each additional bit of resolution, the number of readings should be 4, so w extra bits of resolution require 4^w readings.

For each additional bit, the signal-to-noise ratio (SNR) increases by 6.02 dB. In this case the 16-bit ADC should settle with at least 18-bit accuracy.

$$\text{SNR} = 6.02 \times \text{N} + 1.76,$$

where N is the ADC resolution. SNR is 110.08 dB for 18-bit accuracy, so an extra bit (w) of resolution required is

$$\frac{110.08 - 86^*}{6.02} = 4.$$

The number of samples (n) needed for each reading is $4^4 = 256$.

Results

An RC filter is used at the output of the op amp to filter the external noise. An ADC sampling circuit always consists of another RC (R′, C′), as shown in Figure 4.

Figure 5 shows the settling behavior when three different values of an external capacitor are used for RC filtering.

*Typical SNR specification of ADS8411

Figure 4. Typical noise filter

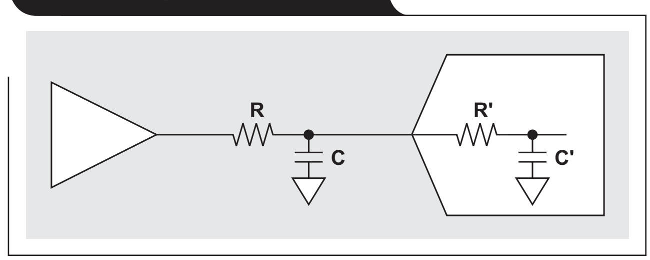


Figure 5. Input settling time with an external capacitor

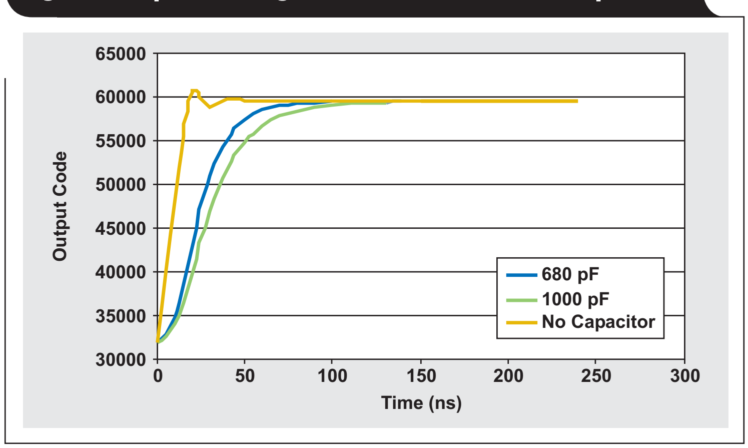


Figure 6. Expanded scale magnifies settling-time behavior shown in Figure 5

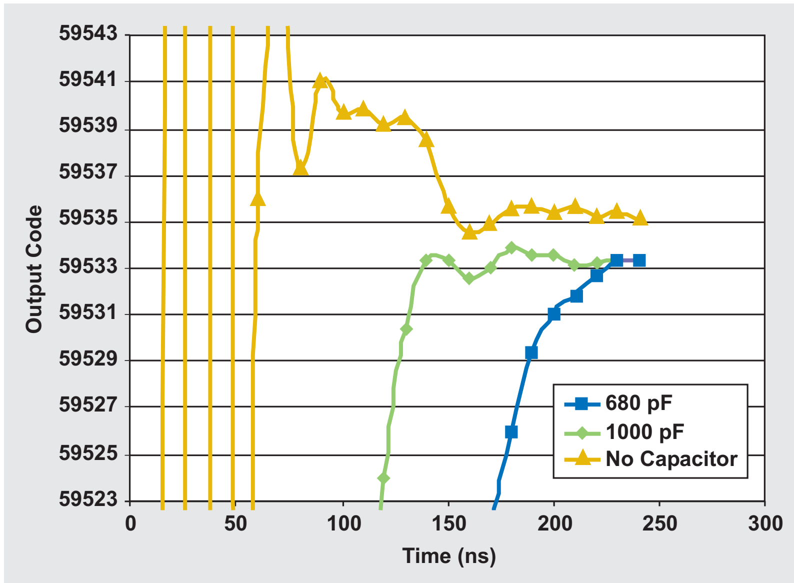


Figure 6 is a zoomed-in version of Figure 5 to show the settling more accurately. While the output code is based on 16-bit sampling, the resolution of the measurement is more than 16-bit because 65536 samples were captured and averaged for each reading. The result shows significant ringing and underdamping of the system when no capacitor was used. Also note that use of a bigger (1000-pF) capacitor significantly increases the settling time.

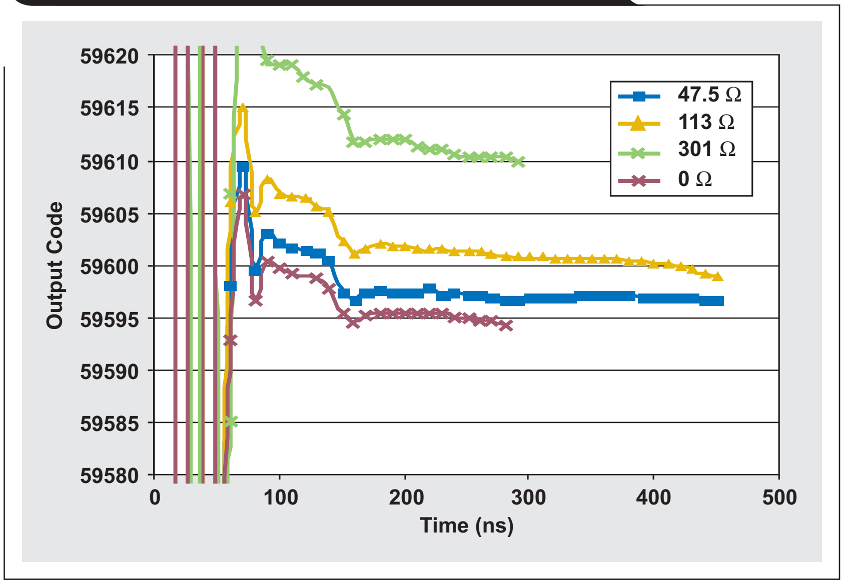
A summary of these results is shown in Table 1. Averaging the output data can improve the resolution of the result beyond 16-bit.

Table 1. Comparison of edge-shift method versus traditional method

<table>
<tr><th colspan="2">METHOD</th><th>CAPACITOR, C (pF)</th><th>ACCURACY* (%)</th><th>SETTLING TIME (ns)</th></tr>
<tr><td rowspan="2">Datasheet Specification</td><td>10-Bit</td><td rowspan="2">No Spec</td><td>0.1</td><td>45</td></tr>
<tr><td>13-Bit</td><td>0.01</td><td>80</td></tr>
<tr><td colspan="2" rowspan="9">Edge-Shift Method (R = 20 Ω)</td><td rowspan="3">25</td><td>0.1</td><td>55</td></tr>
<tr><td>0.01</td><td>140</td></tr>
<tr><td>0.0015</td><td>150</td></tr>
<tr><td rowspan="3">680</td><td>0.1</td><td>109</td></tr>
<tr><td>0.01</td><td>130</td></tr>
<tr><td>0.0015</td><td>140</td></tr>
<tr><td rowspan="3">1000</td><td>0.1</td><td>152</td></tr>
<tr><td>0.01</td><td>195</td></tr>
<tr><td>0.0015</td><td>220</td></tr>
</table>

*16-bit LSB deviation = 0.0015%

Figure 7. Effects of changing feedback resistors



Measurement of bias current

Figure 7 shows op amp settling behavior with different values of feedback resistors. The difference between the settled voltages indicates the offset voltage shift caused by bias current. From this the bias current can be calculated as 3 µA, which matches the typical specification of the THS4031. This experiment validates the correctness of this setup.

Bias current calculation

The settled value with 0 Ω in the feedback is 59595. The settled value with 301 Ω in the feedback is 59610.

Delta (offset voltage) = bias current × resistor (used in the feedback).

$$\text{Delta (offset voltage)} = \frac{(59610 - 59595) \times 4.096}{65536} = 938\ \mu\text{V}.$$

$$\text{Bias current} = \frac{938}{301} = 3.12\ \mu\text{A}$$

(compared to the datasheet typical specification of 3 µA).

Conclusion

This is a practical and simple method to accurately measure the settling time of an ADC driving circuit. The settling behavior is unaffected by the measurement, because no additional component is used for the setup. This method can be implemented as a built-in self-test (BIST) in the future. The averaging of multiple readings improves the accuracy of the result.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. Kevin M. Daugherty, *Analog to Digital Conversion: A Practical Approach* (McGraw-Hill Companies, 1993).	—
2. Ron Mancini, ed., "Op Amps for Everyone," Design Reference (Rev B)	slod006

Related Web sites

amplifier.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with ADS8411, THS4031, or TS5A3159

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