Get low-noise, low-ripple, high-PSRR power with the TPS717xx

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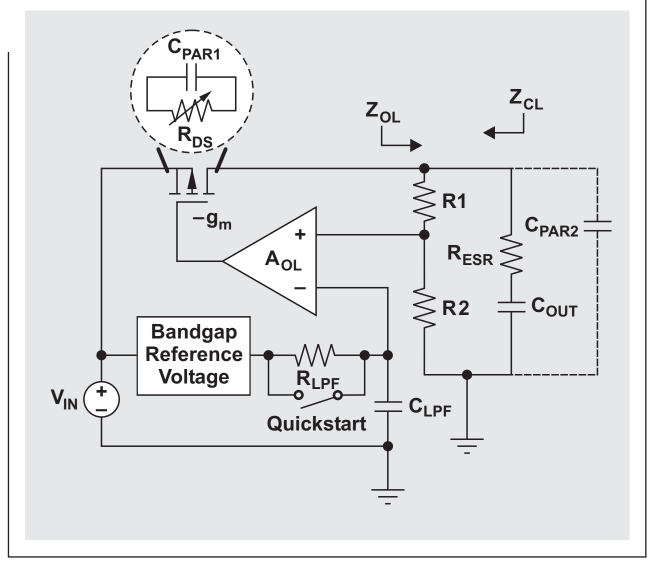
Introduction

While highly efficient switching power supplies are commonly used for long battery life in portable end equipment such as mobile phones and PDAs, the internal circuitry of some of these devices is sensitive to noise and therefore does not operate properly when powered from a switching power supply with output ripple. Audio circuitry, PLLs, RF transceivers, and DACs are just a few examples of such circuits. Linear regulators are ideal for powering these circuits.

Figure 1 shows a simplified block diagram of a linear regulator using a p-channel MOSFET (pFET) as a pass element. A_{OL} is the open-loop gain of the error amplifier, and g_m is the pass-element transconductance. The error amplifier controls the voltage at the gate of the pass element so that the current through the FET keeps the output voltage regulated relative to the internal reference voltage. Assuming that the low-pass filter (LPF) formed by R_{LPF} and C_{LPF} eliminates nearly all internal-reference noise, the output voltage should be ripple- and noise-free for frequencies within the bandwidth of the regulator's control loop. The concept is easy to understand, but achieving a high power-supply rejection ratio (PSRR) over a wide bandwidth with very low quiescent current and in a small package requires innovative circuits. This article highlights the TPS717xx single-output linear regulator, which provides high power-supply rejection (PSR) over a wide bandwidth with very low quiescent current and in a small package. Similar, dual-output versions are available with the TPS718xx and TPS719xx families. This article also provides guidance on component selection and layout techniques for maximizing PSR and minimizing the regulator's self-generated white noise.

Figure 1. Simplified block diagram of a linear regulator



What is the PSRR?

The PSRR is a measure of a circuit's PSR expressed as a ratio of output noise to noise at the power-supply input. It provides a measure of how well a circuit rejects ripple at various frequencies injected from its input power supply. In the case of linear regulators, PSRR is a measure of the regulated output-voltage ripple compared to the input-voltage ripple over a wide frequency range and is expressed in decibels (dB). If the pass element in Figure 1 is treated as a variable resistance, R_{DS}, and the error amplifier and bandgap reference are assumed to have been designed to minimize pass-through of the input-voltage ripple, then the PSR is simply a voltage divider, expressed as

$$PSR = \frac{Z_{OL} \parallel Z_{CL}}{Z_{OL} \parallel Z_{CL} + R_{DS}}.$$

In this equation, Z_{OL} is the output impedance at the regulator's output, ignoring the effect of the regulator's feedback loop:

$$Z_{OL} = (Z_{COUT} + R_{ESR}) \parallel (R1 + R2) \parallel C_{PAR2},$$

where Z_{COUT} and R_{ESR} are the output capacitor's impedance and equivalent series resistance (ESR), respectively, and C_{PAR2} is the parasitic capacitance of the output components and PCB. Z_{CL} is the impedance looking back into the output of the regulator, including the effect of the regulator's feedback loop:

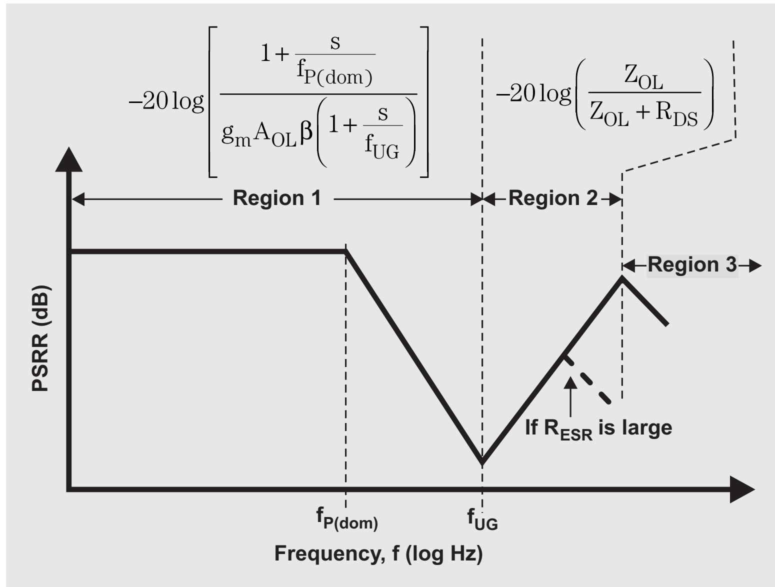
$$Z_{CL} = \frac{Z_{OL} \parallel R_{DS} \parallel C_{PAR1}}{g_m \times A_{OL} \times f \times \beta},$$

where C_{PAR1} is the passive-element parasitic capacitance, f is the ripple frequency, and β is the feedback factor,

$$\beta = \frac{R2}{R1 + R2}.$$

Figure 2 shows the general shape of a PSRR curve, where $f_{P(dom)}$ is the dominant pole and f_{UG} is the unity-gain bandwidth. If the error amplifier is compensated to have a single-pole response, then the Region 1 PSR for amplifier frequencies below f_{UG} can be approximated by the equation on the left side of the graph. Designing the regulator with a high-gain, wide-bandwidth error amplifier can therefore provide high PSR over a wide range of frequencies. In Region 2, above the control-loop bandwidth, the regulator is no longer effective at providing PSR, so the PSRR reduces to a simple voltage divider as shown on the right side of the curve. As Z_{COUT} decreases relative to R_{DS}, the PSR provided by the passive components on the board increases. If C_{OUT} has high R_{ESR}, the PSR peaks sooner. In Region 3, the IC and board parasitic capacitances (C_{PAR1} and C_{PAR2}) dominate, resulting in a capacitive voltage divider, which typically causes the PSR to decrease again. A larger output capacitor with less ESR will typically improve PSRR in this region, but it can also actually decrease the PSRR at some frequencies. This occurs because increasing the output capacitor may lower $f_{P(dom)}$ and/or f_{UG}, depending on how the regulator is compensated, thereby causing the open-loop gain to roll off sooner.

Figure 2. PSRR graph

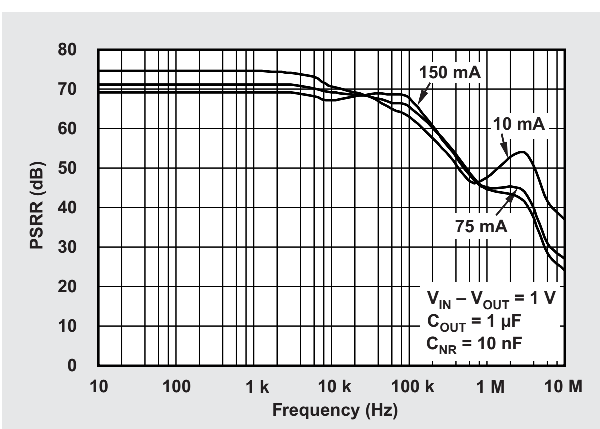


Maximizing PSR

The TPS717xx family of regulators has incorporated both well-known and patentable circuit techniques to provide high PSR over a wide frequency range. An example of the PSRR is shown in Figure 3.

With the simple model previously explained, it can be shown that the TPS717xx's dominant pole with C_{OUT} = 1 µF is at approximately 20 to 30 kHz and the unity-gain frequency is near 400 kHz. Since PSR is a function of the open-loop gain, as the gain varies so will the PSR in Regions 1 and 2 of Figure 2. Figure 3 shows the TPS717xx's PSRR varying with load current. As load current increases, R_{DS} decreases; therefore Z_{CL} decreases, since a MOSFET's output impedance is inversely proportional to its drain current. In many regulators, where $f_{P(dom)}$ varies with Z_{CL}, increasing the load current also pushes $f_{P(dom)}$ to higher frequencies, which increases the feedback-loop bandwidth. As shown in Figure 3, the net effect of increasing the load current is reduced PSRR.

Figure 3. TPS717xx PSRR graph



The differential DC voltage between input and output also affects PSR. As $V_{IN} - V_{OUT}$ is lowered, the pFET (which provides gain) is driven out of the active (saturation) region of operation and into the triode/linear region, which causes the feedback loop to lose gain. Therefore, the PSR of the regulator decreases as V_{IN} approaches V_{OUT}. The lowest PSR, approaching 0 dB, occurs when the device is in dropout ($V_{IN} \approx V_{OUT}$). In this situation, the RC filter formed by the linear regulator's pass-element R_{DS} and output capacitor determines PSR.

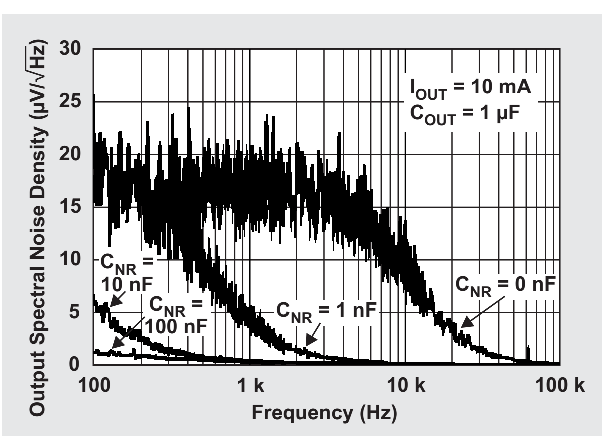
Low noise

A linear regulator's self-generated noise is sometimes confused with its PSRR. However, noise is generated by the transistors and resistors in the regulator's internal circuitry as well as by the external feedback resistors. Transistors generate shot noise and flicker noise, both of which are directly proportional to current flow. Flicker noise is indirectly proportional to frequency and so is higher at low frequencies. The resistive element of MOSFETs also generates thermal noise like resistors. Thermal noise is directly proportional to temperature, the resistor's resistance value, and the current flow through the transistors. Transistors and resistors closest to the error-amplifier inputs in the small-signal path cause the most output noise because their noise is amplified by the regulator's closed-loop gain ($A_{CL} = V_{OUT}/V_{Bandgap} = 1/\beta = 1 + R1/R2$). The noise contribution from components later in the signal path is insignificant when compared to the noise at the error-amplifier inputs. In fact, when modest-sized feedback resistors are used, most of the regulator's noise comes from the amplified bandgap reference. As shown in Figure 1, the simplest way to reduce the bandgap noise is to use a low-pass filter (LPF) consisting of an internal resistor, R_{LPF}, and an external capacitor, C_{LPF}. At startup, this filter would slow down the output-voltage rise without the aid of the "quickstart" transistor. When the quickstart transistor is used, it shorts out the R_{LPF} for a short time at startup so the regulator output can rise quickly. Larger noise capacitors such as C_{LPF} in Figure 1 will reduce the output noise produced by the bandgap until the regulator's other noise sources begin to dominate. Using a noise capacitor that is too large results in the quickstart circuit timer expiring before the $R_{LPF} \times C_{LPF}$ time constant. In this case, the output voltage will rise quickly to a level below regulation and then rise very slowly to its final regulated value.

A regulator's noise output is characterized by two measurements. One is its spectral noise density, a curve that shows noise ($\mu V/\sqrt{Hz}$) versus frequency. The other is the RMS of the spectral noise density integrated over a finite frequency range, also commonly called output-noise voltage (μV_{rms}). Figure 4 shows the TPS717xx's spectral noise density with different C_{NR} values, where C_{NR} is the same as C_{LPF} in Figure 1.

When noise specifications of different regulators are compared, it is imperative that the two regulators' noise measurements be taken over the same frequency range and at the same output voltage and current values. When output noise values for regulators at two different output voltages are compared, an approximate noise value can be used that is computed by scaling one of the noise measurements by the ratio of the two output voltages. When a noise-capacitor pin is not available, adding a capacitor across R1 reduces the noise by reducing the closed-loop gain at high frequencies. However, this could potentially slow down start-up time, since the capacitor would have to be charged by the current in the resistor divider; adding such a capacitor could also potentially make the feedback loop unstable.

Figure 4. TPS717xx spectral noise density



Component selection and board layout

Proper board layout and capacitor selection are critical to maximizing PSR and minimizing noise. Low-ESR output capacitors maximize PSR at high frequencies but may increase noise. The reason for this is that the low impedance created by the output capacitor and its ESR may improve stability and PSR by removing peaking in the control loop at frequencies near $f_{P(dom)}$, but removing this peaking would also provide higher gain for the internal noise sources. To maximize PSR and minimize noise, it is recommended that V_{IN} and V_{OUT} have separate ground planes that are connected at the regulator's ground pin. The input, output, and noise-reduction capacitors should be very close to the IC, with the ground of the noise-reduction capacitor as close to the regulator's ground pin as possible.

Conclusion

Linear regulators are ideal for providing a low-ripple, low-noise power rail to sensitive analog circuitry. The TPS717xx single-output and TPS718xx/TPS719xx dual-output linear regulators are specifically designed for providing high PSR over a wide frequency range with low noise. These linear regulators also consume very little quiescent current when powered and even less when shut down, helping maximize battery life in portable powered applications that need bursts of regulator power only at irregular intervals.

References

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