Common-mode transient immunity for isolated gate drivers

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Introduction

Isolated gate drivers are widely used for driving insulated-gate bipolar transistors (IGBTs) and MOSFETs in various applications such as motor drives, solar inverters and automobiles. In addition to turning the IGBTs or MOSFETs on and off, these drivers provide galvanic isolation. The device's switching rate depends on the application and type of the device being used. Switching frequencies of 10 to 20 kHz are common in IGBTs, however, silicon carbide (SiC) and gallium-nitride or GaN-based systems can operate at 50 kHz to 200 kHz. Some advantages for using a higher switching frequency are smaller filter size, fast control and lower distortion. However, these advantages come with an increased power loss during transition. Common-mode transient immunity (CMTI) is an important parameter of a gate driver to consider when operating it at higher switching frequencies. This article gives background on a general pulse-width modulation (PWM) scheme, the transition loss associated with high switching frequency, and isolated gate-driver solutions to reduce transition time.

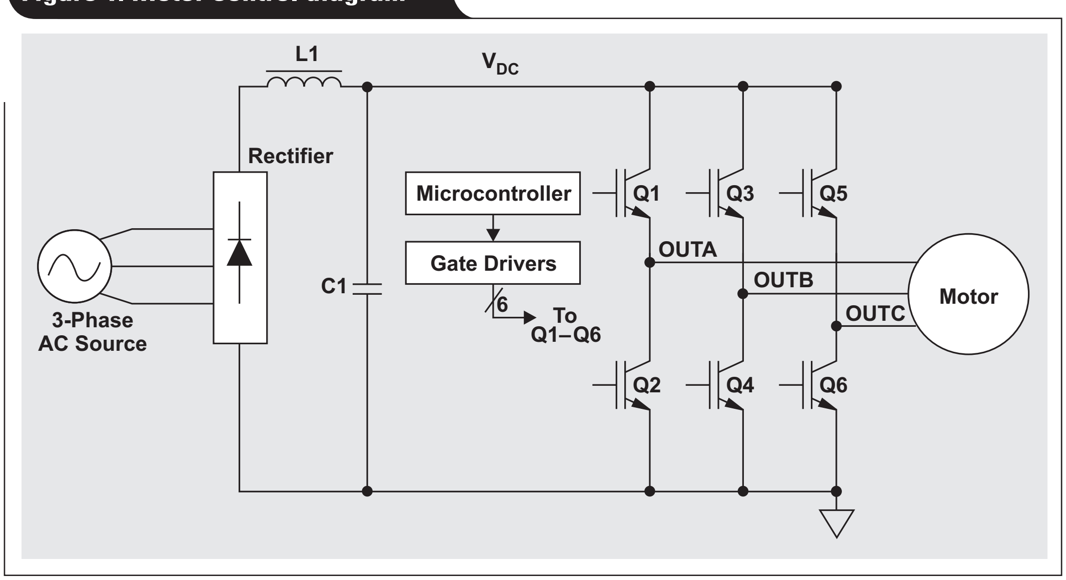
Typical inverter operation

An inverter configuration is used for a DC-to-AC conversion. These voltage-source inverters (VSIs) can be used either for general AC voltage-output generation or motor control. Examples of AC voltage-output applications are solar inverters, uninterruptable power supplies (UPSs), or AC applications powered from a battery in automobiles. The same inverter configuration allows for output-voltage amplitude and frequency control, which is more useful for a motor control. An induction-motor control is a common example of using an inverter for motor control.

Figure 1 contains a high-level diagram of an AC-to-DC and then DC-to-AC conversion. The system has a three-phase input and controllable three-phase AC output. The rectifier block converts the AC to DC, and a filter using L1 and C1 is used to filter out the residual ripple. A key parameter for the rectifier is its power factor. The simplest form of a rectifier uses diodes. Diode-based rectifiers have very poor power factor and are not suitable for high-power applications. Instead, rectifiers using active power factor correction (PFC) are preferred for high-power solutions.[1]

The inverter consists mainly of Q1 through Q6 IGBTs and the gate-driver circuit. Input to the inverter is the DC supply (V_{DC}) produced by the rectifier. The purpose of the inverter is to convert DC to AC voltage. The frequency and amplitude of the inverter output is controlled by how the IGBTs are switched. In applications such as UPSs or solar inverters, a battery supplies power to the inverter. The load can be any general-purpose AC load, or it can connect to the grid. The fundamental structure of the inverter remains the same for many applications.

Figure 1. Motor control diagram



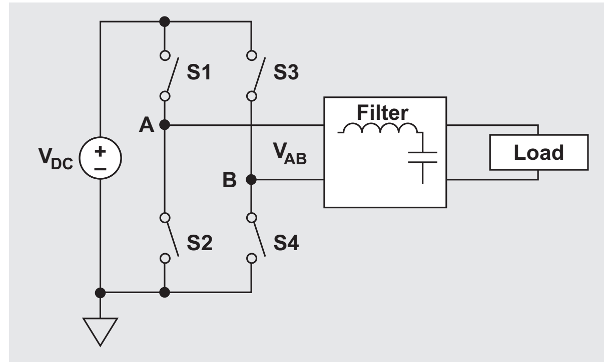
Battery-operated inverters are very common in electric vehicles. A microcontroller is used to produce a PWM waveform to drive the IGBTs and the outputs (OUTA, OUTB and OUTC) switch between 0 V and V_{DC}. An induction motor requires control of voltage and frequency to control its torque and speed. The microcontroller monitors the speed and current in the motor and provides the proper PWM pattern according to user inputs. IGBTs typically require gate drivers with isolated outputs because the output side is switching between 0 V and V_{DC}. The switching frequency of an IGBT-based inverter is typically in the range of 8 to 16 kHz and higher PWM switching frequencies are possible with SiC or GaN IGBTs.[2, 3] In this scenario, gate drivers also need to support faster switching speeds. The inverter can be configured as a single-phase output with only two legs and four switches. Three-phase systems are typically used to get more power.

Pulse-width modulation

PWM or pulse-width modulation is a way to achieve amplitude control by changing the duty cycle.

Figure 2 shows a simple form of a single-phase inverter. Input to the inverter is a DC voltage (V_{DC}) and the voltage across the load is $V_{AB} = V_A – V_B$. The voltage at node A switches between V_{DC} and 0 V via switches S1 and S2. Similarly, the voltage at node B switches between V_{DC} and 0 V via switches S3 and S4. Switches S1 and S2 are complementary, as are switches S3 and S4. The maximum output voltage that can be achieved using this system is V_{DC}. An example of switching waveforms at nodes A and B without filtering is shown in Figure 3. The switching rate can range from 10 to 200 kHz, depending on the application and type of switch. In Figure 3a, the duty cycle at node A is more than 50% and in Figure 3b, the duty cycle is less than 50% at node B. This creates a positive voltage across the load as shown in Figure 3c.

Figure 2. High-level diagram of a single-phase inverter



In Figure 3d, the duty cycle at node A is less than 50% and more than 50% at node B (Figure 3e),which creates a negative voltage across the load (Figure 3f).

The average voltage, V_{AB}, across the load/filter can be written as:

$$V_{AB} = V_{DC} \times D_A – V_{DC} \times D_B \text{ or } V_{AB} = V_{DC} \times (D_A – D_B) \quad (1)$$

where D_A is the duty cycle at node A, and D_B is duty cycle at node B.

Figure 3. Simplified PWM operation with positive and negative output voltages

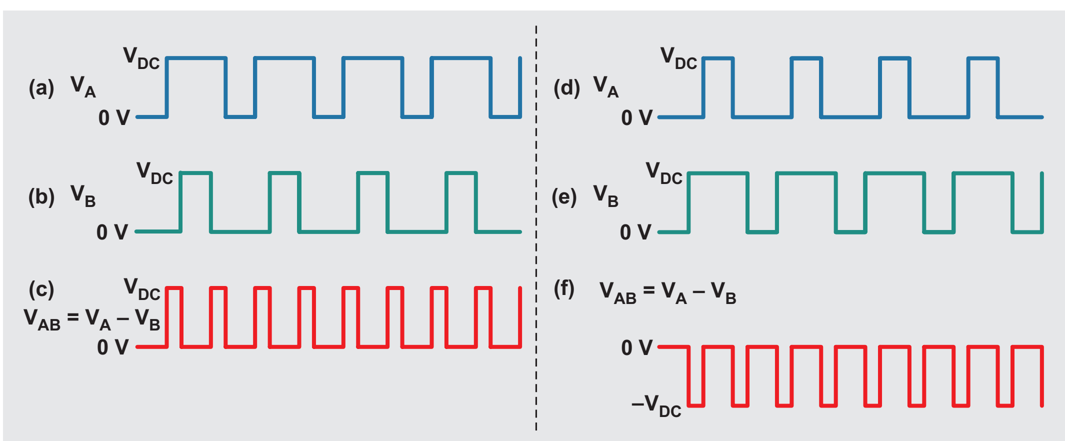
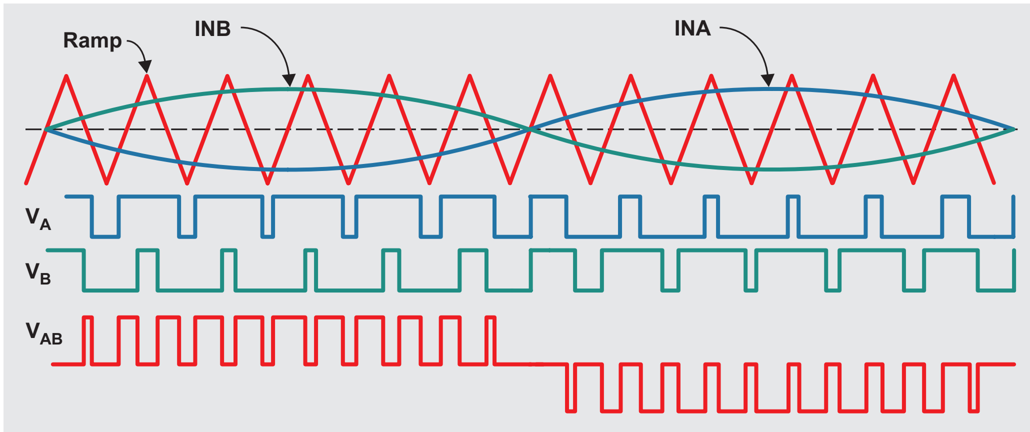


Figure 4. A single-phase PWM output waveform



Controlling the duty cycle, D_A and D_B, allows control of the output voltage, V_{AB}. A sinusoidal single-phase PWM waveform is obtained by comparing a reference sine wave INA and INB with a high-frequency triangular signal as shown in Figure 4.

The fundamental component of the output has an amplitude that is proportional to the differential reference input ($V_{INA} – V_{INB}$), and the frequency is the same as the reference frequency. This allows the voltage and frequency to be controlled by the reference signal. High-frequency tones are at frequencies $2nf_{SW} \pm mf_{IN}$, where f_{SW} is the triangular signal frequency, f_{IN} is the reference input frequency, and the n and m multipliers can be 1, 2, 3, etc. The high-frequency component is filtered by the LC filter, or the motor inductance in the case of motor control.

The ratio between the input signal amplitude and the triangular signal amplitude is called amplitude modulation ratio, or m_A.

$$m_A = \frac{V_{IN}}{V_{RAMP}} \quad (2)$$

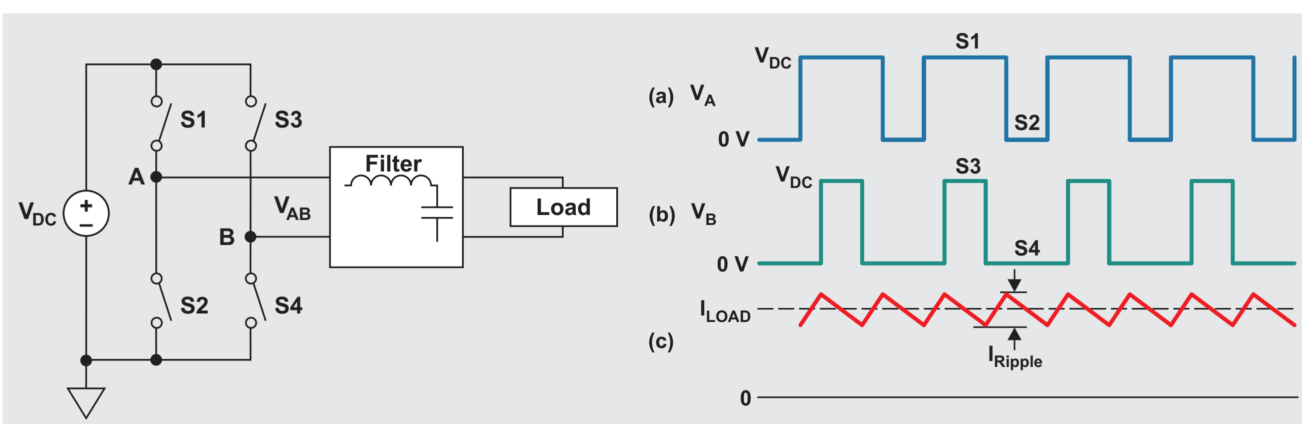
where V_{IN} is the amplitude of the reference input signal and V_{RAMP} is the amplitude of the triangular wave signal. The fundamental output voltage is $m_A \times V_{DC} \times$ sine (ωt); where ω is the frequency of the reference input signal. The root mean square (rms) of the fundamental signal can be written as:

$$V_{RMS} = \frac{m_A \times V_{DC}}{\sqrt{2}} \quad (3)$$

Transition loss in inverters

The inverter outputs switch between ground and V_{DC} at the PWM frequency, however, the output current is filtered either by the LC filter or motor inductance. Figure 5 shows waveforms for voltage and current in a PWM switching output . Figure 5c shows a DC current with a very small ripple component. The ripple amplitude is dependent on the filter size. While this example shows a DC output, the same concept can be extended for a sine-wave output. However, the current is a sine wave with a small ripple riding on it.

Figure 5. An inverter's voltage and current waveforms with an LC filter



The instantaneous output power is $V_{AB} \times I_{LOAD}$, where V_{AB} is the average DC output, which is dependent on the duty cycles at nodes A and B. Assuming that there is no phase difference between the voltage and current, the output power for a sinusoidal output is:

$$P_{OUT} = V_{RMS} \times I_{RMS} = \frac{m_A \times V_{DC} \times I_{RMS}}{\sqrt{2}} \quad (4)$$

The transition time from 0 V to V_{DC} and vice versa of the voltage at node A is finite. The switch's ON impedance is very low when completely on, but higher during transition time. This leads to transition-switching losses. This loss occurs twice at every PWM cycle. Current through the switches during transition is same as the load current because it is filtered. Transition loss for a single event is $V_{DC} \times I_{LOAD} \times t_{RF} / 2$.

The total transition loss for a single-phase inverter is
$P_{LOSS} = 2 \times 2 \times f_{SW} \times I_{LOAD} \times V_{DC} \times t_{RF} / 2$
$= 2 \times V_{DC} \times I_{LOAD} \times t_{RF} \times f_{SW}$,
where t_{RF} is the rise/fall time of the voltage. In case of a sinusoidal current output, current through the switches is an average of the load current:

$$|I_{LOAD}| = \frac{2\sqrt{2} \times I_{RMS}}{\pi} \quad (5)$$

and the power loss is:

$$P_{LOSS} = \frac{4\sqrt{2} \times V_{DC} \times I_{RMS} \times t_{RF} \times f_{SW}}{\pi} \quad (6)$$

Ratio of the loss to output power is:

$$\frac{P_{LOSS}}{P_{OUT}} = \frac{8 \times t_{RF} \times f_{SW}}{\pi \times m_A} \quad (7)$$

Equation 6 suggests that loss is proportional to the switching frequency. An inverter with a switching frequency of 16 kHz and 200-ns rise/fall time will have a 1% transition loss, assuming $m_A = 0.8$. To reduce the transition loss, the rise/fall time has to be lower for a higher switching frequency. For example, a SiC-based inverter with a 64-kHz switching frequency needs a rise/fall time of 50 ns to keep a 1% transition loss.

Gate-drivers for Inverter

A typical drive of an IGBT-based, voltage-source inverter is shown in Figure 6. This figure shows a single-phase inverter, but it can be extended to a three-phase by adding one more leg of the bridge. The voltage at outputs OUTA or OUTB switches from V_{DC-} to V_{DC+}. The IGBT gate drives are isolated because the output-side ground of the driver is switching along with the inverter output while the input-side ground is fixed and connected to a chassis.

The potential differences between GND1 and GND2 of both gate drivers require the drivers to be isolated. The gate drivers support high-voltage isolation across the two grounds along with voltage transition rate at GND2. The gate drivers are also selected based on their isolation rating and their immunity to the transition on GND2, or common-mode transient immunity (CMTI). For example, if the DC bus is 1500 V and the transition time of OUTA is 100 ns, the immunity required by the gate driver is 15 V/ns. The immunity requirement for the driver increases if the rise/fall time is lower. A voltage-source inverter (VSI) with a higher switching frequency will have a higher CMTI requirement. A 1500-V VSI running at 64 kHz and 50-ns rise/fall time requires at least 30-V/ns CMTI. The CMTI requirement increases if the transition loss is to be lower.

The gate drivers are specified for CMTI in their datasheet. For example, the ISO5851 and ISO5852S both have a minimum CMTI of 100 kV/µs. Higher CMTI for a gate driver ensures there is no false fault or false output toggle because of the transient noise.

The component placement or board design also matters for a robustness to transient noise. The parasitic capacitance between one side of the driver to the other side of the driver should be minimized. Using a diagram from the

Figure 6: Single-phase inverter with isolated gate drivers

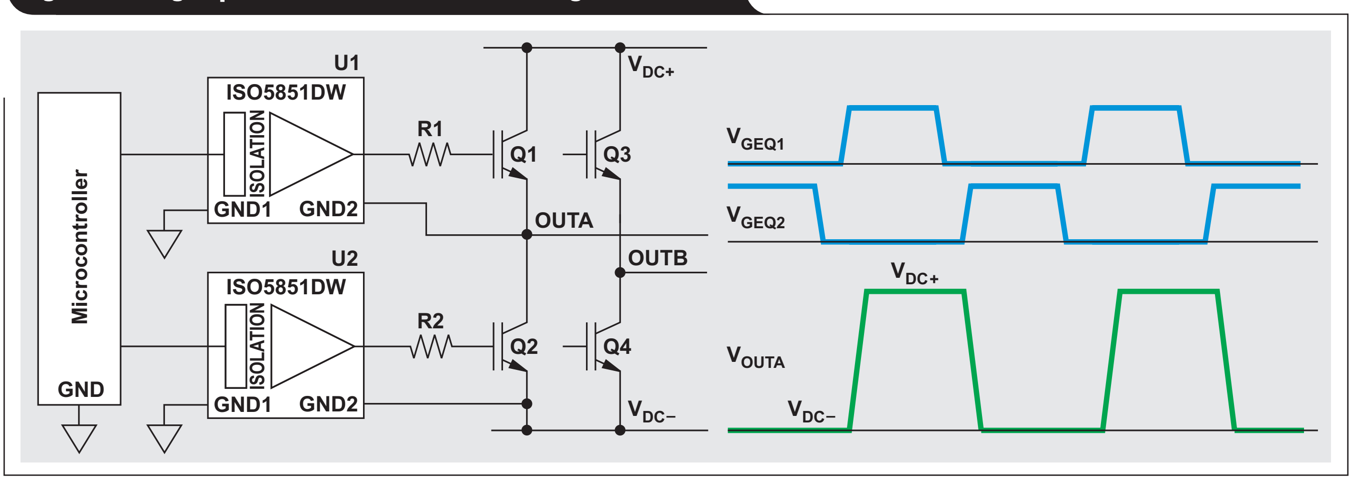
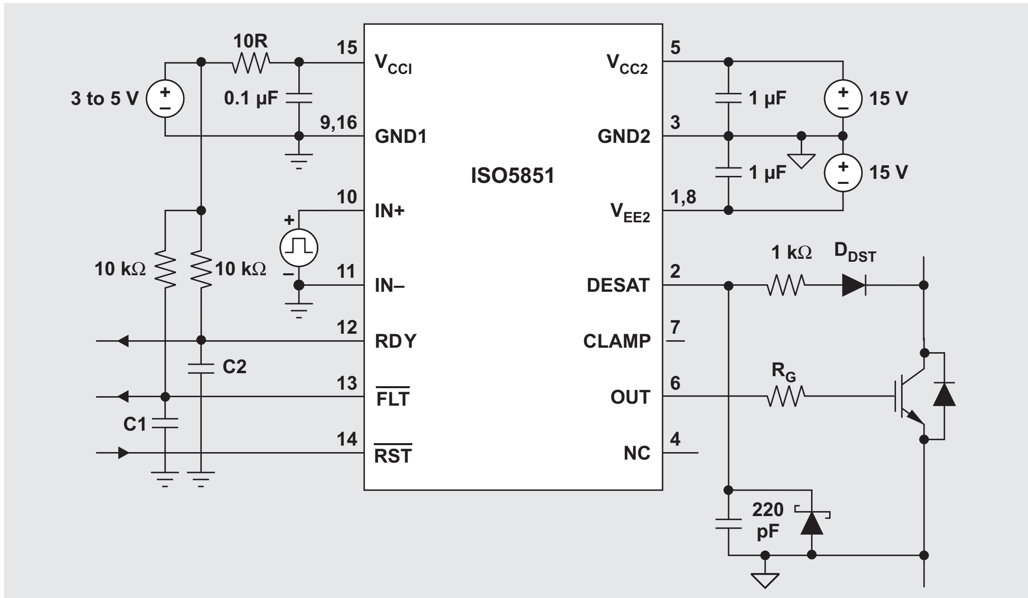


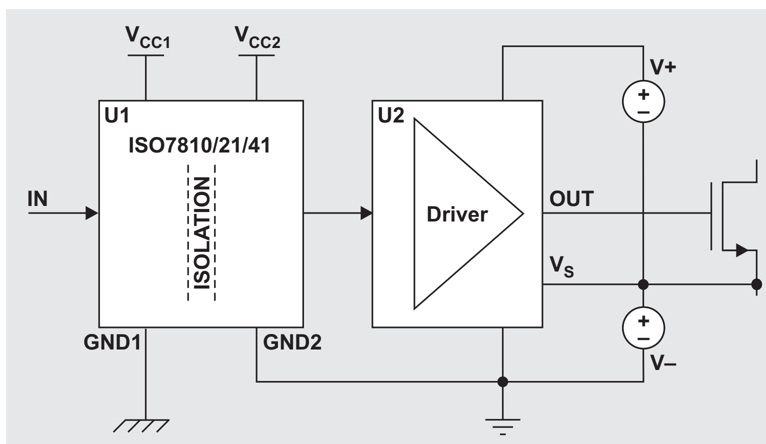
Figure 7. Typical application where C1 and C2 can be changed to adjust CMTI



ISO5851 datasheet, Figure 7 shows a typical application diagram. The Ready (RDY) and Fault (FLT) pins are pulled up by 10-kΩ resistors. These resistor values may need to be lower for noise immunity. Transient noise can generate a false fault or low under-voltage lockout (UVLO) signal. This issue can be solved by either reducing the resistor values or increasing the capacitance of C1 and C2.

Digital isolators such as the ISO7810, ISO7821 or ISO7841 also can be used in conjunction with SiC, GaN or IGBT drivers. Digital isolators provide reinforced isolation and a CMTI at a minimum of 100 kV/µs. Figure 8 shows an isolated driver solution using a digital isolator. The digital isolator can range from a single channel up to four channels, depending on the application. The digital isolator has an added benefit of low propagation delay, low skew and low jitter, which are useful in a high-frequency design.

Figure 8. Gate-driver solution using digital isolators



Conclusion

Voltage-source inverters (VSIs) with PWM topology are a good choice for a motor control because the output amplitude and frequency control have a lot of flexibility. A higher switching frequency of PWM VSIs allows for a smaller filter size. The rise/fall times should be lower with high switching frequencies to keep the transition loss lower. A gate driver with good CMTI supports faster switching speeds. Gate-driver solutions from Texas Instruments can support a CMTI minimum of 100-kV/µs.

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Related Web sites

Product information:
ISO5851, ISO5852S, ISO7810, ISO7821, ISO7841

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