A Phase-Locked Loop Filter Scheme Having Excellent Jitter Transfer Characteristics

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Hee Wong - Information Appliance Engineering

I. Introduction

A phase-locked loop (PLL) exhibits a low-pass response to its input signal. The input signal dimension is in phase angle, so it is a "radian low-pass filter" as opposed to a conventional "voltage low-pass filter." In addition, unwanted input voltage is called "noise," while unwanted phase movement is called "jitter." Since "voltage low-pass filters" use "voltage transfer function" to describe the input to output transfer characteristics, there is an equivalent "jitter transfer function" for PLL measurements.

It is worth noting that these transfer functions are simply input to output transfer characteristics. There is no differentiation between real signal and noise components. Thus, the jitter transfer function is equivalent to the PLL low-pass response.

If the PLL has a poor jitter transfer characteristic, its output may contain jitter components due to inadequate filtering effect. If the application requires cascading several of these PLLs, such as in the SONET line-timing mode [9, pp.5-22], the "jitter leak-through" will create severe jitter accumulation problems. The reason is the line-timing mode uses the recovered clock for transmission, and then the last PLL sees the accumulated jitter from all of the previous transmitters.

For clock-multiplying synthesizers, the reference clock jitter, including jitter from other sources, such as charge-pump phase detectors, will also pass through the PLL. Thus, the "jitter leak-through" will create jitter at the output of the PLL. The output jitter spectrum usually has a high frequency response similar to their filter transfer characteristics. Therefore, good jitter transfer characteristics are essential when designing PLLs.

An ideal PLL response should have a brick-wall, low-pass transfer characteristic. Within the pass-band, the gain should be unity; outside the pass-band, the gain should be zero. With this kind of transfer characteristic, the PLL should track all low frequency variations and reject all high frequency input jitters at its output.

The subject IS-PLL filter scheme approaches these ideal characteristics with a third-order filter. It has an integrator for tracking low frequency changes and a separate low-pass filter for controlling the loop stability and high-frequency attenuation. These two filter elements, the "integrator" and the "stability filter," together with other system components form an IS-PLL.

For performance comparison reasons, many plots are utilized to show the differences between classical PLLs and the IS-PLL. These plots were simulation results from a software program. A high-level common model has been developed for uniquely defining and specifying these PLL examples. The model allows a common definition and test platform for comparison.

II. The IS-PLL Circuit model

A PLL contains a phase detector (PD), a loop filter (LF) and a voltage-controlled oscillator (VCO). Perhaps the most dominating factor that affects the low-pass response of the PLL is the loop filter. There are many types of loop filter designs developed for different applications, for example, timing recovery loops, clock synthesizers, modulators, demodulators, etc& . The differences among these filters are their frequency response characteristics. A multi-order filter may be required to achieve the proper frequency response for tracking application-specific signal phase or frequency changes.

Figure 1 shows a high-level IS-PLL model. We can use it to construct many PLLs that require proportional and integral controls. The loop order has a third-order maximum. The model does not include a

differentiator, so it is not for PLLs that need derivative control.

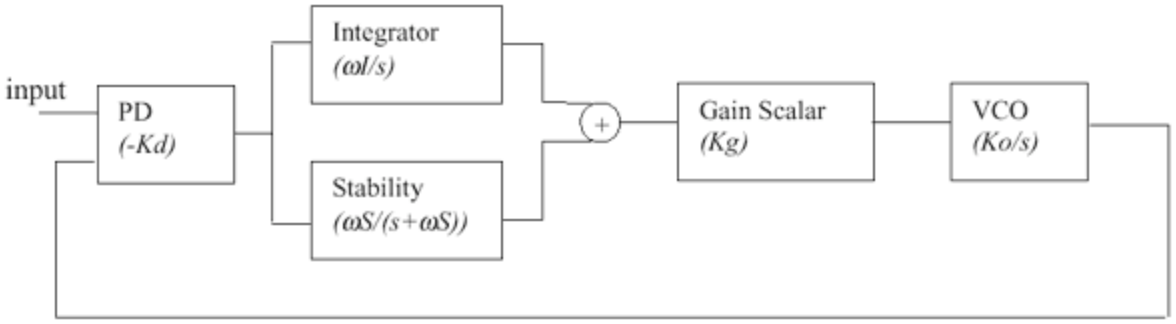

Figure 1. A High-Level IS-PLL Model

The first block in Figure 1 is the conventional phase detector (PD). For high-level simulation purposes, the transfer function of this block can be represented simply by a gain factor *Kd*. For closed-loop phase correction purpose, *Kd* is negative.

The Integrator block (I block) is the conventional integrator. The transfer function is w *I/s*, where w *I* is the integrating time constant and "*s*" is the standard Laplace operator.

The Stability block (S block) can be modeled as a passive low-pass filter having a transfer function of w *S/(s + w S)*. For the IS-PLL, this block is designed to provide a dominant pole w *S* that sets the stability of the IS-PLL.

The fourth block is simply a gain block. The transfer function *Kg* is a gain factor that includes gain elements contributed by miscellaneous blocks in a practical PLL. This quantity also includes a factor that makes the DC gain of the "S" block unity (explanation follows).

The fifth block is the voltage-controlled oscillator (VCO), which has a transfer function of *Ko/s*.

To specify a PLL uniquely for circuit simulation purposes, we need only three frequency-dependent parameters: w *K, w I* and *w S*. The values of w *I* and w *S* are defined by the filter parameters mentioned above. The value w *K* is the product of the *K* elements:

$$\omega K = Kd * Kg * Ko$$

The addition of the Gain Scalar *Kg* has two purposes:

1. To provide a function-holder for all miscellaneous gain blocks used in a practical PLL (e.g., clock pre-scalars, operational-amplifiers, etc& .)
2. To provide gain compensation when the DC gain of the physical implementation of the "S" block is not unity. For simulation purposes, forcing the DC gain of the "S" block to unity eliminates interactions among the filter parameters. The value of *Kg* is then adjusted to absorb the gain redistribution. In addition, the actual value of w *I* also needs adjustment.

For practical purposes, these three parameters are converted from angular velocity "w " to frequency "*f*" in Hz. The following equation shows the conversion relationship:

$$fX = \omega X / 2\pi$$, where *X* can be *K, I or S.*

For scale normalization and ease of parameter comparison purposes, a fourth parameter *fmul* is introduced. This parameter is simply a frequency-multiplying factor such that the actual frequencies of the PLL parameters are *fK*fmul*, *fI*fmul* and *fS*fmul*. When specifying a filter, the value of *fK* is normalized to unity and *fmul* contains a factor for scaling *fK* to its actual value. Therefore the ratios *fK/fI* and *fS/fK* can be

directly represented by the values of 1/*fI* and *fS* respectively.

Example for specifying an IS-PLL: *fK=1, fI=1/256, fS=2, fmul=1*

III. Parameters for Some Classical PLLs and the IS-PLL

The IS-PLL combines two classical PLL types, PI-PLL and S-PLL, to achieve excellent transfer characteristics. These three PLL types have the following properties:

1. PI-PLL (*fK=1, fI=1/2, fS=¥ , fmul=1*)

   Classical name: Active-lag-lead PLL, (other name: Second-order Proportional-Integral PLL)

   Description:

   The loop has an integrator for tracking low frequency changes (*fI=1/2)*.

   The loop does not use low pass filtering, although it has a proportional path for controlling the loop stability that can be modeled as a passive low-pass filter having a very high roll-off frequency (*fS=¥*). Thus, the effective gain of this block is unity for all frequencies *(i.e., If w S=¥ , then w S/(s + w S)=1*).

   When *fI*=1/2, the loop damping factor is z = *0.5 * sqrt(fK/fI) = 0.707*

2. S-PLL *(fK=1, fI=0, fS=2, fmul=1)*

   Classical name:

   Simple RC lag PLL, (other name: 1.5 order PLL)

   Description:

   The loop does not contain any Integrator (I Block) for tracking low frequency changes (*fI=0*).

   The loop uses passive low-pass filtering for controlling the loop stability (*fS=2*).

   When *fS=2*, the loop damping factor is z = *0.5 * sqrt(fS/fK) = 0.707*

3. IS-PLL *(fK=1, fI=1/256, fS=2, fmul=1)*

   Classical name:

   No classical equivalent type. (See comparisons between a classical Active-lag-lead-lag-PLL and the IS-PLL in Section *VII*)

   Description:

   The loop has an integrator for tracking low frequency changes (*fI=1/256)*.

   The loop has a passive low-pass filter for controlling the loop stability (*fS=2*).

   When *fS=2*, the loop damping factor is z = *0.5 * sqrt(fS/fK) = 0.707*

IV. The PI-PLL (Active-lag-lead PLL: fK=1, fI=1/2, fS=¥ , fmul=1)

This is probably the most common loop used in many applications. This type of loop has an ideal integrator (*fI=1/2*) for tracking low frequency changes. Since the loop has very large DC gain, the loop can track out

any changes of input phase. There is no steady-state error resulting from a step change in frequency.

The loop transfer function is given by

$$H(s) = (sfK + fKfI) / (s^2 + sfK + fKfI)$$

where

$fn^2 = fKfI$ (fn is the loop natural frequency)

$2z\,fn = fK$ (z is the damping factor)

$z = 0.5 * sqrt(fK/fI)$

The loop relies on the ratio of *fK/fI* to determine its stability. The stability is quantified by z which is referred to as the damping factor of the loop. Common values for z range from 0.707 to 20.

However, this type of PLL has the following disadvantages:

1. *Poor Jitter peaking response:*

The numerator of the transfer function contains the term "*sfK*." This term creates a response peaking near the loop s natural frequency *fn*. **Figure 2** (30kb pdf) shows this effect by decomposing the PLL output into two components: *sfK* and *fKfI*. The combined output exhibits a peak response of 2.1dB. **Figure 3** (27kb pdf) shows the time-domain phase step response which exhibits a 20% magnitude overshoot.

For some timing recovery applications where very low jitter accumulation is required, the magnitude of the peaking must be less than 0.1dB [9, pp.5-47]. Traditional methods can achieve this by setting *fI* smaller than 1/256. **Figure 4** (29kb pdf) shows the amount of jitter peaking versus different loop damping values. **Figure 5** (38kb pdf) is a close-up of Figure 4. There are eight traces with the following parameters:

fK=1, fI=1/2, fS=¥ ,	*fmul= 1.414:*	*z =0.707, f-3dB= 2.1, peak=2.09dB*
fK=1, fI=1/4, fS=¥ ,	*fmul= 2.000:*	*z =1.000, f-3dB= 2.5, peak=1.25dB*
fK=1, fI=1/8, fS=¥ ,	*fmul= 2.828:*	*z =1.414, f-3dB= 3.2, peak=0.72dB*
fK=1, fI=1/16, fS=¥ ,	*fmul= 4.000:*	*z =2.000, f-3dB= 4.2, peak=0.40dB*
fK=1, fI=1/32, fS=¥ ,	*fmul= 5.657:*	*z =2.828, f-3dB= 5.8, peak=0.22dB*
fK=1, fI=1/64, fS=¥ ,	*fmul= 8.000:*	*z =4.000, f-3dB= 8.1, peak=0.12dB*
fK=1, fI=1/128, fS=¥ ,	*fmul= 11.314:*	*z =5.657, f-3dB=11.4, peak=0.06dB*
fK=1, fI=1/256, fS=¥ ,	*fmul= 16.000:*	*z =8.000, f-3dB=16.0, peak=0.03dB*

Decreasing *fI* also increases the loop s damping factor z . High damping factor makes the loop sluggish, which affects low frequency tracking performance and acquisition speed.

2. *Poor high frequency roll-off characteristic:*

The high frequency roll-off rate is *-6dB/Octave* instead of *-12dB/Octave* (see Figure 2 & 4). This rate is similar to that of a first-order loop. Obviously, the poor roll-off rate is due to *sfK* in the transfer equation, which is created by the proportion-path within the loop filter. This term has a roll-off rate of *-6dB/Octave*, which dominates the loop response when input frequencies are higher than the natural frequency *fn* of the loop.

In PLL designs, where dominating jitter sources are from input reference signals, charge-pumps, or loop filters, then having a *-12dB/Octave* roll-off rate is appropriate for meeting a tight PLL jitter specification. On the contrary, for systems with high VCO noise, this will create adverse effects.

V. The S-PLL (Simple RC-lag PLL: fK=1, fI=0, fS=2, fmul=1)

This is the simplest way to build a second-order PLL. Unfortunately, this method does not include an integrator to track low frequency changes (*fI=0,*) so it cannot satisfy most applications needs. Although it is not widely used, it is still found in applications where this special tracking characteristic becomes an advantage (e.g., modulator and demodulator circuits).

The loop transfer function is given by

$$H(s) = fKfS / (s^2 + sfS + fKfS)$$

where

$fn^2 \circ fKfS$ (*fn is the loop natural frequency)*

$2z\, fn \circ fS$ (*z is the damping factor)*

$\backslash z = 0.5 * sqrt(fS/fK)$

The loop relies on the ratio of *fS/fK* to determine the loop stability. The stability is quantified by z which is referred to as the damping factor of the loop. Common values for *z* range from 0.707 to 20.

However, this type of PLL has the following disadvantage:

1. *Poor low frequency tracking characteristic:*

Since the DC gain of the loop is finite (lack of an integrator, *fI=0*), it creates steady-state phase tracking errors and exhibits poor low frequency tracking performance. Furthermore, it cannot compensate for frequency offsets due to device parameter variations during volume manufacturing. Due to these impairments, this class of PLLs is not widely used in modern large-scale integrated circuits.

Gardner [14, pp. 17] indicated that the denominator of the transfer function is of second degree, so the loop can be considered as a second-order loop; even the loop has no integrator. However, he also mentioned that there are restrictions when selecting parameters for desired loop responses. The loop will be badly under-damped and transient response will be poor when there is a large DC gain and small bandwidth utilized in the loop.

VI. The IS-PLL (fK=1, fI=1/256, fS=2, fmul=1)

The proposed IS-PLL represents a new class of PLLs that utilizes a composite filter which comprises a passive low-pass filter $w\ S/(s + w\ S)$ and an ideal integrator $w\ I/s$.

The loop transfer function is given by a third order equation:

$$H(s) = (sfK \{ fS+fI \} + fKfSfI) / (s^3 + s^2fS + sfK \{ fS+fI \} + fKfSfI)$$

If *fS » fI*, then *{ fS+fI }* » fS, so the transfer function becomes

$$H(s) » (sfK + fKfI) / (s^3/fS + s^2 + sfK + fKfI)$$

For input frequencies *«* fS, the transfer function is identical to that of a PI-PLL:

$$H(s) » (sfK + fKfI) / (s^2 + sfK + fKfI)$$

For input frequencies *»* fI, the transfer function is identical to that of a S-PLL:

$$H(s) » fKfS / (s^2 + sfS + fKfS)$$

Since there are two transfer functions for two different frequency bands, there are two natural frequencies and two damping factors in the system:

For input frequencies « fS : $fn\_low^2 = fKfl$, $z\_low = 0.5 * sqrt(fK/fl)$

For input frequencies » fl : $fn\_high^2 = fKfS$, $z\_high = 0.5 * sqrt(fS/fK)$

For jitter peaking and high frequency roll-off reasons, the ratio of *fK/fl (typical range: 32 to 512)* has a much larger value than that of *fS/fK (typical range: 2 to 5),* so the loop is more sensitive to *fn_high* and *z _high*. Therefore, *fn_high* and *z _high* are the primary loop parameters and *fn_low* and *z _low* are the secondary loop parameters. It is also valid to say that the passive low-pass filter w *S/(s + w S)* is the primary loop filter while the integrator w *I/s* is the secondary loop filter.

VI.1 Criteria for Selecting the Secondary Low Frequency Parameter (fK/fl) for the IS-PLL:

The selection of this parameter is much simpler than the high frequency counterpart *fS/fK* (Section *VI.2*). The value of *fK/fl* can range from 32 to 512 for obtaining different levels of jitter peaking response (from 0.22dB to 0.03dB, z =2.828 to 8.0 respectively, see Section *IV*). Although this tweaking technique cannot eliminate the peaking effect totally, it is proven to be the most practical solution [1-7].

Nevertheless, there are disadvantages using this technique. As mentioned in Section *IV*, the first disadvantage is the degradation of high frequency roll-off rate. Fortunately, this is no longer a design concern because the primary filter w *S/(s + w S*) dominates the high-frequency roll-off rate. Section *VI.2* provides more insight to this topic.

The second disadvantage is the degradation of the loop s low-frequency tracking performance. In effect, the high ratio of *fK/fl* reduces the loop s integrating capability causing the loop s tracking rate to slow down. It is appropriate to inspect the phase error term (q *e* = Input phase Output phase) to ensure an adequate tracking rate when the input reference signal contains modulation. Modifying the value of *fK/fl* can fix this problem. However, it is unnecessary in most designs.

The third disadvantage is the increase in the loop s acquisition time. But still, this is not a design concern since most modern loops have "multi-speed acquisition circuits" to alleviate the performance conflicts.

In summary, although there are several minor low-frequency design considerations, the selection of this parameter is still simple. In any respect, there is insignificant interaction between the secondary and the primary filters because of the large distance between the two frequency poles (at least 32 x 2 = 64 times; more than 200 times in most applications).

VI.2 Criteria for Selecting the Primary High Frequency Parameter (fS/fK) for the IS-PLL:

The selection criteria are based on the classical "All-pole low-pass filter" design topology. A typical second-order low-pass transfer equation is given by:

$H(s) = freq^2 / (s^2 + sfreq / Q\_factor + freq^2)$

This equation has the same form as the equation for IS-PLL when input frequencies » *fl*. Using the common PLL modeling scheme, we can specify some classical filters:

a. A second-order Butterworth low-pass filter (maximally flat amplitude response):

fK=1, fl=0, fS=2, fmul=0.707: z =0.707, f-3dB=1.0

b. A second-order Bessel low-pass filter (maximally flat delay response):

fK=1, fl=0, fS=3, fmul=0.735: z =0.866, f-3dB=1.0

These filter responses are monotonic and exhibit no jitter peaking effect. If the value of *fS* is set less than 2, then the filter response has peaking and the filter class is of the Chebyshev type. If the value of *fS* is higher than 3, then the filter response is still monotonic and exhibits no jitter peaking effect. However, when the value of *fS* is very large or close to infinity, the filter loses all of its second-order effect. Thus, the filter becomes a first-order filter.

In general, these filters have a roll-off rate of *-12dB/Octave*. **Figure 6** (34kb pdf) shows a series of curves, which have the values of *fS* ranging from 2 to ¥ *(simulation uses* 1e50 instead of ¥ *)*, i.e.,

fK=1, fl=0, fS=2,	*fmul=0.707:*	*z =0.707,*	*f-3dB=1.0*
fK=1, fl=0, fS=3,	*fmul=0.735:*	*z =0.866,*	*f-3dB=1.0*
fK=1, fl=0, fS=4,	*fmul=0.778:*	*z =1.000,*	*f-3dB=1.0*
fK=1, fl=0, fS=5,	*fmul=0.814:*	*z =1.118,*	*f-3dB=1.0*
fK=1, fl=0, fS=¥ ,	*fmul=1.000:*	*z =¥ ,*	*f-3dB=1.0*

When *fS* has a value higher than 5, the high frequency attenuation characteristic degrades more rapidly. For systems where minimum peak-to-peak phase jitter is of importance, such as in a timing recovery loop, then the value of *fS* should be less than 5. This is based on the assumption that the output jitter is dominated by components less than 5 (in Hz, note that the *f-3dB* frequency of the filter is normalized to 1 Hz). When frequencies are higher than 5, attenuation is high (more than 20dB). As a result, these frequency components do not contribute much to the total jitter output.

The following provides an attenuation comparison chart on these filters (*fS=2,3,4,5 and ¥)*. The frequency data points range from 1 to 5Hz, and the attenuation numbers are in dB.

frequency **(Hz)**	**fS = 2**	**3**	**4**	**5**	**¥**
1	-3.0	-3.0	-3.0	-3.0	-3.0
2	-12.3	-9.8	-8.5	-7.8	-7.0
3	-19.1	-15.7	-13.5	-12.2	-9.9
4	-24.1	-20.3	-17.7	-15.9	-12.3
5	-28.0	-24.0	-21.1	19.1	-14.1

When *frequency=2Hz* and *fS=2,* the attenuation is *-12.3dB*. The attenuation drops to *-7.8dB* when *fS=5,* while it is almost equivalent to the *-7.0dB* attenuation when *fS=¥* . Note that as *fS* approaches ¥ , the filter behaves like a first-order filter. Hence, in order to achieve high rejection at high frequencies,

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