Application Report

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AN-1727 Calibrating the ADC08xxxx Family of Ultra High-Speed Converters

ABSTRACT

The ADC08xxxx family of giga-sample ADCs (such as the ADC08D1500) incorporates sophisticated self-calibration circuitry. This capability is an important part of this device's impressive performance over a wide temperature range. This application report attempts to give the system designer a comprehensive description of how to make use of this feature.

Contents

1 Introduction

The ADC08xxxx family of giga-sample ADCs (such as the ADC08D1500) incorporates sophisticated self-calibration circuitry. This capability is an important part of this device's impressive performance over a wide temperature range. This application report attempts to give the system designer a comprehensive description of how to make use of this feature. The device datasheet contains specific details of various aspects of self-calibration and the user should refer to the datasheet also.

2 The Self-Calibration Scheme

Since calibration is essential to the stated performance, the device performs self-calibration upon each power-up. In addition, the device allows the user to manually command the device to perform self-calibration as required. Typically this would be done when the system temperature has changed beyond a threshold that system design has established. Since ultimately it is the device's own temperature that affects its performance, an on-chip diode is made available to the user which can be connected to an external temp-sensor device and thus device temperature can be monitored. Texas Instruments recommends the LM95221 (or similar) temp-sensor for this purpose.

Whether upon power-up or upon command, the calibration procedure takes roughly 1–2 msec to complete depending upon the CLK frequency and the specific device (refer to the device datasheet for this and all other parameters mentioned in this application report). In addition, at power-up only, the device inserts a delay before starting the self-calibration process. This delay is user-selectable to be relatively short (tens of milliseconds) or relatively long (few seconds). The purpose of this delay is to allow the power-supply and other variables to stabilize. Note that the longer delay is not available when the device is configured for Extended Control mode of operation (that is, configured through the serial interface). Also note that the device's delay counters can only begin after the clock input is valid.

The CalRun pin always indicates whether the device is in self-calibration mode or operating normally.

3 Performing Self-Calibration

First thing that should be recognized is that self-calibration is part and parcel of the “normal” operation of the device. As such, the device's operating conditions should be as stable and as close to “normal” system conditions as possible during calibration. This means that the power supply, temperature and all inputs must be within the operating conditions stated in the “Operating Ratings” section of the datasheet and stable. Then, for greater calibration accuracy, the operating conditions should be as close to their operational state as possible.

In order to allow the conditions to stabilize, a certain amount of time delay would be necessary. The system engineer must decide what this time delay is for his system — which may vary from about 1–2 seconds to tens of seconds. As mentioned in Section 2, the device has built-in calibration delay capability. If longer delay is required then the CAL input pin can be used to further delay the start of the calibration cycle. The user does this by holding the CAL pin high during power-up and keeping it high for as long a delay as desired. The device will wait until the CAL pin is cycled low and then high again before initiating the power-up calibration cycle. The CAL input “low-then-high cycle” timing requirements can be found in the AC Electrical Characteristics table in the datasheet. Other than inhibiting the calibration from occurring, this scheme does not interfere with the rest of the device's behavior. Although delayed in this manner with the CAL input, this should still be considered the *power-up calibration that must occur before proper performance can be expected*.

In addition to waiting for the environment conditions to be stable (supply and temperature), the device's other operational conditions have to be stable as well to obtain the most accurate calibration. Here are some specific requirements:

- The clock input must be stable (this includes NOT performing DCLK_RST);
- The analog input must be within its valid* range, but the frequency is not important — including DC;
- The control/configuration settings must not be disturbed while calibration is under way.
- The device must be in normal mode (not DES mode) on the ADC08D500/1000/1500 and ADC08500/1000/1500 family of devices. This restriction does not exist on the newer ADC08D1020/1520 and ADC083000/B3000 devices;
- The control registers must not be accessed, though the SCLK may be active;

- The device should not be in power-down mode when starting calibration, nor enter power-down while calibration is underway.
- On the ADC083000 and ADC08B3000 only, if Clock Phase Adjust feature is being used, it is imperative that the RTD bit should be kept in the set position after enabling this feature so that DCLK will keep running during calibration.

* “valid” means that the input is within the range specified in the Operating Ratings section.

4 Device Behavior During Self-Calibration

In addition to the obvious interruption to the signal processing path, the device also exhibits few other effects during the calibration cycle.

1. The digital outputs are disabled.
2. The DCLK output is also disabled on certain devices of this family.

The DCLK output of the device is generally intended for data capture purposes only. The fact that it is interrupted, means that the ASIC/FPGA device should not rely on it as a clock signal for its logic beyond the capturing logic. However, for those applications where it is essential to use the DCLK signal as a general purpose clock, the newer devices of this family give the user the control to keep the DCLK running during calibration. The cost of this is that the analog input termination resistor (Rterm) is not calibrated if the DCLK is kept active — causing the Rterm value to be slightly less accurate. Thus, this option should not be used during power-up calibration, but only for subsequent on-command calibration cycles.

On the ADC08D1020/1520 and ADC083000/B3000 devices the RTD (Resistor Trim Disable) bit in the Extended Configuration Register controls whether the DCLK is allowed to stop during calibration or not. The default state of this bit, upon power-up, is such that DCLK will be stopped and Rterm will be trimmed during calibration. At the time of power-up calibration, the user must leave this bit in its default state and expect the DCLK to stop during calibration. Thereafter the user may set this bit in order to keep the DCLK running during subsequent on-command calibration cycles. It must be stressed that at least one calibration must be performed with the RTD bit disabled so that the input termination resistors are trimmed at least once.

The act of calibration, in of itself does not require the control registers to be rewritten or any values to be adjusted. Also, if the system design is using multiple devices and they have been synchronized using DCLK_RST, the calibration cycle does not require the synchronization to be performed again.

5 Performance Effects

The devices' performance is specified in the datasheet under the condition that the device is correctly calibrated under the operating conditions at the time of measurement. As with any electronic circuitry, the device exhibits some amount of performance degradation as environmental conditions change after calibration. The system parameter that usually affects performance after calibration the most is temperature. On-command self-calibration should be performed when temperature change exceeds a certain threshold. This threshold should be determined by the system designer during the design process. *Texas Instruments does not specify the amount of device's uncalibrated performance degradation with temperature variance*. However, the following observations, from limited data, may be useful to the user.

1. The ENOB performance of the device has been seen to degrade by 0.35 bits over a temperature range of 55°C (from +45°C to +100°C die temperature).
2. Gain error of 2% across an 80°C temperature range (from +20°C to +105°C die temperature) has been seen.
3. If the DCLK is enabled by the user to run during calibration and the Rterm is not calibrated after the required power-up calibration, the Rterm's value due to temperature effects alone is expected to vary by a total of 1% over a 120°C temperature range (from 0°C to +120°C die temperature).

Based on this set of limited data, a reasonable temperature variance threshold to trigger a self-calibration cycle could be in the 20°C to 30°C maximum range.

6 Conclusion

Self-calibration is a powerful feature of the giga-sample family of 8-bit ADCs. The user is provided a great deal of flexibility — with which these devices can provide reliable performance over a wide range of temperature.

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