DS90C387,DS90C387A,DS90C387R,DS90CF388, DS90CF388A

LVDS goes the distance!

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LVDS goes the distance!

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Abstract

LVDS is the indisputable de-facto standard for notebook digital displays today. LDI (LVDS Display Interface) extends this technology to desktop applications, supporting high-resolution panels (QXGA), and enhances the cable drive capability to provide a robust, long, low cost interface. This paper discusses the performance of the new DS90C387/DS90CF388 LDI chipset.

Introduction

LDI (LVDS Display Interface) is *the* optimal interface for the high-resolution flat panel monitor applications. The chipset employs LVDS, (Low Voltage Differential Signaling) as its physical layer. Products are based on the de-facto LVDS standard interface widely used in notebook displays. This allows for backward compatibility with today's notebook displays, and enables a notebook to interface directly to a flat panel monitor through a desktop docking station. LDI includes new features and architecture improvements to drive long, low-cost cables required by monitor applications.
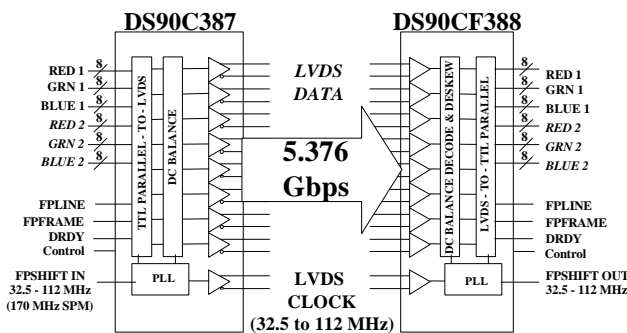
LDI Block Diagram

The LDI chipset from National provides a dual-pixel interface between the graphics controller (GUI/VGA) and the panel. The standard interface is 9 pairs wide (8 for data and one for clock) as shown in figure 1. This was chosen to provide the **best** balance between timing margins / EMI / and required bandwidth. Control signals are passed across the interface during blanking intervals. With the 7:1 serialization and the dual-pixel interface, line speed is kept under 1Gbps for optimal data recovery **and** long cable drive. LDI supports cables 5-10 meters in length at maximum thruput. It can drive longer cables at lower rates too. With the dual-pixel architecture and a 112MHz clock rate an effective bandwith of 224MHz is obtained that is sending data at **5.38Gbps**. LDI has three major enhancements over FPD-Link to extend the cable drive and to enhance signal quality. These are: pre-emphasis, DC balancing, and cable deskew. Each are discussed in detail below.
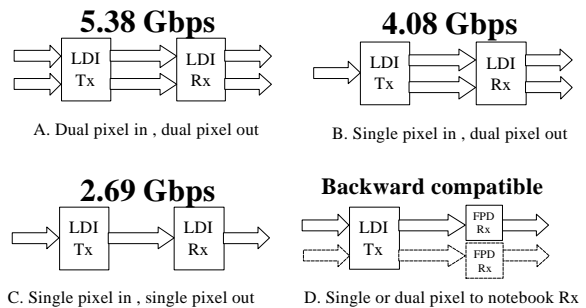

Figure 2

Versatile LDI Configurations

The transmitter (DS90C387) can support a 24-bit wide RGB interface from the graphics controller and performs the single-pixel to dual-pixel conversion. In this mode data can be clocked into the transmitter at a maximum pixel clock frequency of **170MHz** (see figure 2B). The transmitter can also

Figure 1

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support a 48-bit wide dual-pixel RGB interface from the graphics controller. In dual-pixel mode, 48 bit wide data can be clocked into the transmitter at a maximum pixel clock frequency of 112MHz (see figure 2A).

The LDI chipset also supports two other unique modes of operation as shown in figures 2C and 2D above. The first is for a single-pixel application. Twenty-four RGB data bits can be clocked to the transmitter and serialized across 4 data pairs to the receiver. Maximum clock rate for this mode is 112MHz. This configuration is useful for lower resolution monitors (XGA-SXGA) where power consumption and cable size may be of a concern.

The fourth mode provides backward compatibility to FPD-Link Receivers. Note that the LDI TX provides a second optional clock output for this application. This allows for connectivity with existing panels that are available today which use a dual-pixel FPD-Link interface. This has been demostrated in a 20 meter cable application with pre-emphasis enhancement alone.
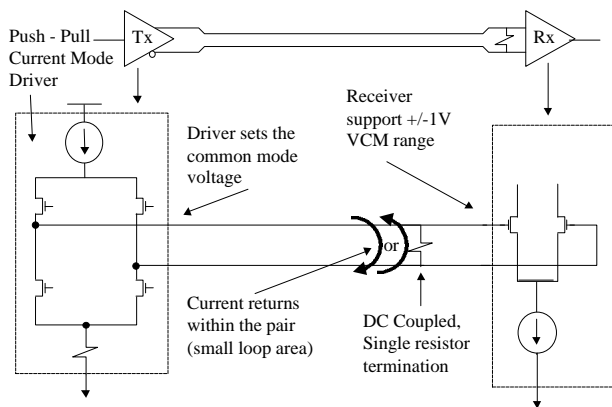

Figure 3

LVDS Physical Layer

The LVDS physical layer is shown above in figure 3. The driver is a current mode driver, that sources and sinks current. This creates equal and opposite current flow in the twisted pair interconnect (odd mode transmission) which helps to minimize emissions. The resulting ring antenna is also very small in area, thus reducing EMI and minimizing the number of ground connections required. A dedicated drain wire per pair is also not required, simplifying the cable construction and lowering cost. A simple, single across-pair termination resistor is all that is required at the receiver end. No pull-up resistors, bias resistors, or AC coupling capacitors are required for LVDS. The receiver is very noise tolerant and can reject common mode noise up to +/-1V in magnitude. It features a sensitivity of less than 100mV, and robust ESD tolerance. A 20% difference in power supply potential can be tolerated between the transmitter and the receiver with LVDS! All in all, LVDS provides a strong physical layer foundation for FPD-Link and LDI.
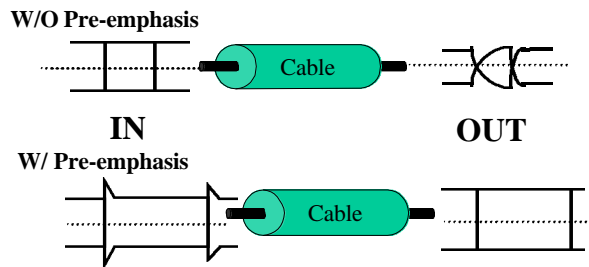

Figure 4

Pre-emphasis reduces cable loading

LDI uses a new pre-emphasis feature to counteract the adverse low pass effects of the long cable at the start of the cable. During transitions, additional dynamic current is supplied to 'overdrive' the signal. This compensates for the edge rate attenuation that occurs at the far-end of the cable. The resulting signal has a sharp transition edge and a wide open eye pattern appears at the receiver's input. This high quality signal is easily sampled by the receiver's strobes. The wide open eye pattern is obtained without the need for any "*special*" encoding that just burns up bandwidth and reduces bit time. With LDI, signal quality is improved with pre-emhasis which enhances the edge rate with out reducing the information bandwidth of the line. This provides a more efficient bus. Pre-emphasis is performed by the LDI transmitter, allowing the feature to be used for improved cable drive of longer cables between the LDI transmitter and the FPD-Link receiver. This application takes full advantage of backward compatibility with existing panels.
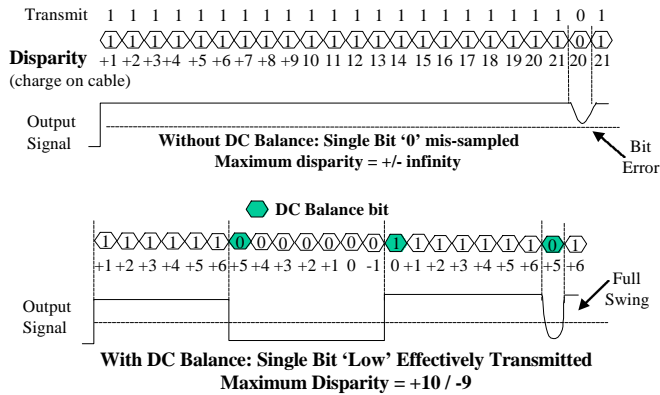
Figure 5

Simple DC Balancing reduces ISI distortion

DC balance is provided with an efficient, low-overhead scheme that limits the charge disparity on the interconnect and maintains a 'balance' on the cable. A simple representation of this is shown in figure 5. Again countering the effects of the cable loading and inter-symbol interference (ISI), this time by minimizing a charge build-up due to repetitive signal transmissions (such as a long stream of 0's). Such a scheme allows single bit transitions – a single '1' amid a stream of '0's' – to be received correctly at the end of a long cable. The overhead for DC balancing is low. Only 1 bit per 7 bit serialized word is used for this purpose per line. This makes LDI a low overhead bus at 86% efficiency (6 information bit every 7 bits).

Skew – there are two

Skew across the interconnect is yet another concern with long cable data transmission applications. The more controlled (minimized) the skew, the more expensive the cable. Since cost is typically a factor in system design, a tolerance for cable skew is required. The LDI receiver compensates for this interconnect skew allowing standard cables (standard twisted pair with single overall shield) to be used in typical desktop applications. The receiver self-calibrates for skew between the clock and each data channel. Skew may be a product of unequal electrical lengths between interconnect pairs (cables and/or PCB traces) due to twisting factors and or pair placement in the cable assembly. This deskew calibration is independent for each channel to guarantee that data from each pair is sampled with the greatest accuracy. During the deskew operation, which is done during blanking, the switching frequency on the data pairs is minimized. Data pairs toggle at the clock rate – transitions are not MAXIMIZED during blanking. The entire deskew operation is accomplished in 4 clock cycles, allowing the chipset to be used in "Reduced Blanking" applications. EMI is also minimized due to the low toggle rate.

Intra-pair skew (skew between the true and complement wires of a differential pair) is also of concern for differential transmission. Deskew techniques do not address this type of skew, so the inherent tolerance of the receiver's input is critical. An LDI receiver can tolerate >300ps of intra-pair skew, enabling the use of a cost effective cable solution. A well controlled and monitored cable assembly operation typically keeps this parameter in check. LDI intra-pair skew limit is not specified as a percentage (ie 10%) of a bit time.
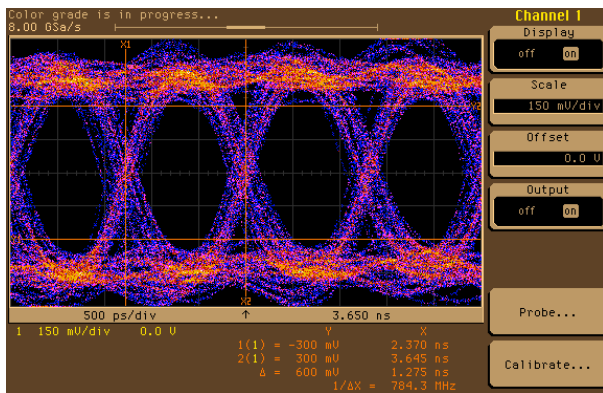

Figure 6

5.38Gbps / 5meter EYE Pattern

The eye pattern shown in figure 6 shows a LVDS data bit time of 1.28ns. Pseudo random data (PRBS) is being driven down 5 meters of twisted pair cable. Bit times are equal, jitter is low, and the data is recovered by the receiver error free. ISI and cable loading effects are kept in check with the pre-emphasis transmitter feature and also the DC balancing of the data.

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Bench Marks / BERT

LDI has been evaluated with a 48-bit wide bit error rate tester (TEK MB100s). Testing has been over extreme conditions for many different high-resolution application configurations. Zero bit errors were detected in this testing. This includes the following benchmark tests:

Data Rate	Clock Rate	Cable	Errors
5.38Gbps	112MHz (224)	5m	**0**
3.84 Gbps	80MHz (160)	10m	**0**
2.69 Gbps	56MHz (112)	10m	**0**

In all cases, the LDI links have proven to be error free. This testing was conducted with all 48 inputs switching, and a PRBS pattern which is random between inputs. This creates a worse case test as internal noise on the chip die is maximized.

LDI has been deployed in the SGI 1600SW Desktop Monitor (SXGAW) and is also deployed in several UXGA applications in the pre-production phase.

Conclusions

LDI delivers the bandwidth for today's (SXGA) and tomorrow's (UXGA/HDTV/QXGA) high-resolution display applications. It utilizes LVDS, an open industry standard, as its physical layer to deliver Gigabits @ milliwatts across long low cost cables. It provides enhancements over the standard FPD-Link interface in the area of long cable drive with the inclusion of three new features to extend its' reach. This includes transmitter pre-emphasis, DC balancing of the data, and also a cable deskew feature. It also provides a compatibility path to the de-facto notebook digital interface (FPD-Link) without the need for adapters or dongles!

References

1. DS90C387 / DS90CF388 Datasheet, National Semiconductor Corp. http://www.national.com/pf/DS/DS90C387.html

2. Open LVDS Display Interface (Open LDI), Draft Specification, V0.9, February 1999, National Semiconductor Corp. http://www.national.com/appinfo/fpd/

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