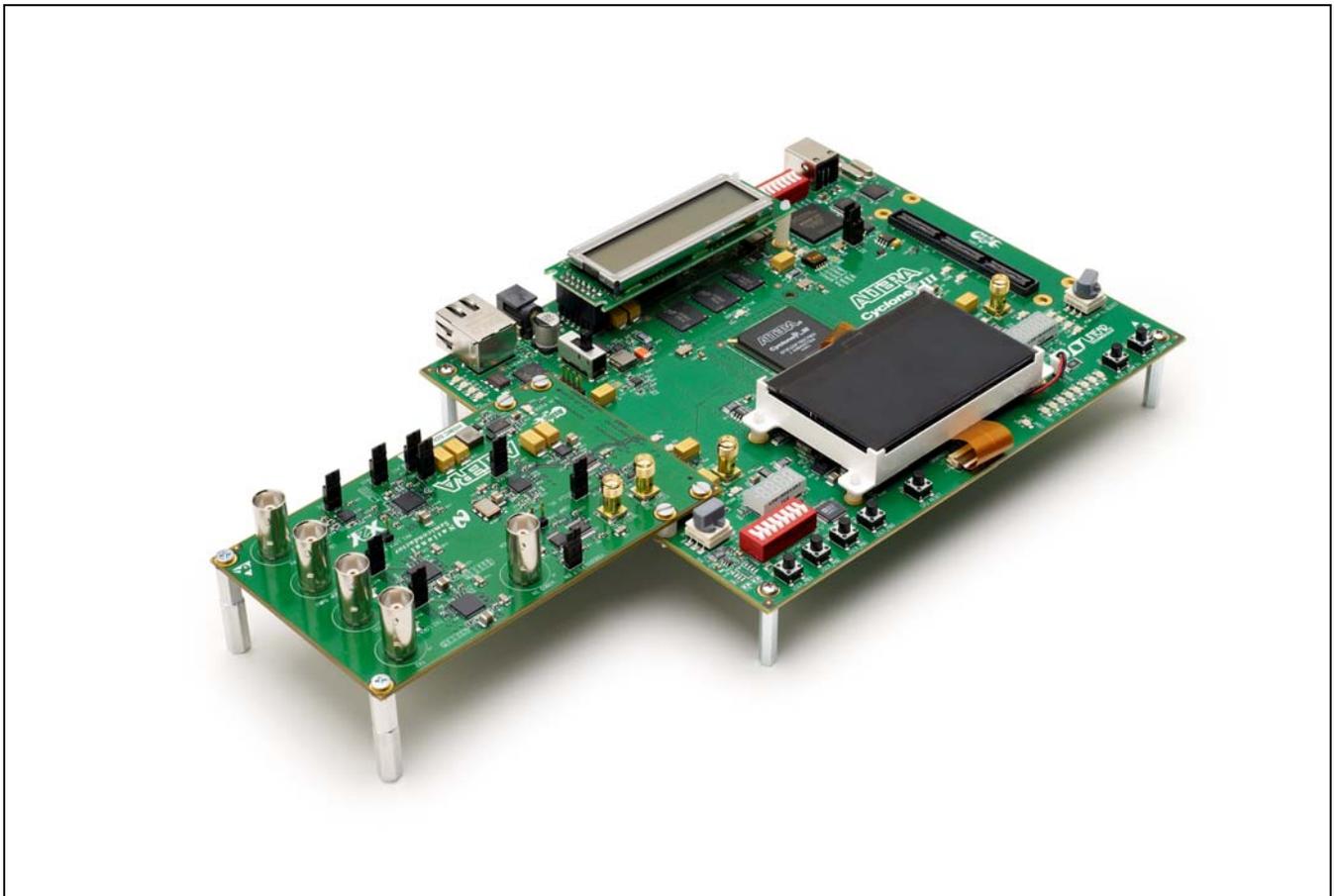


User Guide: SDALTEVK HSMC SDI ADAPTER BOARD

9-Jul-09

Version 0.06

SDI Development Kit using National Semiconductor's LMH0340 serializer and LMH0341 deserializer



1....Overview	3
2....Evaluation Kit (SDALTEVK) Contents	3
3....Hardware Setup	5
3.1 CYCLONE III DEVELOPMENT BOARD (MAIN BOARD) DESCRIPTION.....	6
3.2 SDALTEVK BOARD DESCRIPTION.....	8
4....Software Setup	9
4.1 INSTALLATION.....	9
4.2 STARTUP	10
5....Evaluating Hardware	13
5.1 TEST SETUPS.....	13
5.1.1 <i>Standalone Video Generator Tests</i>	13
5.1.2 <i>Genlock Tests</i>	14
5.1.3 <i>Video Pass-through Tests</i>	15
5.2 TERMINAL BASED SD/HD/3G SDI EVALUATION.....	15
5.2.1 <i>Standalone Mode</i>	16
5.2.2 <i>Pass-through Mode</i>	17
5.2.3 <i>Genlocked Mode</i>	Error! Bookmark not defined.
5.3 PUSH BUTTON BASED SD/HD/3G SDI EVALUATION	19
5.3.1 <i>Push Button Main Menu</i>	19
5.3.2 <i>System Mode</i>	20
5.3.3 <i>Datapath Menu</i>	20
5.3.4 <i>Video Format Menu</i>	20
5.3.5 <i>Frequency Menu</i>	21
5.4 FPGA REGISTER MAP.....	21
5.4.1 <i>Miscellaneous Registers:</i>	22
5.4.2 <i>Reset Registers</i>	22
5.4.3 <i>Rx Video Registers</i>	22
5.4.4 <i>Datapath Registers</i>	24
5.4.5 <i>Clocking</i>	26
5.4.6 <i>Video Timing</i>	26
5.5 SUPPORTED TEST PATTERNS.....	29
6....Documentation	30
7....Schematics, BOMs, and Data Sheets	30
8....Reference FPGA IP	30
9....Up to Date Information	30
10 ..Part Numbers	30

1 Overview

The SDALTEVK enables rapid evaluation of the LMH0340/0341 serializer and deserializer in Serial Digital Interface (SDI) applications. Other National devices also highlighted on this board are shown in Table 1.

Table 1) National Semiconductor Devices on the SDALTEVK

Device	Quantity	Description	Function	Reference Designator
LMH0340	2	SD, HD and 3G SDI serializer + cable driver	SDI Serializer	U1, U6
LMH0341	1	SD, HD and 3G SDI deserializer	SDI Deserializer	U11
LMH0344	1	SD, HD and 3G cable equalizer	SDI Equalizer	U13
LMH1981	1	Multi-Format Video Sync Separator	Optional Clock Source	U3
LMH1982	1	Multi-Rate Video Clock Generator with Genlock	Optional Clock Source	U9
DS90CP22	1	2x2 LVDS Cross Point Switch	Clock Multiplexer	U7
DS90LV028 A	1	Dual LVDS to 3V CMOS Receiver	Optional Clock Output	U5
DS90LV031 A	1	Quad 3V CMOS to LVDS Line Driver	Optional Clock Source	U2
LP3878-ADJ	1	Micropower 800mA Low Noise Adjustable Voltage Regulator	2.5V Regulator	U10
LM20242	1	2A PowerWise™ Adjustable Frequency Synchronous Buck Regulator	3.3V Regulator	U12

Examples of firmware are provided for the Standard Definition SMPTE 259M (SD-SDI) interface, the High Definition SMPTE 292M (HD-SDI) interface, and the 3G SMPTE 424M (3G-SDI) interface. The video standards supported by the example firmware are shown in Table 2.

Table 2) Video Standards Supported by Firmware

Rate	Video Standard
SD	NTSC, PAL
HD	720p50, 720p59, 720p60, 1080s23.98, 1080s24, 1080i50, 1080i59, 1080i60, 1080p29.97, 1080p30
3G	1080p50, 1080p59.9, 1080p60

A user interface allows for managing the FPGA firmware functions and the LMH0340/0341/1982 device registers.

2 Evaluation Kit (SDALTEVK) Contents

The SDALTEVK contains the following parts:

- SDALTEVK HSMC SDI ADAPTER Board
- Screws, standoffs and spacers for mounting the EVK to the Cyclone III Development Board

The following is required to complete the evaluation kit:

- Altera Cyclone III Development Kit Altera Part Number: [DK-DEV-3C120N](#)
- National Semiconductor SDI compiled .sof file from: <http://www.national.com/sdaltevk>
 - Triple Rate Standalone mode with multiple format selection
 - Triple Rate pass-thru mode with format detection
 - Pattern selection
 - Gen-Lock function supported
 - Register programming supported
- Altera compiled .sof file from: ftp://ftp.altera.com/outgoing/National_SerDes/an535_1_0.zip
 - Triple Rate pass-thru mode
- Quartus II 8.0 or newer <http://www.altera.com/products/>
- Nios II EDS 8.0 <http://www.altera.com/products/>
- Cygwin from <http://www.cygwin.com/>
- SDI cables
- PC

Hardware Setup

The SDALTEVK printed circuit board is designed to interface with the HSMC connector on the Cyclone III Development Boards. Power, control bus, and LVDS bus signals are supplied to the daughter board through the HSMC connector. The Cyclone III FPGA provides the SD/HD/3G SDI and general purpose stacks as well as the control interface to a PC through a USB cable. This evaluation system allows inexpensive FPGAs to deliver up to 3 Gbps on a coax cable.

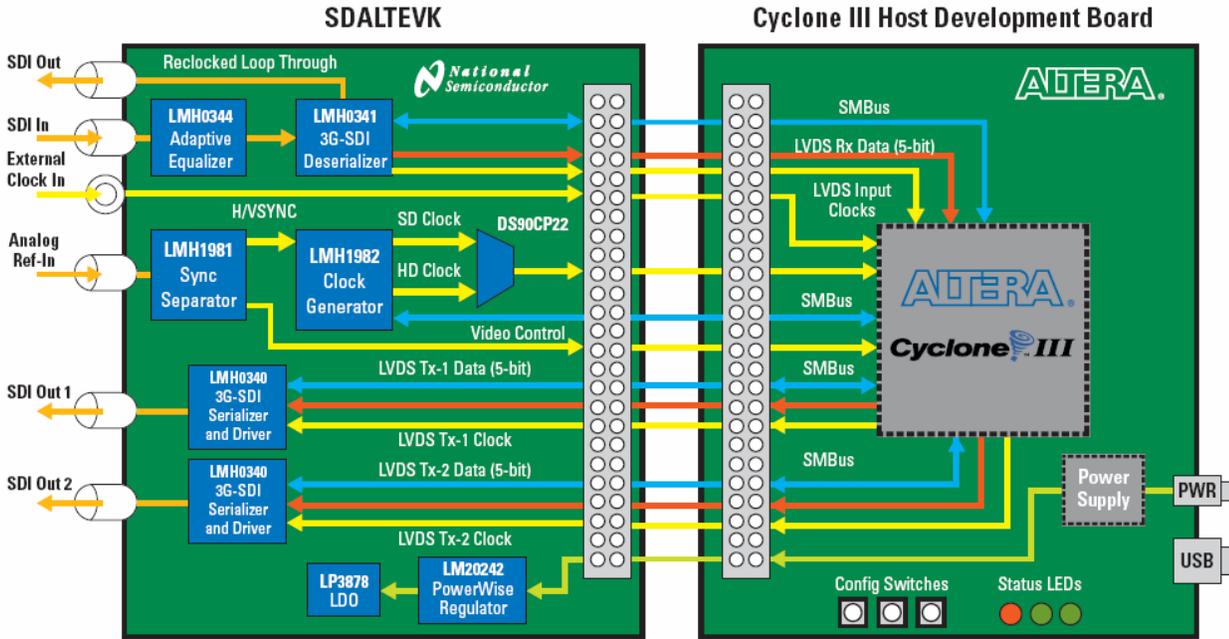


Figure 1 Evaluation Kit Block Diagram

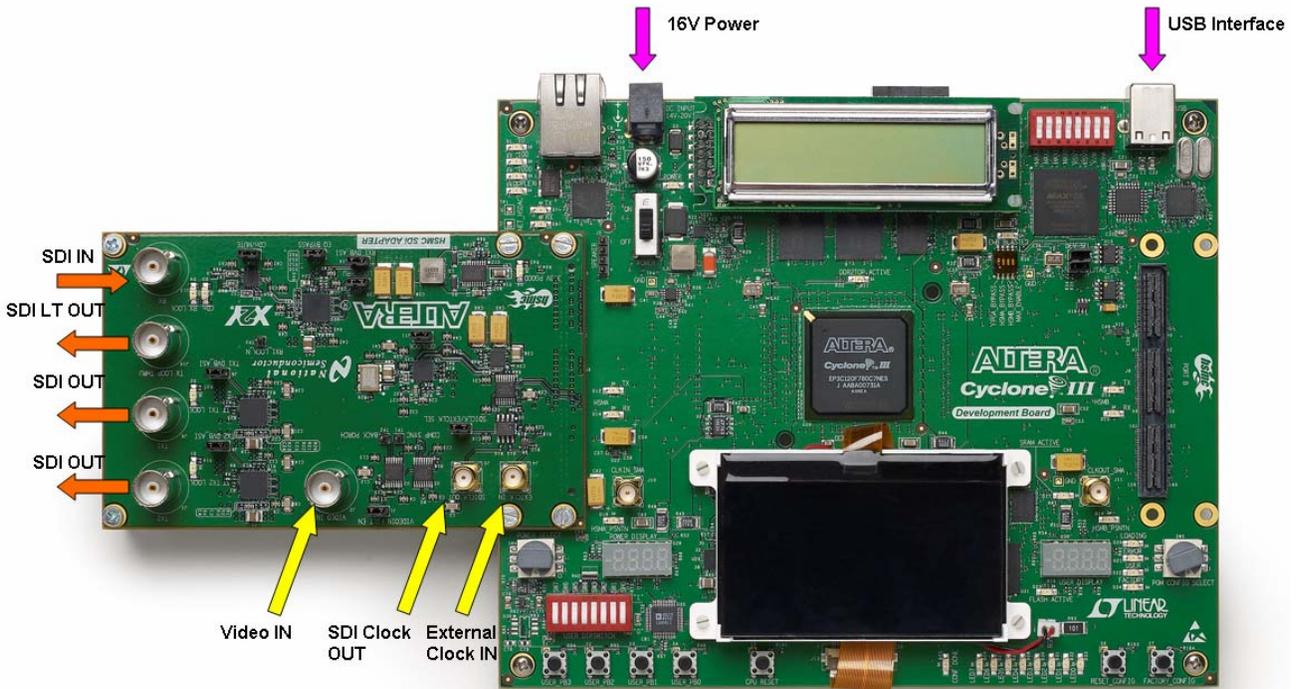


Figure 2 Evaluation Kit Connections

2.1 Cyclone III Development Board (Main Board) Description

The main board has a Cyclone III FPGA. The FPGA provides the SD/HD/3G SDI and general purpose stacks as well as the control interfaces through the supplied example firmware. The daughter board is connected to the main board through the high speed mezzanine connector (HSMC), J8. This connector provides power, control bus, and data bus. The main board communicates to a PC through a USB cable.

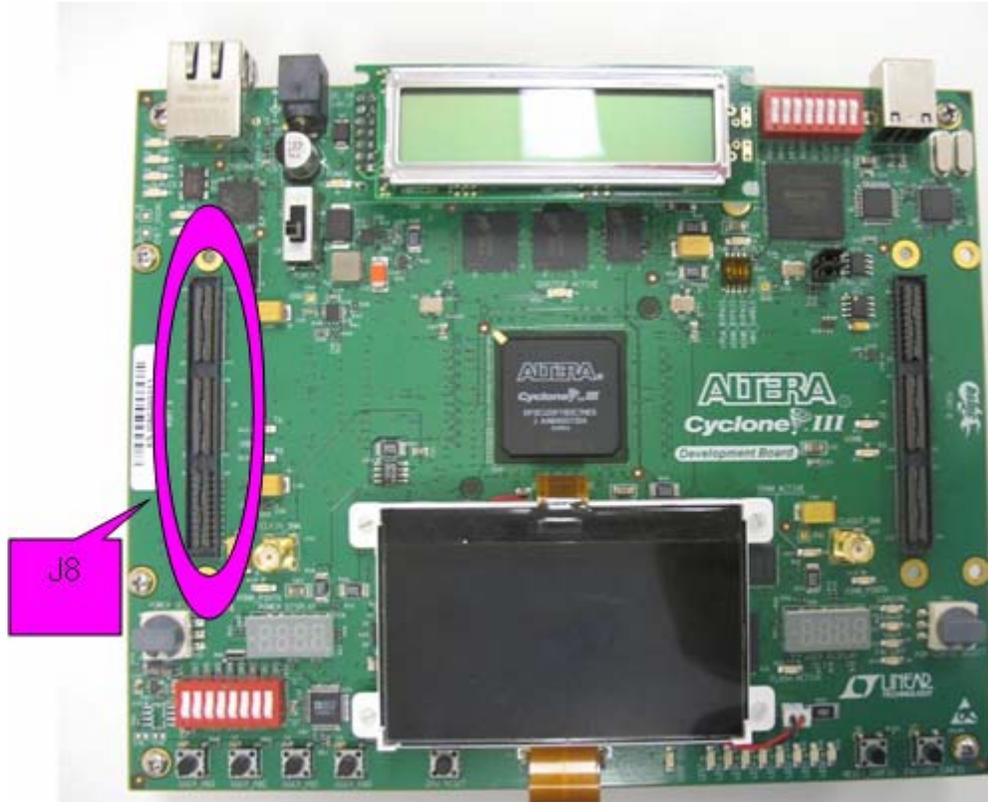


Figure 3 Cyclone III Development Board

2.2 Cyclone III Development Board Termination Resistors

The Altera Cyclone III device does not have any internal termination on the receive LVDS I/O's. Termination resistors must be added to the Cyclone III board. The terminations resistors must be placed as close to the FPGA's pin as possible. The 3C120 host board has the layout footprints for the termination resistors. Eleven 100 Ohm resistors in 0402 package size are required to install onto the host board. The resistors are located on the bottom side of the board. They are between the FPGA and the HSMC port A connector. Figures 4 and 5 show the schematic and board location of the LVDS termination resistors.

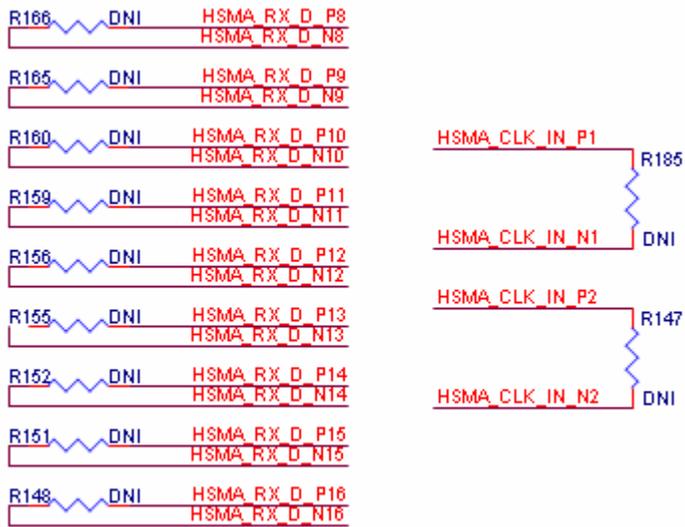


Figure 4 Resistors on HSCM port A

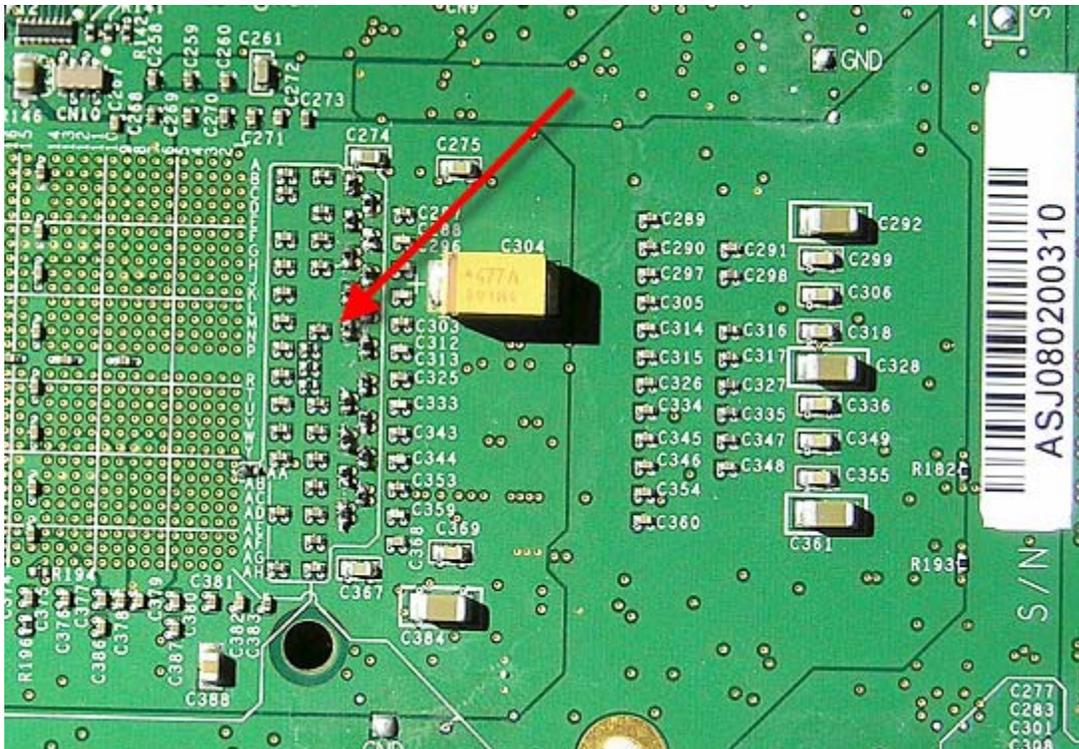


Figure 5 Photograph of the back of the Cyclone III board showing location of the 100 Ohm Resistors

2.3 SDALTEVK Board Description

The HSMC SDI ADAPTER board features the 5:1 LMH0340 serializer IC with integrated cable driver, the 1:5 LMH0341 deserializer IC and the LMH0344 adaptive cable equalizer IC, all highlighted in orange. These devices support SD, HD, or 3G SDI interfaces across 75 ohm coaxial cable, which can interface with the board via BNC connectors J3, J8, J10, or J13.

For added testing flexibility, the additional components shown in blue allow for several different clocking schemes. All of the clocking schemes are controlled by the DS90CP22 which is used to multiplex the various clock sources to the FPGA. The LMH1981 receives analog video via BNC connector J2 and provides the HSYNC and VSYNC to the LMH1982 for clock generation. The LMH1982 can also generate a clock based on a local 27 MHz oscillator. By using the DS90LV031A, an external clock can be applied to the card at SMA connector J4. In order to observe the quality of the clock provided to the FPGA, the clock can be routed to the DS90LV028A which will drive a CMOS clock out of SMA connector J5.

Power is provided to the board via two separate power rails that travel across the HSMC connector from the Cyclone III host board. The Powerwise® LM20242 adjustable frequency synchronous buck regulator supplies the 3.3V power for the evaluation card by using the 12V rail from the host board. The LP3878ADJ low noise regulator uses the 3V power of the host board to supply the 2.5V power to the evaluation card.

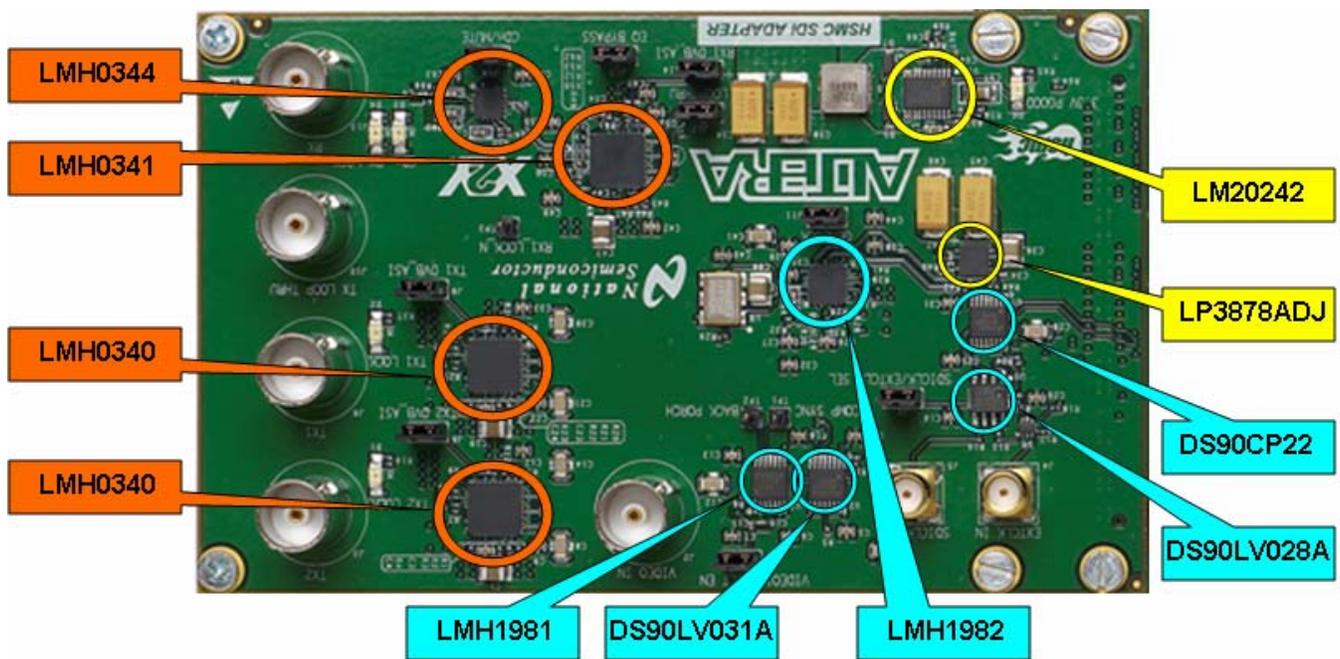


Figure 6 SDALTEVK

3 Software Setup

3.1 Installation

Make sure the Altera hardware is not connected to the PC. The following installation instructions are for the Windows XP Operating System. Quartus II 8.0 or newer is required to properly operate the SDALTEVK. If the terminal interface is desired then Nios II EDS 8.0 or newer must also be installed on the PC. If an older version of either Quartus II or Nios II EDS is already installed, make sure that it is updated before attempting to use the SDALTEVK. If necessary, please see <http://www.altera.com/products/> to download the latest software.

In order to use the Nios II terminal interface, Cygwin must be installed on the PC. Visit <http://www.cygwin.com/> to download the latest version of Cygwin for free. Make sure that the file "cygwin1.dll" is installed to the path:

C:\altera80\nios2eds\bin

Install the Quartus II 8.0 Software

Execute the Quartus II 8.0 software installation program. The program is called "80_quartus_windows.exe". This will load the driver files onto the PC.

- Follow the install instructions prompted by the Quartus install daemon

Install the Nios II EDS 8.0 Software

Execute the Nios II EDS installation program. The program is called "80_nios2eds_windows.exe".

- Follow the install instructions prompted by the Nios II install daemon

The software installation is complete.

3.2 Startup

Make sure all the software has been installed and the hardware is powered on and connected to the PC. Run Quartus II by either by using the path “C:\altera\80\quartus\bin\quartus.exe” or selecting it from the “altera” folder in the start menu. Once the software has loaded go to the “Tools” menu, and select “Programmer.”

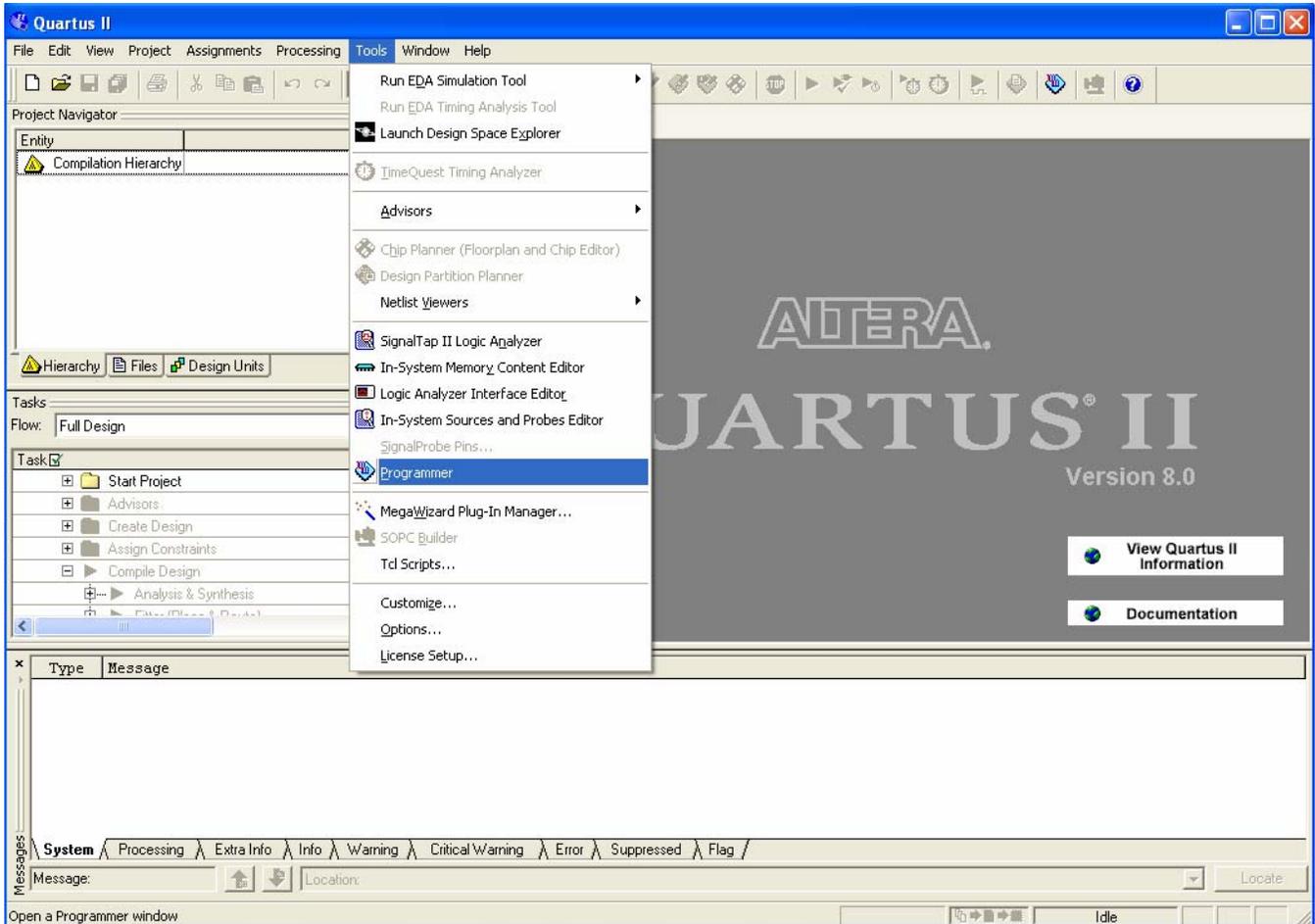


Figure 7 Quartus Main Screen

This will bring up the programming window shown below. Click on the “Hardware Setup...” button, select the USB-Blaster and click Close. Use the “Add File...” button to select the appropriate bit image to program the FPGA. Make sure that the “Program/Configure” box is checked and that the “Mode” menu has JTAG selected. Press the “Start” button to program the FPGA. Once the progress bar reaches 100%, the SDALTEVK is ready to use.

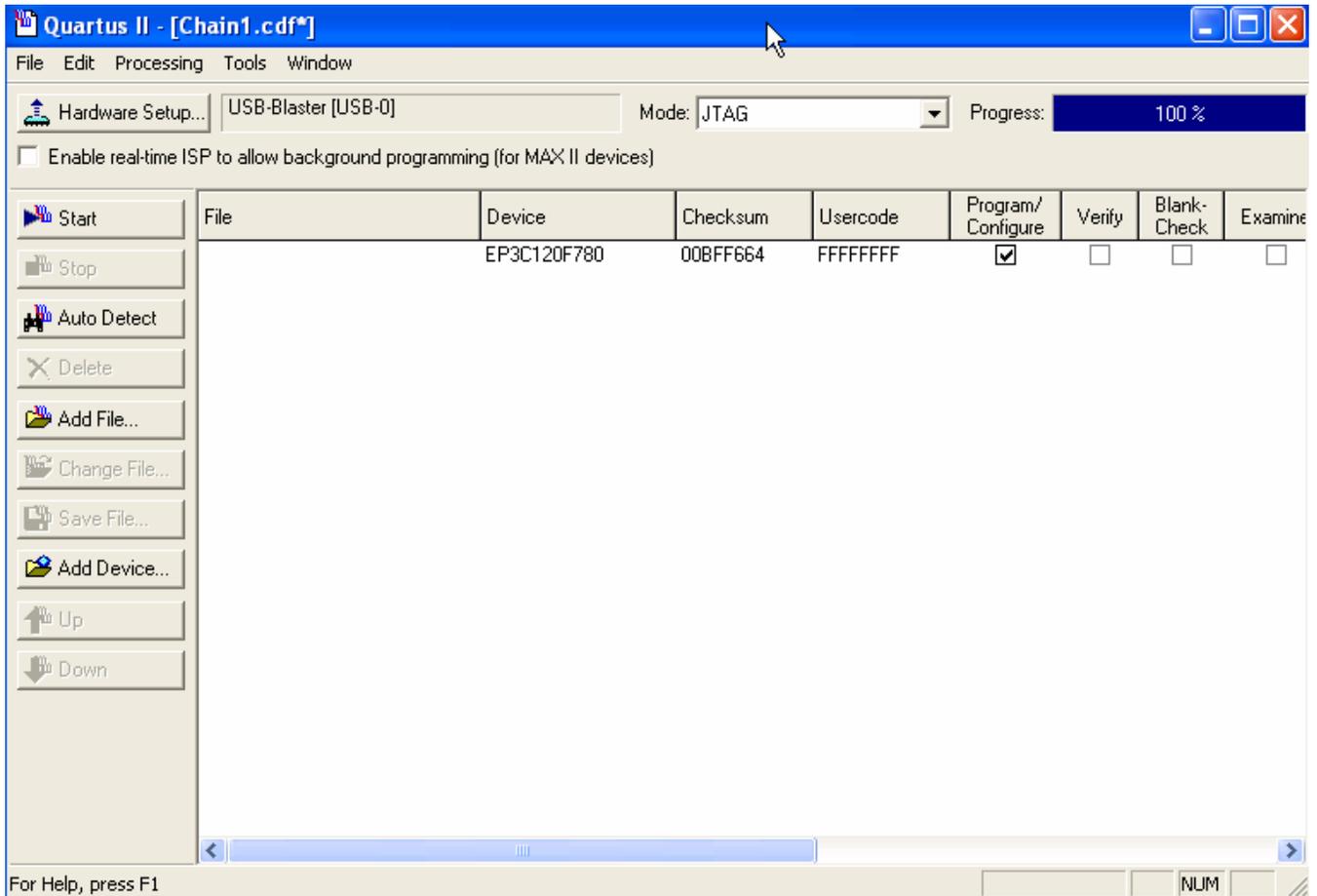


Figure 8 Quartus Programming Screen

Once the FPGA has been programmed, the SDALTEVK can be evaluated using the push button interface on the Cyclone III main board. However, if the terminal interface is desired for evaluation, run the Nios II terminal program called "nios2-terminal.exe". This program can be found in the bin folder of the Nios II root directory, for example "C:\altera\80\nios2eds\bin\nios2-terminal.exe". If the software loads correctly, a terminal window will appear with a greeting message as shown below.

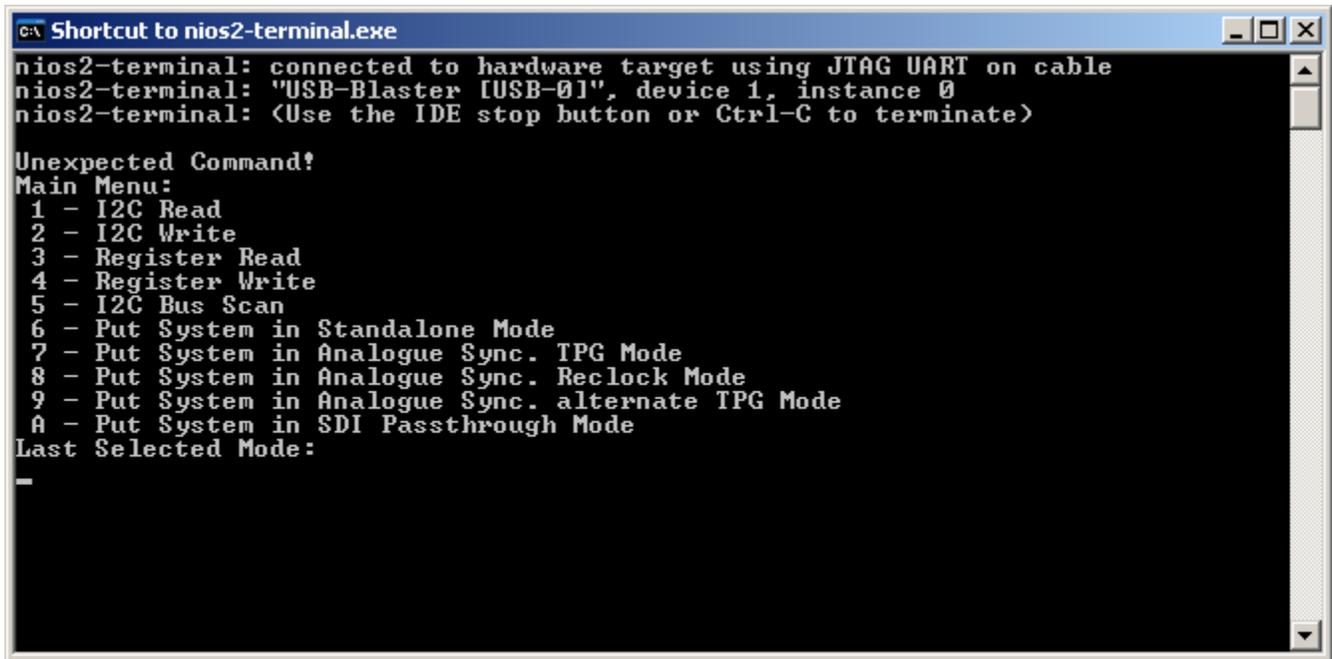


Figure 9 Nios II Terminal Main Menu

4 Evaluating Hardware

The EVK is designed for flexible and accurate evaluation of LMH0340 and LMH0341. Evaluation can be performed using internal or external stimuli.

There is an internal pattern generator implemented in the FPGA that will generate test patterns to verify signal transmission and signal integrity. The pattern generator can generate various types of SD, HD and 3G SDI static video patterns.

4.1 Test Setups

4.1.1 Standalone Video Generator Tests

In Standalone mode the system performance can be determined by the internal pattern generator. This is done by connecting the serializer output TX1 on J8 to the deserializer input RX on J13. The loop through output of the deserializer can be connected to external test equipment such as a WFM700 or an oscilloscope.

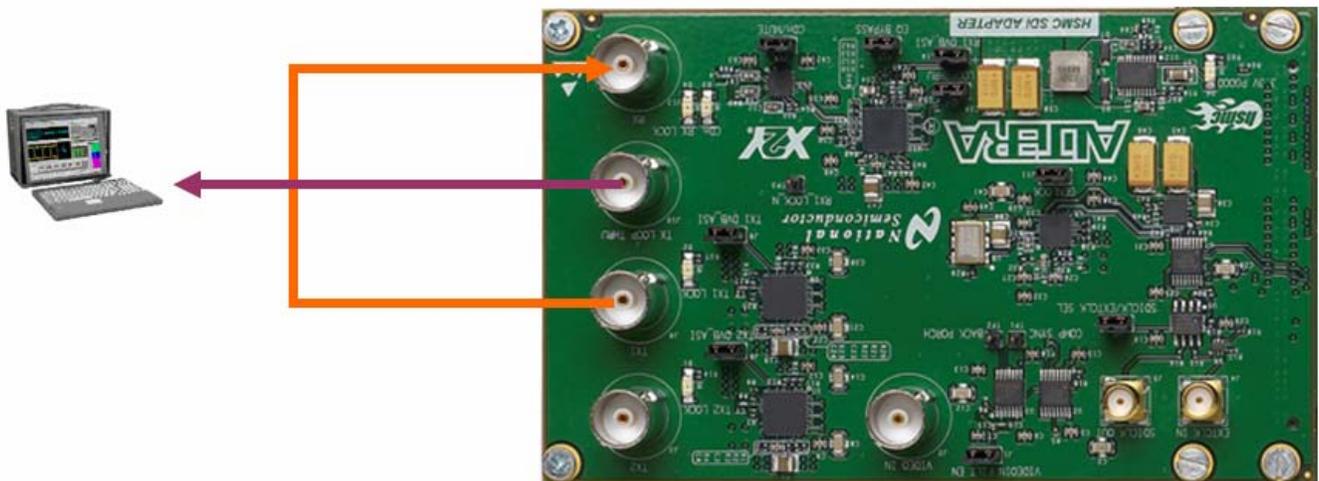


Figure 10 Loop-back Test Setup

4.1.2 Genlock Tests

When one of the genlocked modes is selected the system is configured to use an analog sync input to generate genlocked video. The analog reference signal is applied to the EVK through BNC connector J2. If no analog reference is present, the LMH1982 has been configured to automatically switch to the on board oscillator.

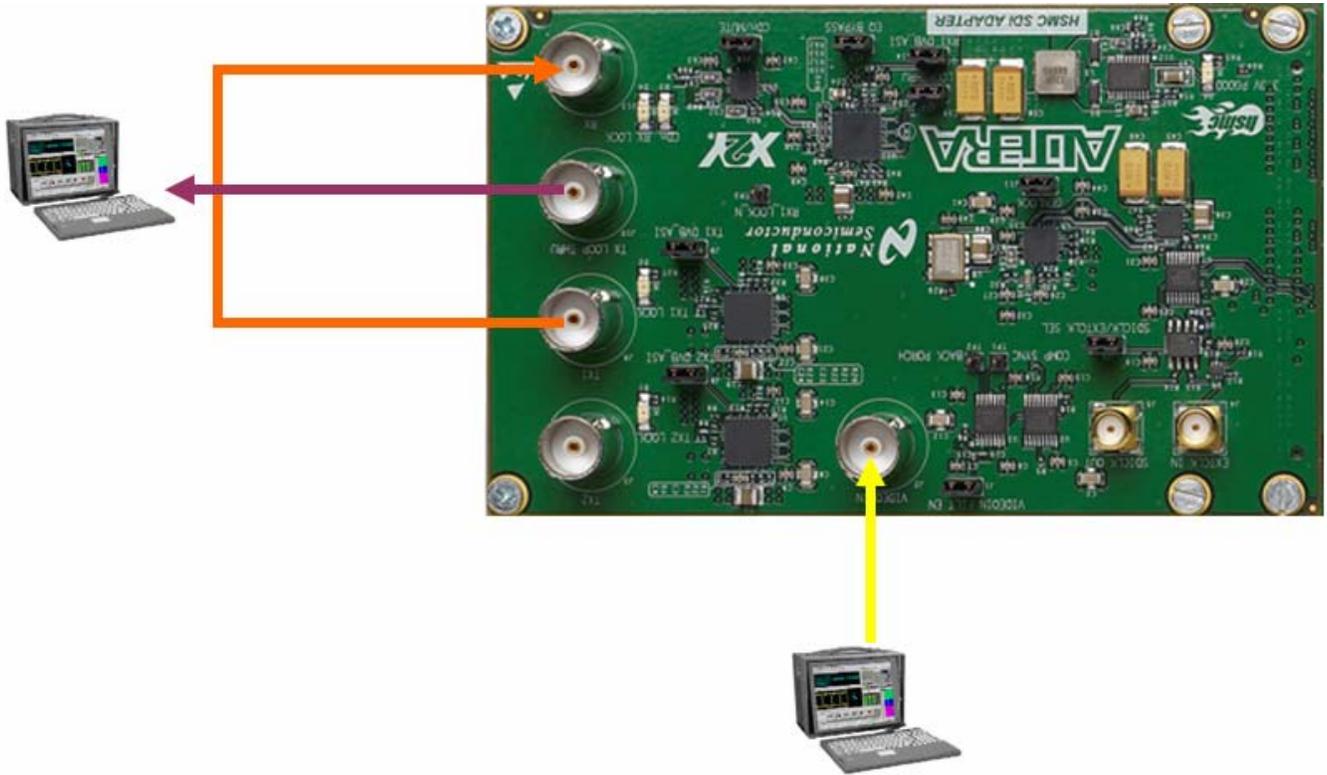


Figure 11 Genlock Test Setup

4.1.3 Video Pass-through Tests

In Pass-through Mode the EVK uses the clock recovered by the LMH0341 from the SDI input as the reference clock. The video data is then routed through the FPGA to the LMH0340 for transmission. To configure the EVK for Pass-through Mode connect the source generator to J13 of the deserializer and connect the terminating device to the serializer BNC connector J8. Refer to the diagram below. The loop through driver can also be connected to the terminating device via BNC connector J10.

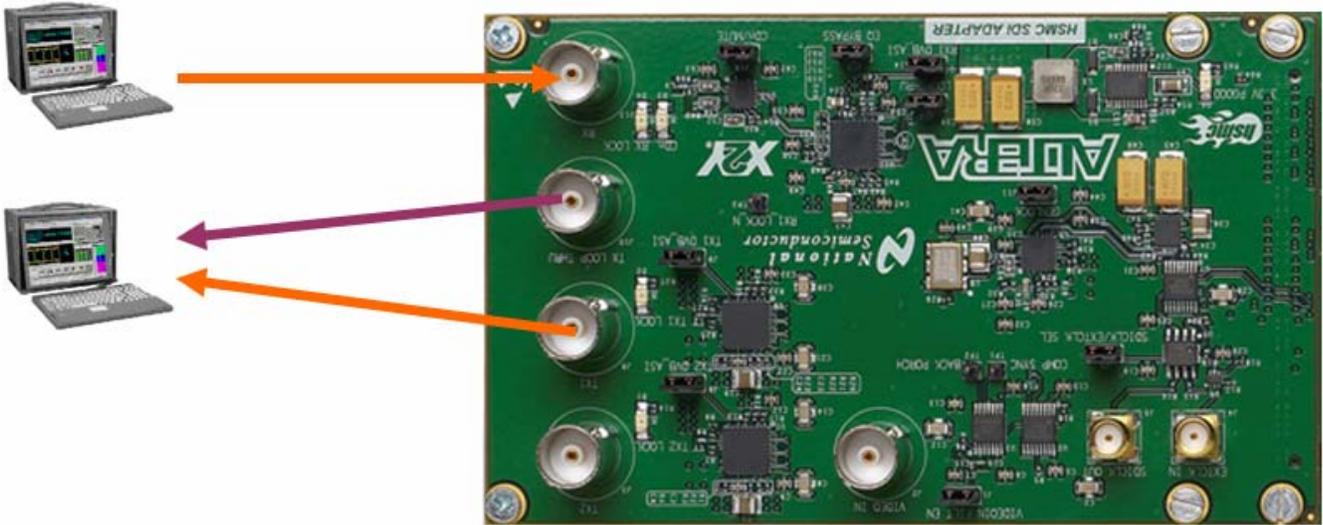


Figure 12 Pass-through Test Setup

4.2 Terminal Based SD/HD/3G SDI Evaluation

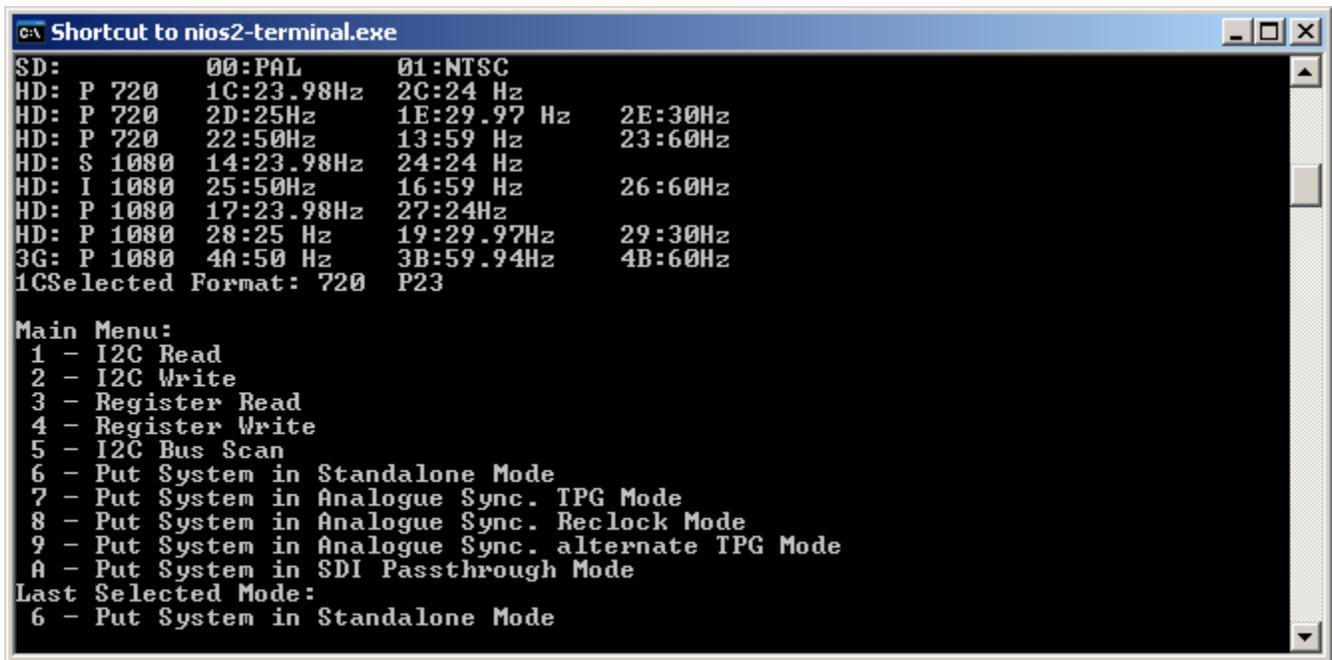
Below the terminal greeting message is the main menu. The table below gives a brief description of the main menu options.

Table 3 Terminal Menu Options

Menu Option	Name	Function
1	I2C Read	Read from a device register.
2	I2C Write	Write to a device register.
3	Register Read	Read from an FPGA register.
4	Register Write	Write to an FPGA register.
5	I2C Bus Scan	Returns 7-bit address of all devices on the serial control bus.
6	Put System in Standalone Mode	Configures system for Standalone Mode. Accesses format select menu.
7	Put System in Analog Sync TPG mode	Generates clock from Analog sync input and uses this to drive Test Pattern Generator
8	Put System in Analog Sync Reclock Mode	When supplied with an Analog Sync and a synchronous SDI input, the system uses the gunlock feature of the LMH1982 to reclock the SDI video with a clock derived from the analog input.
9	Put System in Analog Sync Alternate TPG mode	Generates Test patterns synchronized to the SDI input.
A	SDI Passthrough Mode	SDI video is received by the LMH0341, analysed and retransmitted, using the clock recovered from the LMH0341.

4.2.1 Standalone Mode

If Standalone Mode is selected from the main menu, a list of available video formats will appear. To select a video format enter the two digit code that appears directly to the left of the format title. Once a format is selected, the terminal will return to the main menu and the SDALTEVK will then be operating, sending a test pattern in the specified SDI video format. Once the two digit code is selected, the Selected format will be displayed followed by the Main Menu. After the main menu a reminder of what mode the system is currently in will be shown.



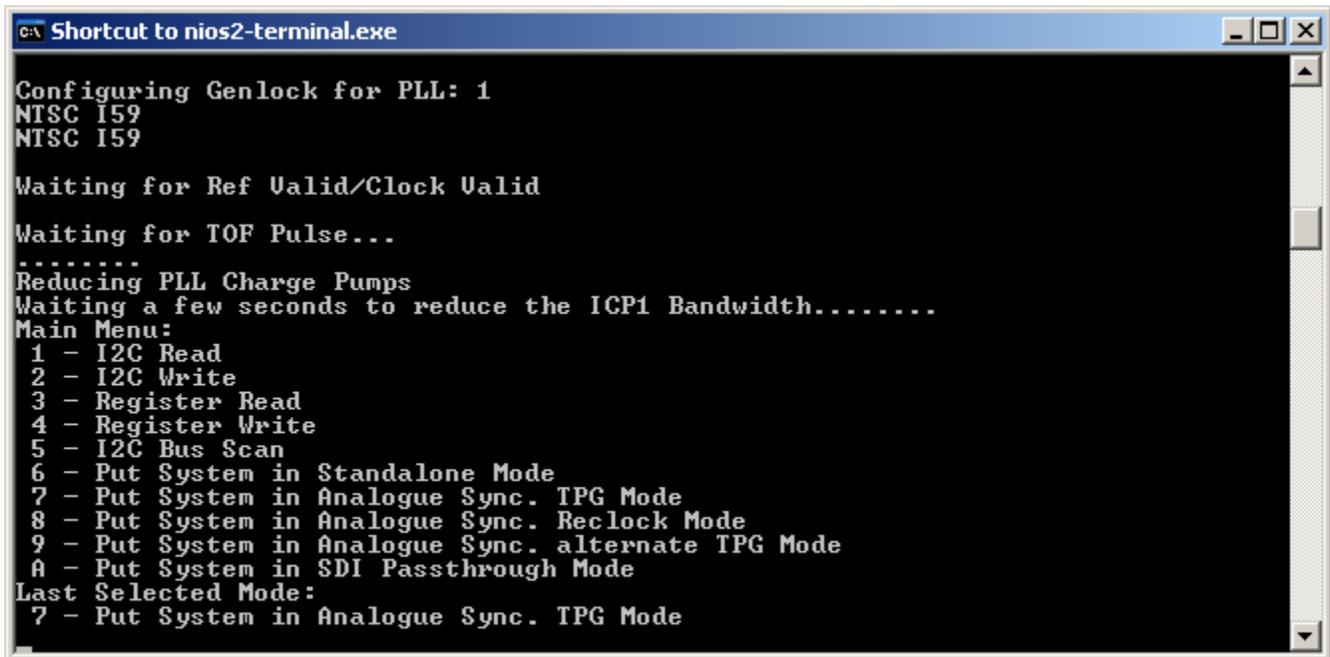
```
C:\> Shortcut to nios2-terminal.exe
SD:          00:PAL          01:NTSC
HD: P 720    1C:23.98Hz    2C:24 Hz
HD: P 720    2D:25Hz      1E:29.97 Hz    2E:30Hz
HD: P 720    22:50Hz      13:59 Hz      23:60Hz
HD: S 1080   14:23.98Hz    24:24 Hz
HD: I 1080   25:50Hz      16:59 Hz      26:60Hz
HD: P 1080   17:23.98Hz    27:24Hz
HD: P 1080   28:25 Hz      19:29.97Hz    29:30Hz
3G: P 1080   4A:50 Hz      3B:59.94Hz    4B:60Hz
1CSelected Format: 720 P23

Main Menu:
1 - I2C Read
2 - I2C Write
3 - Register Read
4 - Register Write
5 - I2C Bus Scan
6 - Put System in Standalone Mode
7 - Put System in Analogue Sync. TPG Mode
8 - Put System in Analogue Sync. Reclock Mode
9 - Put System in Analogue Sync. alternate TPG Mode
A - Put System in SDI Passthrough Mode
Last Selected Mode:
6 - Put System in Standalone Mode
```

Figure 13 Video Format Menu

4.2.2 Analog Sync TPG mode

In Analog Sync TPG mode, the user provides an analog sync signal to the analog sync input on the evaluation board (the BNC connector labeled 'Analog IN'). The LMH1981 extracts the sync information from this signal and passes it to the LMH1982 which generates video clocks for the FPGA, which are then used to clock the LMH0340 serializer and provide an SDI test signal output which is genlocked to the Analog input.



```
C:\> Shortcut to nios2-terminal.exe

Configuring Genlock for PLL: 1
NTSC 159
NTSC 159

Waiting for Ref Valid/Clock Valid

Waiting for TOF Pulse...

.....
Reducing PLL Charge Pumps
Waiting a few seconds to reduce the ICP1 Bandwidth.....
Main Menu:
1 - I2C Read
2 - I2C Write
3 - Register Read
4 - Register Write
5 - I2C Bus Scan
6 - Put System in Standalone Mode
7 - Put System in Analogue Sync. TPG Mode
8 - Put System in Analogue Sync. Reclock Mode
9 - Put System in Analogue Sync. alternate TPG Mode
A - Put System in SDI Passthrough Mode
Last Selected Mode:
? - Put System in Analogue Sync. TPG Mode
```

Figure 14 Analog Sync TPG Mode

4.2.3 Analog Sync Reclock Mode

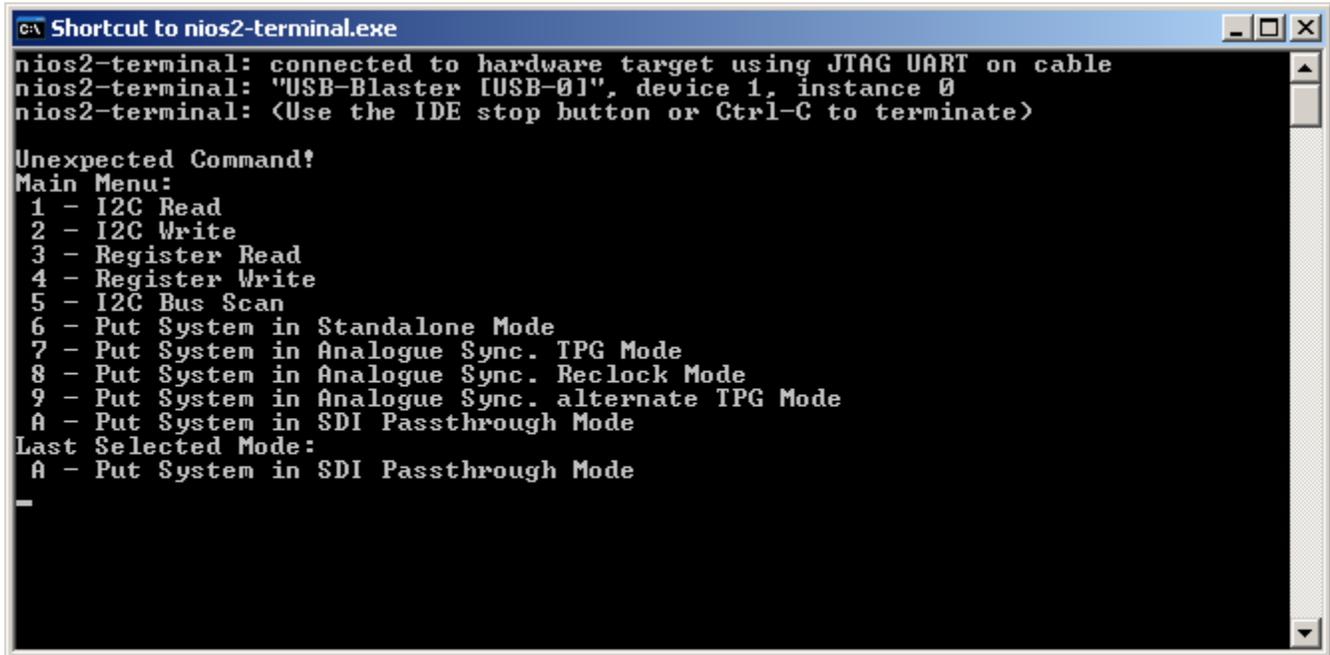
In Analog Sync Reclock Mode, you provide both an analog Sync input as in the Analog Sync TPG mode, and an SDI input which is genlocked to the Analog Sync input. The timing information is extracted from the analog signal, and a new serial clock is generated using the LMH1982, and this clock is used to reclock the data received through the SDI input port.

4.2.4 Analog Sync alternate TPG Mode

In Analog Sync Alternate TPG Mode, the system operates in a similar manner to the Analog Sync TPG mode, except that the output video format need not be the same as the analog sync input. For example you could use an analog sync from an NTSC 525 line 59.94 frame rate signal, and generate an SDI output which is an HD, 720P50 output.

4.2.5 Pass Through Mode

Before selecting Pass-through Mode from the main menu, apply an SD, HD or 3G SDI video signal from an external source to the SDALTEVK. When Pass-through Mode is selected from the main menu, a message will appear notifying if an input signal of a supported format is detected and return to the main menu.



```
C:\> Shortcut to nios2-terminal.exe
nios2-terminal: connected to hardware target using JTAG UART on cable
nios2-terminal: "USB-Blaster [USB-01]", device 1, instance 0
nios2-terminal: <Use the IDE stop button or Ctrl-C to terminate>

Unexpected Command!
Main Menu:
1 - I2C Read
2 - I2C Write
3 - Register Read
4 - Register Write
5 - I2C Bus Scan
6 - Put System in Standalone Mode
7 - Put System in Analogue Sync. TPG Mode
8 - Put System in Analogue Sync. Reclock Mode
9 - Put System in Analogue Sync. alternate TPG Mode
A - Put System in SDI Passthrough Mode
Last Selected Mode:
A - Put System in SDI Passthrough Mode
-
```

Figure 15 Pass-through Mode Screen

4.3 Push Button Based SD/HD/3G SDI Evaluation

The EVK can be configured for evaluation by using the push buttons on the Cyclone III main board only. The push button interface allows the EVK to be configured in the same modes as the terminal interface option. However, only the Nios II terminal interface allows for device and FPGA register access.

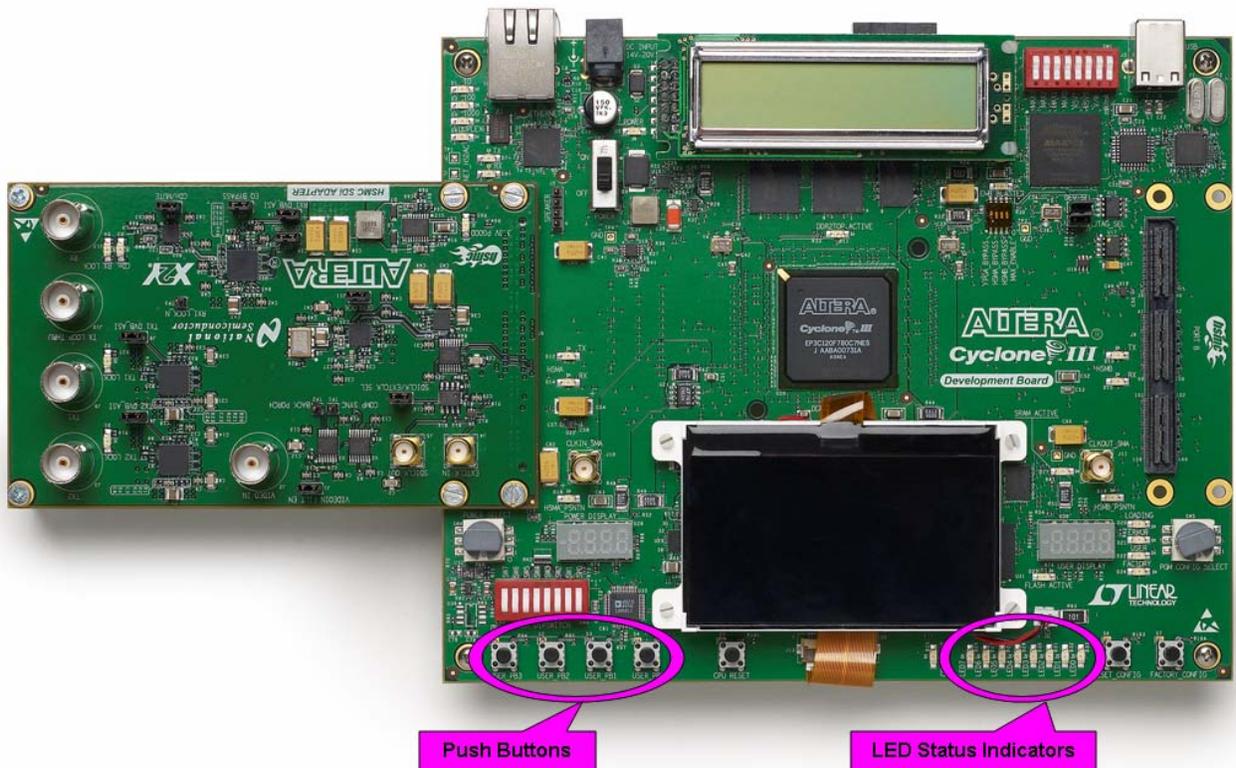


Figure 16 LED and Push Button Locations

4.3.1 Push Button Main Menu

After the FPGA has been programmed, the push buttons default to the main menu options. While in the main menu, LED 1 will blink. LED 6, 7, or 8 will illuminate to indicate the current configuration of the EVK.

PB 0	PB 1	PB 2	PB 3
System Mode	DP Settings	Video Format	Video Frequency

LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8
Blink	Off	Off	Off	Off	Genlock	Passthro h	Standalone

Figure 19) Main Menu Push Button Functions and Board Status LED Indications

4.3.2 System Mode

The System Mode menu contains the various configuration options for the EVK. Use this menu to configure the EVK into one of the 3 previously discussed modes of operations.

PB 0	PB 1	PB 2	PB 3
Cancel	Genlock	Passthrough	Standalone

LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8
Off	Blink	Off	Off	Off	Indicates Current Mode		

Once a mode has been selected, all of the LEDs will flash and the system will return to the main menu. A successful configuration is indicated by a single flash, while two flashes indicate a failure. If a failure occurs, refer to the table below for the most common causes.

Configuration	Typical Cause of Failure
Standalone	Incorrect format specified or mismatch between frequency and video format.
Genlock	No reference or invalid reference.
Passthrough	Input video not present or unrecognized.

4.3.3 Datapath Menu

This menu will be available in a future release. If this menu is selected the LEDs will flash twice and the system will return to the main menu.

4.3.4 Video Format Menu

The Video Format Menu configures the push buttons to navigate through the supported video formats. Users must select a video format with a compatible frequency in order for the system to be configured. If the system is in Standalone Mode and a valid combination is selected, the LEDs will flash once to indicate successful configuration. In other modes the video format and frequency settings are ignored. See the table below for the supported video formats and clock frequencies.

PB 0	PB 1	PB 2	PB 3
Cancel	OK	Up	Down

LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8
Off	Off	Blink	Off	Off	Indicates Current Mode		

5 Frequency Menu

This menu configures the push buttons to cycle through supported clock frequencies. Users must select a video format with a compatible frequency in order for the system to be configured. If the system is in Standalone Mode and a valid combination is selected, the LEDs will flash once to indicate successful configuration. In other mode the video format and frequency settings are ignored.

PB 0	PB 1	PB 2	PB 3
Cancel	OK	Up	Down

LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7	LED 8
Off	Off	Off	Blink	Off	Indicates Current Mode		

Figure 22) Frequency Menu Push Button Functions and Board Status LED Indications

Format Number	Clock Frequency						
	Active Lines	Type	13.5 MHz SD 000	74.17 MHz HD 001	74.25 MHz HD 010	148.35 MHz 3G 011	148.5 MHz 3G 100
0:0000	525	I	PAL				
1:0001	486	I	NTSC				
2:0010	720	P			720P50		
3:0011	720	P		720P59.94	720P60		
4:0100	1080	S		1080S23.9 8	1080S24		
5:0101	1080	I			1080I50		
6:0110	1080	I		1080I59.94	1080I60		
7:0111	1080	P		1080P23.9 8	1080P24		
8:1000	1080	P			1080P25		
9:1001	1080	P		1080P29.9 7	1080P30		
A:1010	1080	P					1080P50
B:1011	1080	P				1080P59.94	1080P60

Figure 23) Video Format and Clock Frequency Table

Depending on the format the frequency specified in Figure 22 can refer to either the field or frame rate. For interlaced images it is the field rate and for progressive and segmented frame it is the frame rate.

5.1 FPGA Register Map

This section describes the registers associated with the SDI Video Firmware. Registers can be either status or control, and are read or write respectively. The registers are grouped into several main sections:

1. Miscellaneous
2. Reset
3. Rx Video
4. Datapath
5. Clocking
6. Timing

5.1.1 Miscellaneous Registers:

Hex Address:	Name	Description	Bits	Bit Description
00	IPT ID	ID Code (1234 Hex)	15:0	ID Code

5.1.2 Reset Registers

Hex Address:	Name	Description	Bits	Bit Description
01	RESET STATUS	Status bits of various system resets	15:4	Reserved
			3	Deserializer Lock
			2	Serializer Lock
			1	CPU_RST_N
			0	CPU_RST
02	RESET CONTROL	Control Reset Signals	15:0	Reserved

5.1.3 Rx Video Registers

Hex Address:	Name	Description	Bits	Bit Description
03	RX VID STATUS	Status bits of Rx video	15:4	Reserved
			3	Vid Reset Flag: Indicates that video reset has been asserted
			2	Deser Flag: Indicates that the deserializer lock has toggled.
			1	Descram Flag: Indicates that the descrambler lock has toggled.
			0	Descram Locked: Indicates that the descrambler is locked onto incoming video
04	RX VID STD	Detected Video Standard	15:13	Reserved
			12	SMPTE 352 Packet Detected
			11	Reserved
			10:8	Frequency detected: 000 0 SD 270Mbps 001 1 HD 1.485/1.001 Gbps 010 2 HD 1.485 Gbps 011 3 HD 2.97/1.001 Gbps 100 4 HD 2.97 Gbps

Hex Address:	Name	Description	Bits	Bit Description
			7:4	Reserved
			3:0	Format Detected: 0000 0 PAL I50 0001 1 NTSC I59 0010 2 P720 50 0011 3 P720 60 0100 4 S1080 24 0101 5 I1080 50 0110 6 I1080 60 0111 7 P1080 24 1000 8 P1080 25 1001 9 P1080 30 1010 A P1080 50 1011 B P1080 60
05	CRC STATUS	CRC Error Check	15	Reserved
			14:0	CRC Error Count
06	CRC CONTROL	CRC Check Control	15:3	Reserved
			2	Select Holdover Mode
			1	Reset Status flags
			0	Reset CRC Error Count
07	EDH STATUS 1	EDH Error Check Status Reg	15	Reserved
			14:10	Full Field error flags
			9:5	Active Picture error flags
			4:0	ANC flags
08	EDH STATUS 2	EDH Error Check Status Reg 2	15	EDH Present
			14:12	EDH Detection Count (indicates intermittent EDH)
			11:8	Full Frame CRC error count
			7:4	Active Picture CRC error count
			3	Full Field CRC Error detected
			2	Active Picture CRC Error detected
			1	Full Field CRC valid
			0	Active Picture CRC valid

Hex Address:	Name	Description	Bits	Bit Description
09	EDHAP COUNT	Extended Count of EDH Errors	15:0	16 bit Active Picture EDH error count
0A	EDH FF COUNT	Extended Count of EDH Errors	15:0	16 bit Full Frame EDH error count
0B	AUDIO IN STATUS	Input Audio (Over SDI) Status	15:4 3 2 1 0	Reserved Group 4 detected Group 3 detected Group 2 detected Group 1 detected
0C	SMPTE35234	Extracted SMPTE352 Bytes 3, 4	15:0	SMPTE352 Bytes 4 and 3
0D	SMPTE35212	Extracted SMPTE352 Bytes 1, 2	15:0	SMPTE352 Bytes 2 and 1
0E	AUDIO IN CONTROL	I2S Output Control	15:1 0	Reserved Enable I2S Output

5.1.4 Datapath Registers

Hex Address:	Name	Description	Bits	Bit Description
10	DP STATUS	Datapath Status Register	15:0	Reserved
11	DP CONTROL		15 14:7 6 5 4 3 2 1 0	Data Pat Bypass Reserved Insert CRC/EDH Errors on output Insert EDH Packets on output Insert SMPTE352 Packets on output Insert audio on output Reserved Disable TPG/Output Received video Reserved
12	DP FORMAT CONTROL	Datapath Format Control	15 14:4 3:0	Force Format Reserved Select Video Format, see RX VID STD for values
13	DP FREQ	Datapath Frequency Control	15:3	Reserved

Hex Address:	Name	Description	Bits	Bit Description
	CONTROL		2:0	Selected Frequency, see RX VID FREQ for values
14	DP AUDIO OUT CONTROL	Control Audio Insertion Module	15:8 7:4 3 2 1:0	AFN (Audio Frame Count) Max Audio control packet rate Reserved Select internal tone generator (0) or I2S input (1) Select output audio group
15	AUDIO OUT STATUS	Audio Output Status	15:0	Reserved
16	AUDIO OUT INCR 1	Controls Increment Rate for Internal Tone Generator	15:8 7:0	Channel 1 Frequency Channel 2 Frequency
17	AUDIO OUT INCR 2	Controls Increment Rate for Internal Tone Generator	15:8 7:0	Channel 3 Frequency Channel 4 Frequency
18	AUDIO OUT CSB 1	Controls Audio CSB	15:8 7:0	Channel Status Block CRC Channel Status Block Byte 2
19	AUDIO OUT CSB 2	Controls Audio CSB	15:8 7:0	Channel Status Block Byte 1 Channel Status Block Byte 0
1A	TEST PATTERN CONTROL	Select Output test Pattern	15 14 13:12 11:6 5:4 3 2:0	Reserved RP219 Pattern Select 3A (0) 3B(1) RP219 Part 2 Pattern Select: 00 0 2A 01 1 2B 10 2 Y Valid Range Ramp 11 3 YUV Full Range Ramp Reserved Select Calculate Patterns: 00 0 Black 01 1 Pathological 10 2 Y Valid Range Ramp 11 3 YUV Full Range Ramp Reserved Pattern Select: 000 0 100% Color Bars

Hex Address:	Name	Description	Bits	Bit Description
				001 1 Sweep (not implemented) 010 2 Calculated Patterns 011 3 Pulse/Bar 100 4 RP219 Pattern 101 5 SMPTE Bars Others 100% Color Bars
1B	SMPTE 352 INSERT CONTROL	Allows bytes 3 and 4 of the SMPTE352 packet to be set	15:8 7:0	Byte 4 Byte 3
1C	LINE PATTERN UPDATE 1	16 MSB for line pattern update	15:0	Update Value
1D	LINE PATTERN UPDATE 2	16 LSB for line pattern update	15:0	Update Value
1E	LINE PATTERN UPDATE ADDR	Adress and write enable for pattern update	15 14:11 10:0	Write Enable Reserved Update adress

5.1.5 Clocking

Hex Address:	Name	Description	Bits	Bit Description
20	CLOCK STATUS: ALTERA	Status of ALtera PLLs	15:3 2 1 0	Reserved Active clock: specified whether the receive (0) or PLL (1) clock is for transmission Tx PLL Locked Rx PLL Locked
21	CLOCK CONTROL: ALTERA	Control Altera Clock selection	15 14:0	Select PLL (1) or Rx (0) Clock Reserved

5.1.6 Video Timing

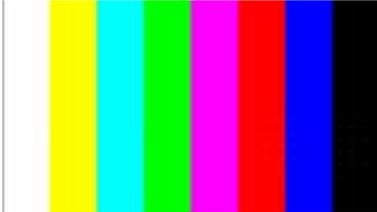
Hex Address:	Name	Description	Bits	Bit Description
23	CONTROL GENLOCK	Control Genlock Mode	15:2 1:0	Reserved Select System Mode: 00 0 Use Received Video Timing 01 1 Use Genlock timing 10 2 Freerun/User specified timing 11 3 Use Genlock timing with user specified format
24	GENLOCK STATUS	Status of Gunlock Interface	15 14:12	Progressive video on reference SD HD 3G Format

Hex Address:	Name	Description	Bits	Bit Description
			11	Reserved
			10	Genlock reference present
			9	Genlock No Lock
			8	Genlock No Ref
			7	Reserved
			6:4	Genlock frequency, as per RX VID FREQ
			3:0	Genlock format, as per RX VID STD
25	VFORMAT STATUS	Looks for Matching VFORMAT Sequences from the LMH1981 and Decodes Them	15	Reserved
			14:12	Decoded format type: 000 0 Unknown 001 1 PAL 010 2 NTSC 011 3 576P 100 4 480P 101 5 720P 110 6 1080I 111 7 1080P
			11	Reserved
			10:0	Vformat received from LMH1981
26	LINE TIME COUNT	Used to Determine Format. See Genlock_if module for details	15:0	Line time count 16 MSB
27	STATUS GENFORMAT	Format Used to Drive Timing Generator	15:11	Reserved
			10:8	Frequency selected, as per RX VID FREQ
			7:4	Reserved
			3:0	Format selected, as per RX VID STD
28	STATUS TIMING	Status of Timing Generator	15	Input present
			14:12	Reserved
			11	Sync to input timing
			10:8	Reserved

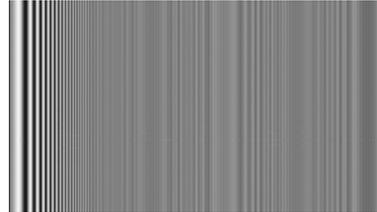
Hex Address:	Name	Description	Bits	Bit Description
			7:0	Counts when timing is resynchronized

5.2 Supported Test Patterns

The following test patterns are available from the SDI firmware in all SD, HD and 3G formats:



100% Color Bars



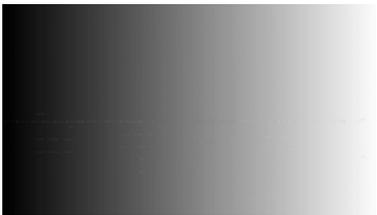
Frequency Sweep



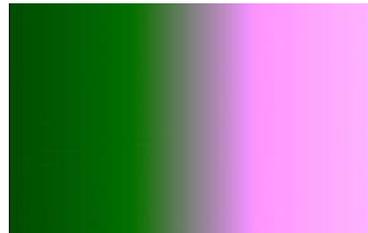
Black



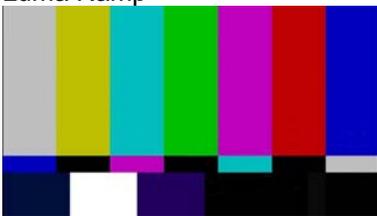
Matrix Pathological



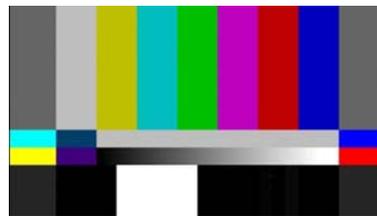
Luma Ramp



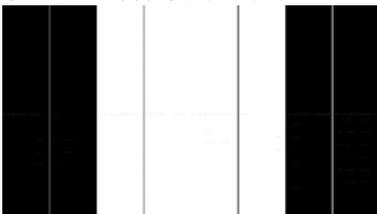
Y/C Full Range Ramp



SMPTE 75% Color Bars



SMPTE RP219 Color Bars



Luma Pulse & Bar

6 Documentation

Additional SDALTEVK documentation can be found on the EVK website.

7 Schematics, BOMs, and Data Sheets

All of the schematics, BOMs, and data sheets for the SDALTEVK can be found on the EVK website.

8 Reference FPGA IP

The reference FPGA IP source code and documentation can be found on EVK website.

9 Up to Date Information

For up to date information check this URL <http://www.national.com/sdaltevk>

10 Part Numbers

Cyclone III Development Board: [DK-DEV-3C120N](#)

<http://www.altera.com/products/devkits/altera/kit-cyc3.html>

LMH0340/LMH0341 Evaluation Kit: SDALTEVK

Revision History

Release	Date	Who	Revisions
0.00	8-19-2008	M. Wolfe	Creation
0.01	8-19-2008	M. Wolfe	1 st draft
0.02	8-25-2008	N. Unger	Updated TOC Table headings Column widths
0.03	8-28-2008	N. Unger	Put revision history at the end Change font of the TOC to Ariel Inserted termination resistor instructions Minor wording changes on Table 1
0.04	9-02-2008	N. Unger	Updated Altera Part Number to DK-DEV-3C120N
0.05	9-03-2008	N. Unger	Recovered File Changed date format in the revision history
0.06	07-09-2009	M. Sauerwald	Updated for December 2008 IP release

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