

SERDESUB-913 User's Guide

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Introduction:

National Semiconductor's Automotive SERDES DS90UB913/914Q FPD-Link III evaluation kit contains one (1) DS90UB913Q Serializer board and one (1) DS90UB914Q Deserializer board. The boards are mounted with the Rosenberger connectors for connectivity using the Leoni-Dacar cables (not sent along with the kits). The boards also have the option of being populated with single ended coaxial cables. This mode is for evaluation purposes only.

The DS90UB913Q/914Q chipset supports a variety of automotive mega-pixel camera systems over a two (2) wire serial stream. The single differential pair (FPD-Link III) is well-suited for direct connections between an imager and Host Controller/Electronic Control Unit (ECU)/FPGA. The bidirectional control channel of the DS90UB913Q/914Q provides seamless communication between the ECU/FPGA and the display module.

This kit will demonstrate the functionality and operation of the DS90UB913Q and DS90UB914Q chipset. The chipset enables transmission of a high-speed video data along with a low latency bi-directional control bus over a single twisted pair cable. The integrated control channel transfers data bi-directionally over the same serial video link. The transport delivers 10/12 bits of parallel data, two SYNC bits and PCLK together with a bidirectional control channel that supports an I²C bus. Additionally, there are four unidirectional general purpose (GPI and GPO) signal lines for sending control data. This interface allows transparent full-duplex communication over a single high-speed differential pair, carrying asymmetrical bi-directional control information without the dependency of video blanking intervals. The Serializer and Deserializer chipset is designed to transmit data at PCLK clocks speeds ranging from 10 to 100 MHz and I²C bus rates up to 400 kbps at up to 10 meters cable length over -40 to +105 Deg C.

The user needs to supply only a single 5V supply to the Deserializer boards as these kits have power transfer over coax/ power transfer over differential pair capabilities.

The demo boards can be used for EMI testing.

System Requirements:

In order to demonstrate, the following are required:

- 1) Mega-pixel imager modules such as the Omnivision OV10630 or Aptina MT9M023/24.
- 2) Microcontroller (MCU) or FPGA with I²C interface bus (I²C master)
 - a. slave clock stretching must be supported by the I²C master controller/MCU.
- 3) External peripheral device that supports I²C (slave mode)
- 4) 5V power supply.

Contents of the Demo Evaluation Kit:

- 1) One Serializer board with the DS90UB913Q
- 2) One Deserializer board with the DS90UB914Q

DS90UB913Q/914Q SerDes Typical Application

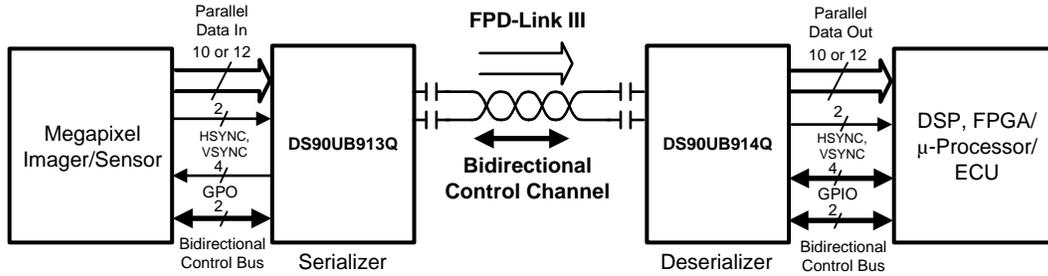


Figure 1. Typical Application of DS90UB913Q/914Q Chipset

The diagram above illustrates a typical application of DS90UB913Q/914Q chipset. The ECU/FPGA can program device registers on the DS90UB913Q, DS90UB914Q, and remote peripheral device, such as a display module.

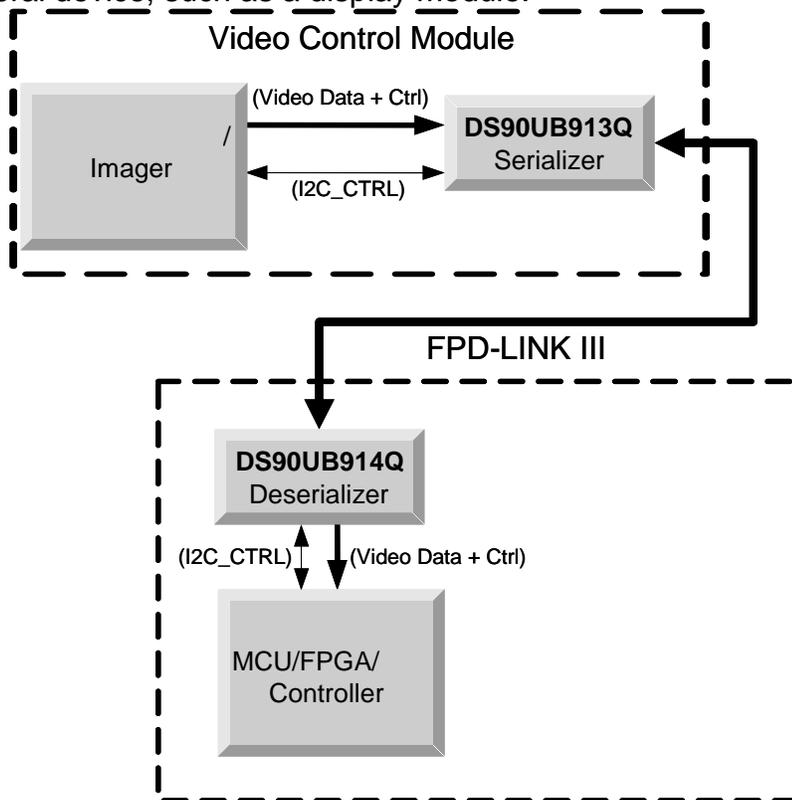


Figure 2. Typical DS90UB913Q/914Q Imager System Diagram

Refer to the proper datasheet information on Chipsets (Serializer/Deserializer) for more detailed information.

How to set up the Demo Evaluation Kit:

The DS90UB913Q/914Q evaluation boards consist of two sections. The first part of the board provides the point-to-point interface for transmitting parallel video data. The second part of the board allows bi-directional control communication of an I²C bus control of using a MCU/FPGA to programming a remote peripheral device via the Serializer.

The PCB routing for the Serializer input pins (DIN) accept incoming parallel video data at 1.8V/3.3V LVCMOS signals from J1 IDC connector. The FPD-Link III interface can use a single twisted pair cable or a single coax cable. The output pins (ROUT) are accessed through a JP1 IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

- 1) Connect the DS90UB913/914Q demo boards using a Leoni/Dacar cable or a coaxial cable(not provided)
- 2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings and datasheet for more details. The jumpers and connectors are configured in external oscillator mode with the VDDIOs toggling at 3.3V.
- 3) From the imager, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the Deserializer board to the ECU/FPGA module.
Note: For 50 ohm signal sources, provide 1.8V/3.3V LVCMOS input signal levels into DIN[12:0], HS, VS and PCLK
- 4) Connect the Deserializer I²C ports to the I²C of the MCU/FPGA (I²C master). Connect the Serializer I²C ports to the I²C bus of the peripheral slave device.
- 5) Power for the Serializer and Deserializer boards must be supplied externally through JP5 on the Deserializer board and JP4 on the Serializer board.

Bi-Directional Control Bus And I²C Modes:

In order to communicate and synchronize with remote devices on the I²C bus through the bi-directional control channel, slave clock stretching must be supported by the I²C master controller/ECU. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I²C slave pulls the SCL line low prior to the 9th clock of every I²C data transfer (before the ACK signal).

The bidirectional control bus supports an I²C compatible interface that allows programming of the DS90UB913Q, DS90UB914Q, or an external remote device (such as an imager). Register programming transactions to/from the DS90UB913Q/914Q chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and must be pulled-up to VDDIO by external resistors. The boards have an option to use the on-board 10K Ω pull-up resistors tied to VDDIO or connected through external pull-ups at the target Host. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UB913Q/914Q I²C bus data rate supports up to 400 kbps according to I²C specification.

Demo Board Power Connections:

Power should be only applied to the DS90UB914Q Deserializer boards. Power is transferred over the link using either the Differential pair.

DS9UB913Q Serializer Board Description:

The 2x15-pin IDC connector JP1 accepts 10/12 bits of 1.8V or 3.3V data, HS, VS and PCLK. VDDIO must be set externally for 1.8V or 3.3V LVCMOS inputs using jumper JP8 and JP6 on the Serializer and Deserializer boards respectively.

The Serializer board can be powered from the Deserializer board. For the Serializer to be operational, the S1-PDB switch on 1 must be set HIGH. S1-RES0 must be set LOW.

The boards can be connected to the Deserializer boards using either Rosenberger connectors.

Configuring the Mode Pin on the Serializer Board

To configure the device in the external oscillator mode, PCLK mode or the AON clock mode, switch S8 has to be configured as shown in Table. 1.

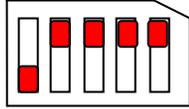
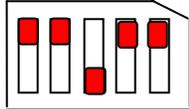
Mode Configuration	Switch S8 Settings
PCLK from imager	
External Oscillator Mode	

Table 1. Mode switch configuration on the Serializer Board

Serializer LVCMOS Pinout by Connector

The following three tables illustrate how the Deserializer connections are mapped to the IDC connector J1 on the Serializer board.

JP1 LVCMOS I/O			
pin no.	name	name	pin no.
1	GND	DIN0	2
3	GND	DIN1	4
5	GND	DIN2	6
7	GND	DIN3	8
9	GND	DIN4	10
11	GND	DIN5	12
13	GND	DIN6	14
15	GND	DIN7	16
17	GND	DIN8	18
19	GND	DIN9	20
21	GND	DIN10	22
23	GND	DIN11	24
25	GND	HS	26
27	GND	VS	28
29	GND	PCLK	30

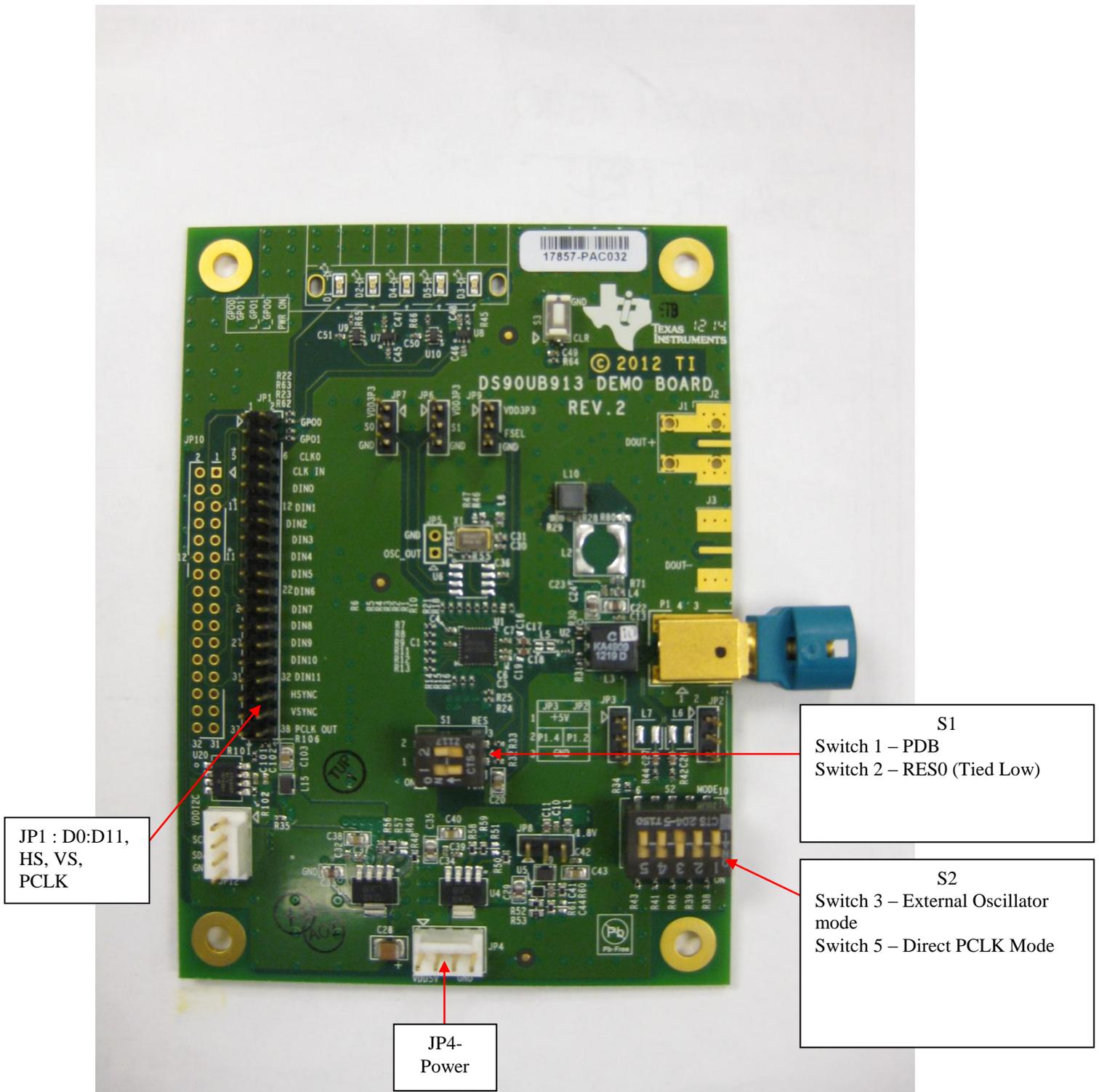


Figure 3. DS90UB913Q Boards with HSD Connector

DS9UB914Q Deserializer Board Description:

The Deserializer board can be powered using header JP5. For the Deserializer to be operational, follow the dip switch configuration for S1 and S2 shown in Table 2 and Table 3. The 2x15 pin IDC Connector JP1 provides access to the 1.8V or 3.3V LVCMOS data, HS, VS and PCLK outputs.

The Deserializer board is by default configured to operate in the 100MHz mode with 3.3V I/O. The default device address of the DS90UB914Q on the Board is C0.

Dip Switch S2 Configuration on the Deserializer Board

To configure the DS90UB914Q device on the Deserializer board, please follow Table.2.

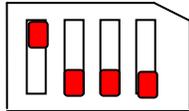
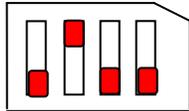
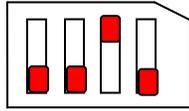
Mode Configuration	Switch S6 Settings
12-bit Low Frequency Mode	
12-bit High Frequency Mode	
10-bit Mode	

Table 2. Mode Switch Configuration on the Deserializer Board

Dip Switch S1 Configuration on the Deserializer Board

To configure the DS90UB914Q device on the Deserializer board, please follow Table.2.

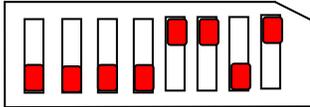
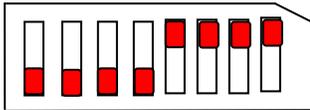
Mode Configuration	Switch S6 Settings
Normal Mode configuration	
BIST Mode configuration	

Table 3. Mode Switch Configuration on the Deserializer Board

Deserializer LVCMOS Pinout by Connector

The following table illustrates how the Deserializer connections are mapped to the IDC connector J1 on the Serializer board.

J1			
LVCMOS I/O			
pin no.	name	name	pin no.
1	ROUT0	GND	2
3	ROUT1	GND	4
5	ROUT2	GND	6
7	ROUT3	GND	8
9	ROUT4	GND	10
11	ROUT5	GND	12
13	ROUT6	GND	14
15	ROUT7	GND	16
17	ROUT8	GND	18
19	ROUT9	GND	20
21	ROUT10	GND	22
23	ROUT11	GND	24
25	HS	GND	26
27	VS	GND	28
29	PCLK	GND	30

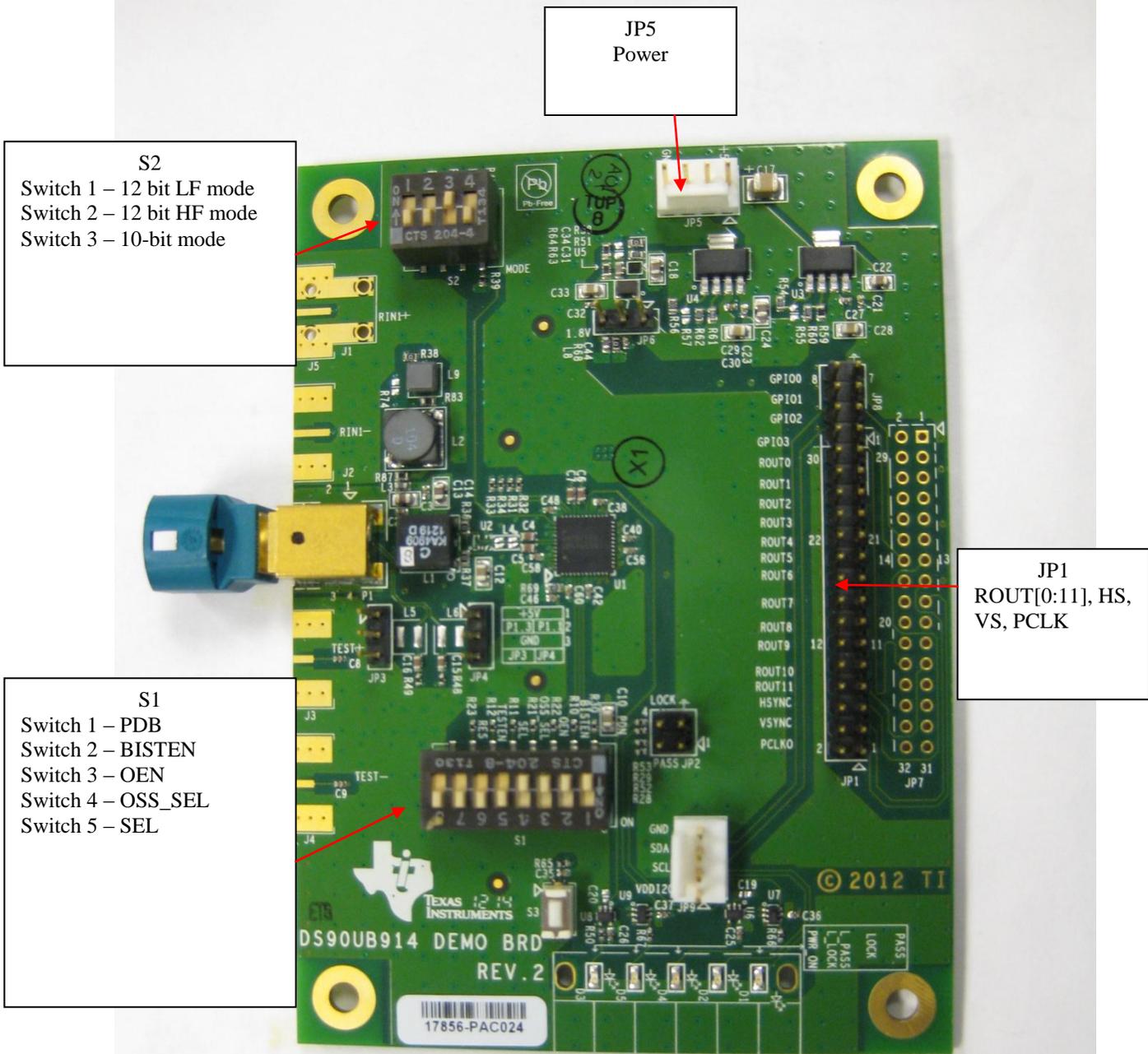


Figure 4. DS90UB914Q Deserializer boards with HSD Connectors

Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Serializer inputs:

- 1) Image Sensor such as the OV10630 or MT9M024
- 2) Any other signal generator / video source that generates the correct input levels.

The following is a list of typical test equipment that may be used to monitor the output signals from the Deserializer:

- 1) Microcontroller or FPGA with an I²C interface
- 2) Optional – Logic Analyzer or Oscilloscope
- 3) Any SCOPE with a bandwidth of at least 50MHz for 1.8V/3.3V LVCMOS and/or 1.5GHz for observing differential signals.

Troubleshooting Demo Setup

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

QUICK CHECKS:

1. Check that Powers and Grounds are connected to both Serializer and Deserializer boards.
2. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB register) edge of the clock.
3. Check that the Jumpers and Switches are set correctly.
4. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem...	Solution...
There is only the output clock.	Make sure the data is applied to the correct input pin.
There is no output data.	Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and Deserializer boards to make sure that the devices are enabled (PDB=Vdd) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the Serializer and Deserializer boards.
After powering up the demo boards, the power supply reads less than 1.8V when it is set to 1.8V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers. It is not intended to be an endorsement of any particular equipment or supplier.

Cable References

For optimal performance, we recommend Shielded Twisted Pair (STP) 100ohm differential impedance and 24 AWG (or larger diameter) cable for high-speed data applications.

Leoni Dacar 535 series cable:

www.leoni-automotive-cables.com

Rosenberger HSD connector:

www.rosenberger.de/en/Products/35_Automotive_HSD.php

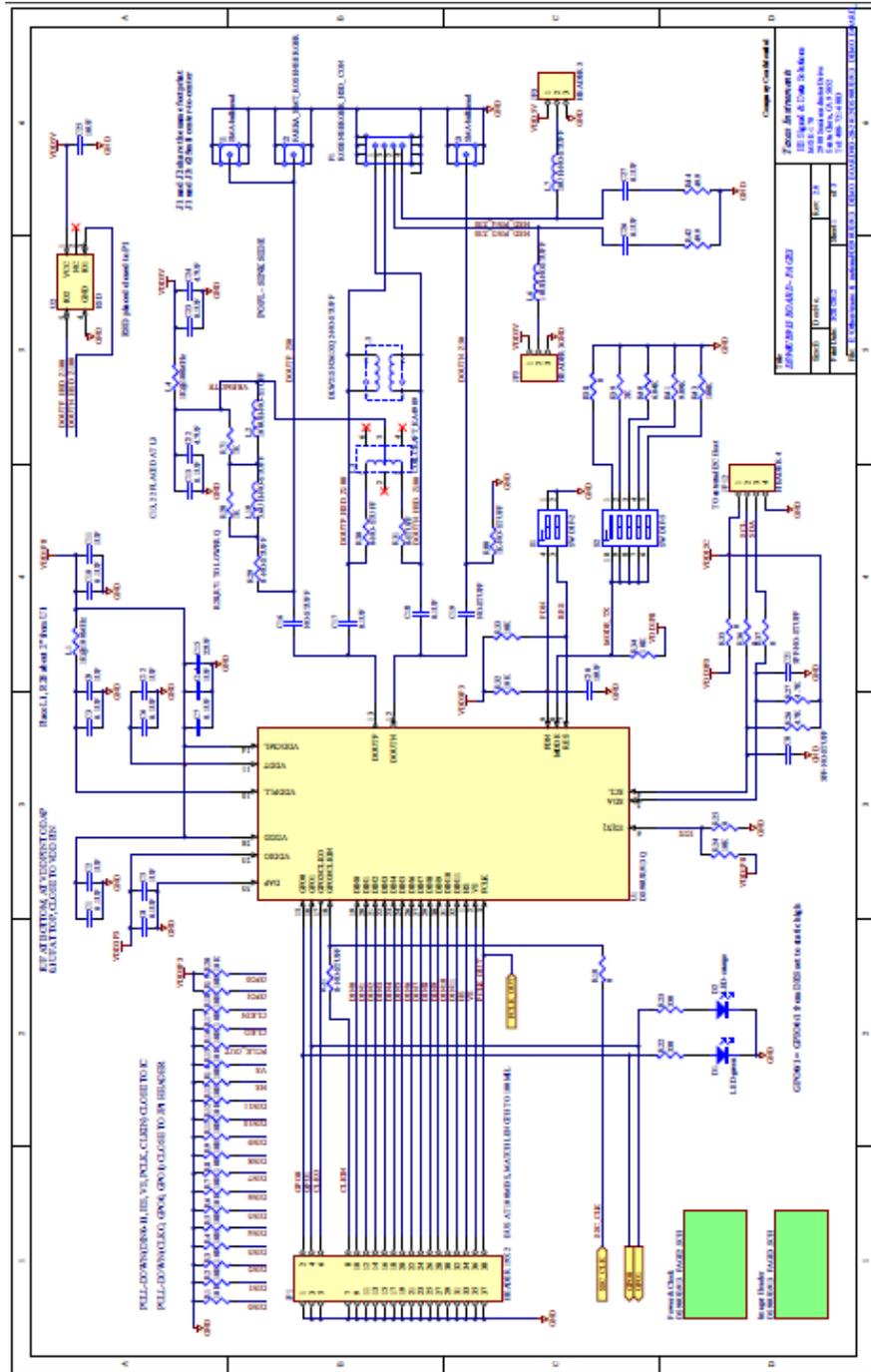
Equipment References

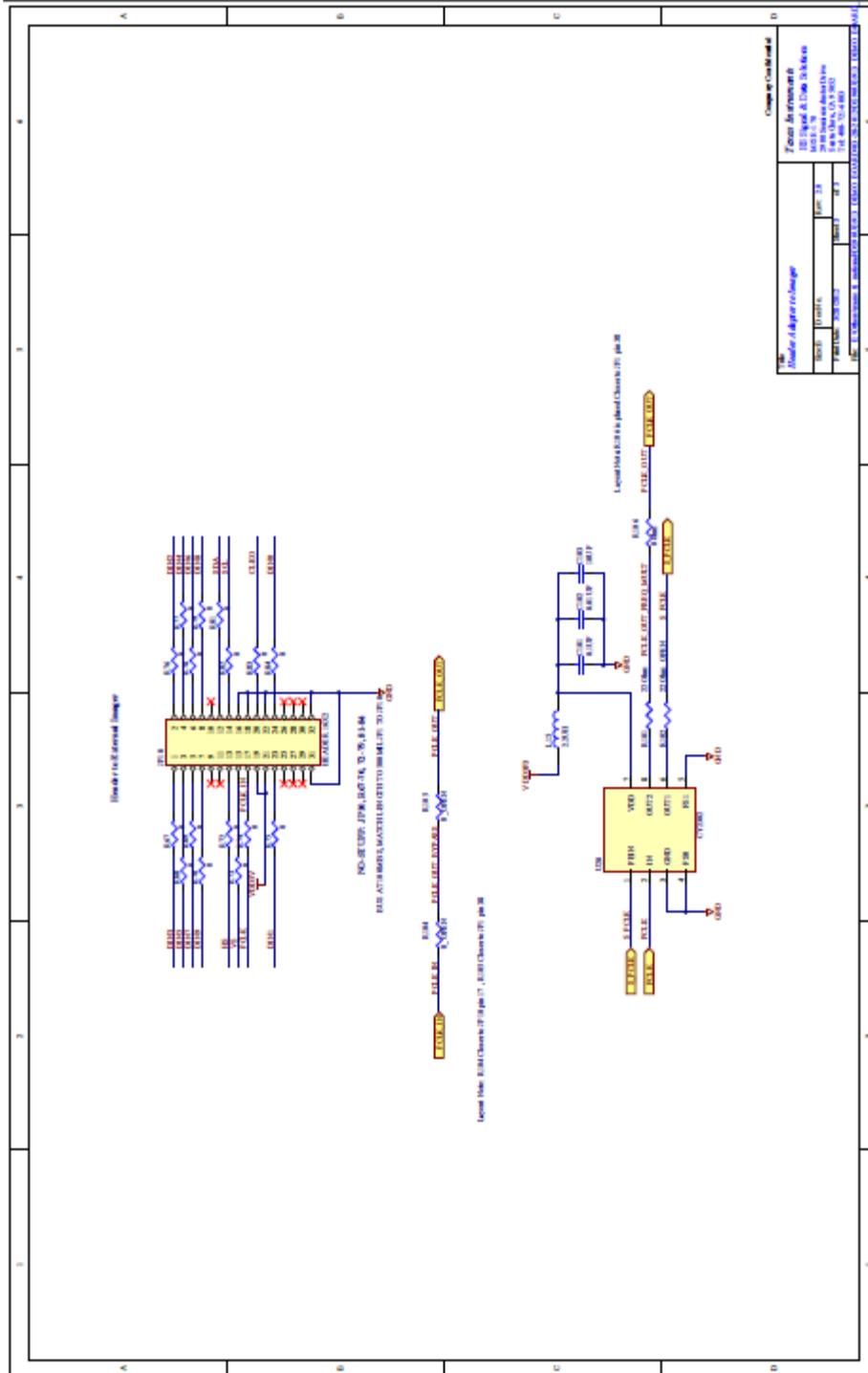
Corelis CAS-1000-I2C/E I2C Bus Analyzer and Exerciser Products:

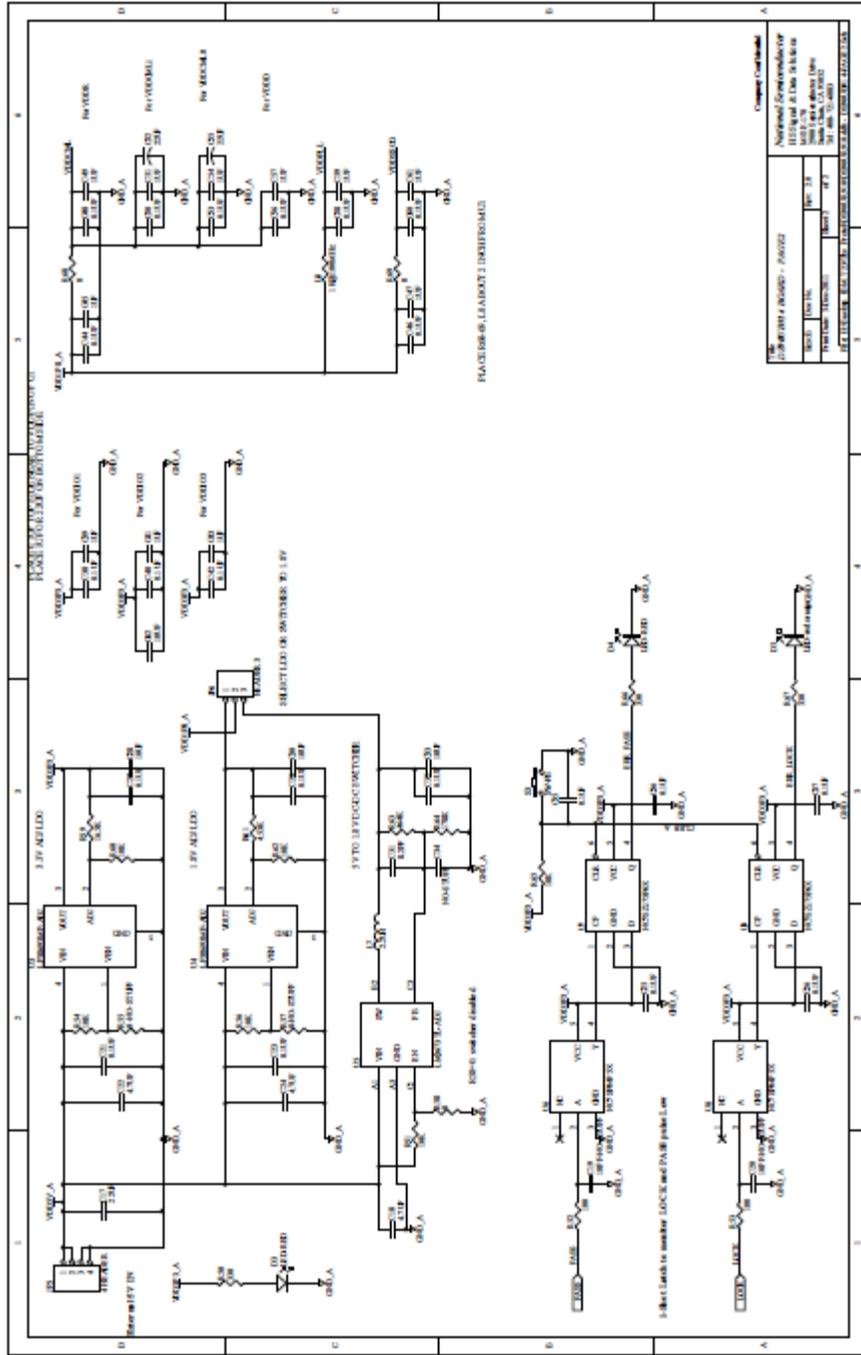
www.corelis.com/products/I2C-Analyzer.htm

Appendix

DS90UB913Q EVK Schematic





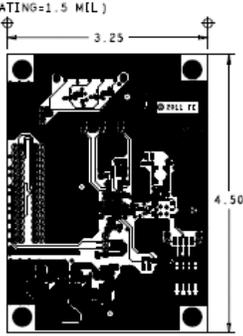


DS90UB913Q PCB Layout

LAYER STACK-UP
THIS IS A 6 LAYER BOARD

LAYER 1	TOP SIDE SOLDER MASK	0.50 MILS	→ TOP	(Cu + PLATING=1.5 MIL)
LAYER 2		5.00 MILS	→ GND-1	1.30 MILS
LAYER 3		4.00 MILS	→ VCC	1.30 MILS
LAYER 4		24.00 MILS	→ GND-2	1.30 MILS
LAYER 5		10.00 MILS	→ SIG	0.70 MILS
LAYER 6	BOTTOM SIDE SOLDER MASK	0.50 MILS	→ BOTTOM	(Cu + PLATING=1.5 MIL)

FIGURE	SIZE	TOLERANCE	PLATED	QTY
*	8.0	+3.0/-3.0	PLATED	9
*	10.0	+3.0/-3.0	PLATED	217
*	15.0	+3.0/-3.0	PLATED	353
*	16.0	+3.0/-3.0	PLATED	5
*	35.0	+3.0/-3.0	PLATED	4
Ø	40.0	+3.0/-3.0	PLATED	94
*	40.0	+3.0/-3.0	PLATED	1
*	40.0	+3.0/-3.0	PLATED	3
*	62.99	+3.0/-3.0	PLATED	4
*	65.0	+3.0/-3.0	PLATED	4
*	156.0	+3.0/-3.0	PLATED	4
Ø	118.0x79.0	+2.0/-2.0	NON-PLATED	2

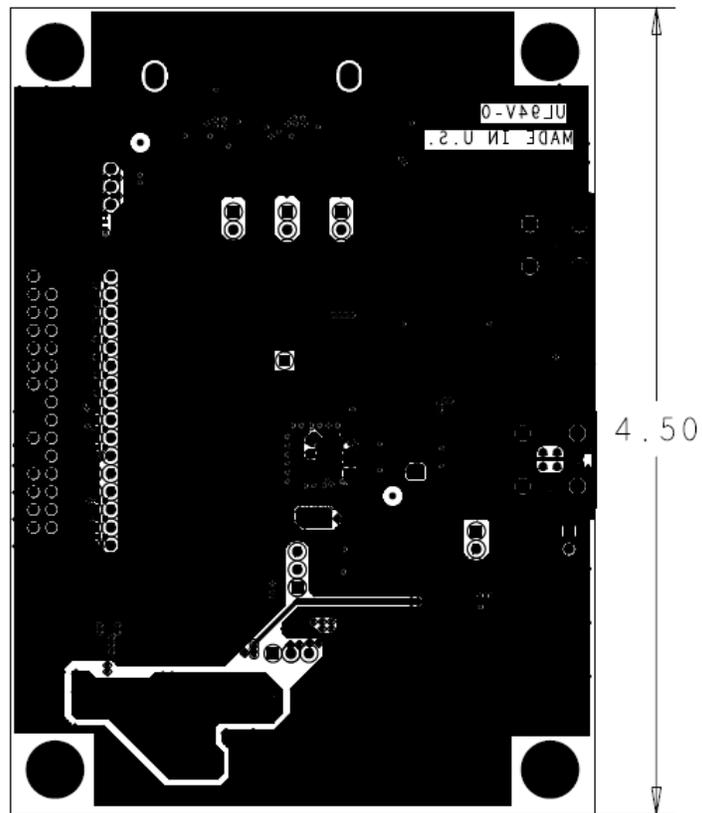
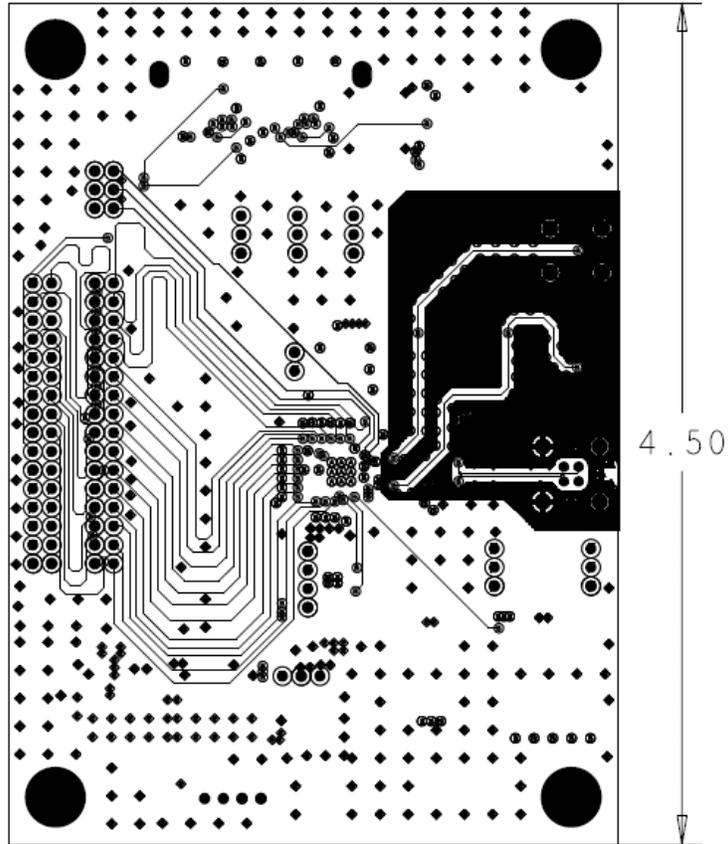


NOTES (UNLESS OTHERWISE SPECIFIED):

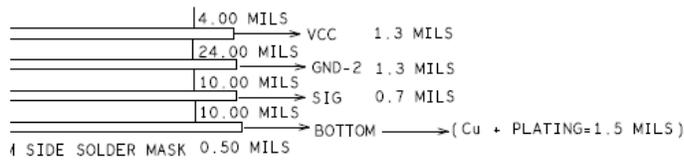
- BOARD FINISHES: 82 +/- 4 MILS
- RESISTANCE: FIM
- NUMBER OF LAYERS: 6
- SOLDERMASK: LPT GREEN
- CONDUCTIVE: WHITE DRINK CAN
- NO VENDOR LOGO OR MARK ON THE BOARD
- REMOVE THE NON-FUNCTIONAL PADS ON ALL INNER LAYERS
- PLATE IN: 100% (MINIMUM HOLE)
- MATCHING MARK AND TRENCH SHALL NOT EXCEED .005 PER DRILL
- ANY CHANGES MADE BY THE PCB FABRICATOR TO THE PLAN OR THE BOARD FILED MUST BE APPROVED BY FACTRON
- ROUND ALL SHARP EDGES
- BOARD DIMENSIONS ARE IN INCHES
- Ø HOLE TRACES INDICATED TO 90% +/- 5 OHM SIGNALS BUILT EXPANSION ON TOP LAYER AND SIGNAL LAYER
- Ø/Ø TRACES REQUIRE 100 OHM +/- 5 OHM DIFFERENTIAL IMPEDANCE ON TOP LAYER
- Ø/Ø TRACES REQUIRE 100 OHM +/- 5 OHM DIFFERENTIAL IMPEDANCE ON SIGNAL LAYER
- THIS BOARD SHOULD BE LEAD FREE

FACTRON	
NAME: DS90UB913 DEMO BOARD	
DATE: DEC 2012	JOB: 305-PD-11-0843 Rev. 1
LAYER: 064TOP	

COMPANY: FACTRON	
2248 Truman Drive, Sunnyvale Ca 94089	
909 747 1837 (phone) 408 747 2238 (fax)	
TITLE: DS90UB913 DEMO BOARD	
SIZE	FSCM NO
	DWG NO
	305-PD-11-0843
SCALE	SHEET

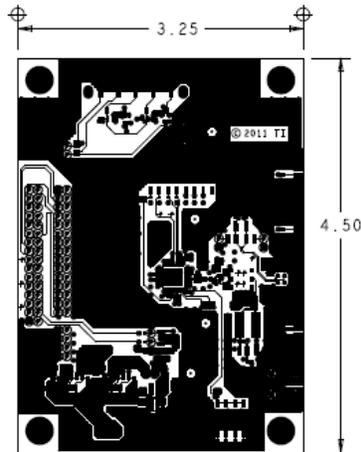


DS90UB914Q EVK Layout



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

E	TOLERANCE	PLATED	QTY
0	+3.0/-3.0	PLATED	9
0	+3.0/-3.0	PLATED	335
0	+3.0/-3.0	PLATED	312
0	+3.0/-3.0	PLATED	5
0	+3.0/-3.0	PLATED	4
0	+3.0/-3.0	PLATED	87
0	+3.0/-3.0	PLATED	3
0	+3.0/-3.0	PLATED	1
99	+3.0/-3.0	PLATED	4
0	+3.0/-3.0	PLATED	4
.0	+2.0/-2.0	NON-PLATED	4
79.0	+2.0/-2.0	NON-PLATED	2

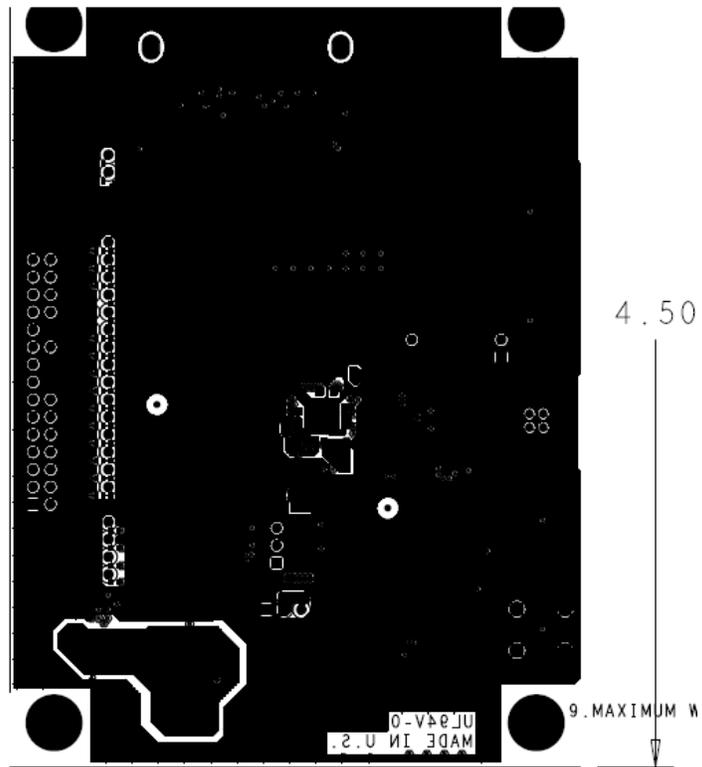
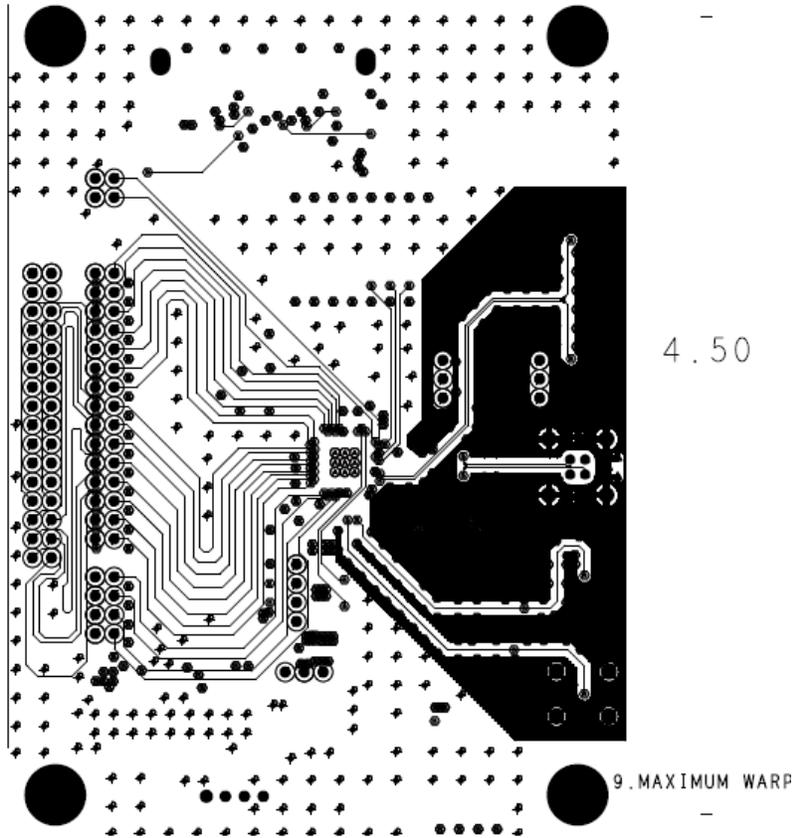


- NOTES (UNLESS OTHERWISE SPECIFIED):
1. BOARD THICKNESS : 62 +/- 4 MILS
 2. DIELECTRIC : FR4
 3. NUMBER OF LAYERS: 6.
 4. SOLDERMASK : LPC GREEN.
 5. SILKSCREEN : WHITE EPOXY INK.
 6. NO VENDOR LOGO OR NAME ON THE BOARD.
 7. REMOVE THE NON-FUNCTIONAL PADS ON ALL INNER LAYERS.
 8. PLATING : SOFT IMMERSION GOLD.
 9. MAXIMUM WARP AND TWIST SHALL NOT EXCEED .005 PER IN
 10. ANY CHANGES MADE BY THE PCB FABRICATOR TO THE FILED GERBER FILES MUST BE APPROVED BY PACTRON.
 11. DEBURR ALL SHARP EDGES.
 12. BOARD DIMENSIONS ARE IN INCHES.
 13. 8 MIL TRACES REQUIRE 50 OHM +/-5 OHM SINGLE ENDED
 14. 6/8/8 TRACES REQUIRE 100 OHM +/-5 OHM DIFFERENTIAL IMP
 15. 8/7/6 TRACES REQUIRE 100 OHM +/-5 OHM DIFFERENTIAL IMP
 16. THIS BOARD SHOULD BE LEAD FREE.

⊕

PACTRON		
NAME: DS90UB914 DEMO BRD		
DATE: DEC 2011	JOB: 305-PD-11-0844	Rev. 1
LAYER: 01E X0P		

COMPANY: .



FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general customer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range specified in datasheet.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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NOTES

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