LMP8358 Zero-Drift, Programmable Instrumentation Amplifier with Diagnostics

Check for Samples: LMP8358

FEATURES

Typical Values Unless Otherwise Noted, T_A = 25°C

- **Supply Voltage 2.7V to 5.5V**
- **Supply Current 1.8 mA**
- **Max Gain Error 0.15%**
- **Max Gain Drift 16 ppm/°C**
- **Min CMRR 110 dB**
- **Max Offset Voltage 10 µV**
- **Max Offset Voltage Drift 50 nV/°C**
- **GBW (Gain = 10) 8 MHz**
- **Max Non-Linearity 100 ppm**
- **Operating Temperature Range −40°C to 125°C**
- **Input Fault Detection**
- **SPI or Pin Configurable Modes**
- **EMIRR at 1.8GHz 92 dB**
- **14-Pin SOIC and 14-Pin TSSOP Package**

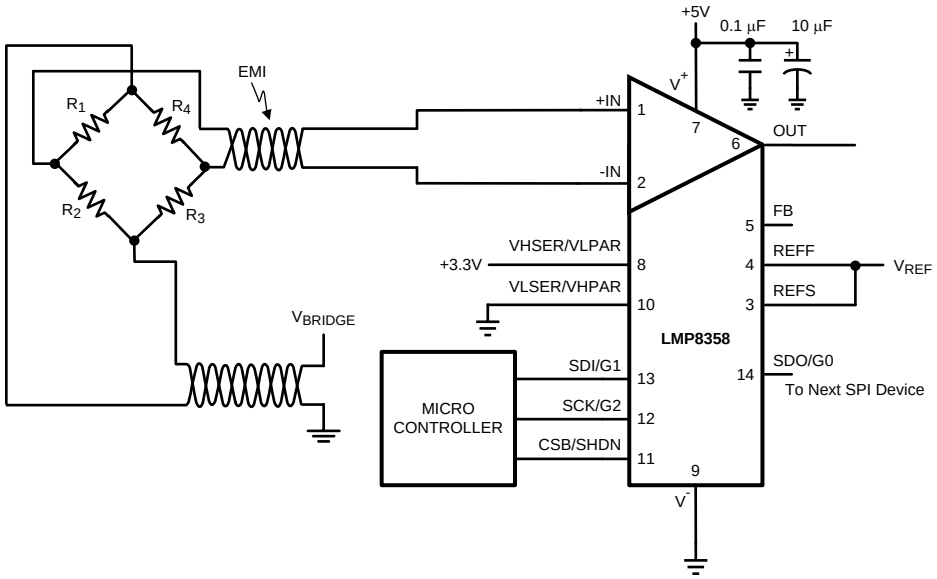
APPLICATIONS

- **Bridge Sensor Amplifier**
- **Thermopile Amplifier**
- **Portable Instrumentation**
- **Medical Instrumentation**
- **Precision Low-side Current Sensing**

DESCRIPTION

The LMP8358 is a precision programmable-gain instrumentation amplifier in TI's LMP™ precision amplifier family. Its gain can be programmed to 10, 20, 50, 100, 200, 500, or 1000 through an SPI-compatible serial interface or through a parallel interface. Alternatively, its gain can be set to an arbitrary value using two external resistors. The LMP8358 uses patented techniques to measure and continuously correct its input offset voltage, eliminating offset drift over time and temperature and the effect of 1/f noise. Its ground-sensing CMOS input features a high CMRR and low input bias currents. It is capable of sensing differential input voltages in a common-mode range that extends from 100mV below the negative supply to 1.4V below the positive supply, making it an ideal solution for interfacing with ground-referenced sensors, supply-referenced sensor bridges, and any other application requiring precision and long-term stability. Additionally, the LMP8358 includes fault detection circuitry to detect open and shorted inputs and deteriorating connections to the signal source. Other features that make the LMP8358 a versatile solution for many applications are its rail-to-rail output, low input voltage noise and high gain-bandwidth product.

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	2kV
	Machine Model	200V
	Charge Device	1kV
V_{IN} Differential (V_{+IN} − V_{-IN})		V_S
Output Short Circuit Duration (4)		
Any pin relative to V^-		6V, −0.3V
+IN, −IN, OUT Pins		V^+ +0.3V, V^- −0.3V
+IN, −IN Pins		±10 mA
Storage Temperature Range		−65°C to 150°C
Junction Temperature (5)		150°C
For soldering specifications: see product folder at www.ti.com and http://www.ti.com/lit/SNOA549.		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not ensured. For ensured specifications and the test conditions, see Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22–A115–A (ESD MM std. of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C (ESD FICDM std. of JEDEC).
(4) The short circuit test is a momentary test which applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can exceed the maximum allowable junction temperature of 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings (1)

Temperature Range		−40°C to 125°C
Supply Voltage ($V_S = V^+ – V^-$)		2.7V to 5.5V
V_{IN} Differential ($V_{+IN} – V_{–IN}$)		±100mV
Package Thermal Resistance (θ_{JA}(2))	14-Pin SOIC	145°C/W
	14-Pin TSSOP	135°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but for which specific performance is not ensured. For ensured specifications and the test conditions, see Electrical Characteristics.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

3.3V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 3.3V , V^- = 0V, $V_{REF} = V^+/2$, $V_{CM} = V^+/2$, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_{OS}	Input Offset Voltage	$V_{CM} = V^+/2$		1	10 **15**	µV
		V_{CM} = 0V		1	10 **15**	
TCV_{OS}	Input Offset Voltage Temperature Drift(3)	$V_{CM} = V^+/2$			50	nV/°C
		V_{CM} = 0V			50	
CMRR	Common Mode Rejection Ratio	$V^- – 0.1V \le V_{CM} \le V^+ – 1.4V$	110 **105**	139		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 110 dB	**−0.1**		**1.9**	V
$V_{REF}RR$	V_{REF} Rejection Ratio	$V^- + 0.1V \le V_{REFF} \le V^+ – 1.4V$	110 **105**	145		dB
PSRR	Power supply Rejection Ratio	$2.7V \le V^+ \le 5.5V$	112 **105**	138		dB
EMIRR	Electro Magnetic Interference Rejection Ratio	+IN / −IN, V_{RF} = 100 mV_P, f = 900 MHz		83		dB
		+IN / −IN, V_{RF} = 100 mV_P, f = 1800 MHz		93		
Z_{INDM}	Differential Input Impedance			50||1		MΩ ‖ pF
Z_{INCM}	Common Mode Input Impedance			50||1		MΩ ‖ pF
V_{INDM}	Differential Mode Input Voltage				±100	mV
I_B	Input Bias Current			0.006	1.2 **2**	nA
I_{OS}	Input Offset Current			0.1	112	pA
e_n	Input Voltage Noise Density	Gain = 10, f = 1 kHz		27		nV/√Hz
		Gain = 20, f = 1 kHz		31		
		Gain = 50, f = 1 kHz		28		
		Gain = 100, f = 1 kHz		27		
		Gain = 200, f = 1 kHz		28		
		Gain = 500, f = 1 kHz		28		
		Gain = 1000, f = 1 kHz		27		
		Gain = External, f = 1 kHz		27		

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values indicate the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The offset voltage average drift is determined by dividing the value of V_{OS} at the temperature extremes by the total temperature change.

3.3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 3.3V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
e_n	Input Voltage Noise	Gain = 10, 0.1 Hz < f < 10 Hz		0.9		μV_{PP}
		Gain = 20, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 50, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 100, 0.1 Hz < f < 10 Hz		0.7		
		Gain = 200, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 500, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 1000, 0.1 Hz < f < 10 Hz		0.6		
		Gain = External, 0.1 Hz < f < 10 Hz		0.6		
I_n	Input Current Noise Density	Gain = 100, f = 1 kHz		0.5		$pA/\sqrt{Hz}$
G_E	Gain Error	Gain = 10, 20, 50, 100, 200, 500 V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03	0.1 **0.15**	%
G_E	Gain Error	Gain = 1000 V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03	0.15 **0.25**	%
G_E	Gain Error Contribution from Chip	V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03		%
	Gain Error Temperature Coefficient	For all gain settings (internal and external), V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		3	16	ppm/°C
NL	Non-Linearity			3.3	100	ppm
GBW	Gain Bandwidth	COMP[2:0] =000b, Gain > 10		8		MHz
		COMP[2:0] = 001b, Gain > 30		24		
		COMP[2:0] = 010b, Gain > 200		80		
		COMP[2:0] = 011b, Gain > 300		240		
		COMP[2:0] = 1xxb, Gain > 1		0.8		
BW	−3 dB Bandwidth	Gain = 10, COMP[2:0] = 000b		900		kHz
		Gain = 10, COMP[2:0] = 1xxb		70		
		Gain = 20, COMP[2:0] = 000b		400		
		Gain = 20, COMP[2:0] = 1xxb		37		
		Gain = 50, COMP[2:0] = 001b		490		
		Gain = 50, COMP[2:0] = 1xxb		16		
		Gain = 100, COMP[2:0] = 010b		680		
		Gain = 100, COMP[2:0] = 1xxb		8		
		Gain = 200, COMP[2:0] = 010b		195		
		Gain = 200, COMP[2:0] = 1xxb		4		
		Gain = 500, COMP[2:0] = 011b		130		
		Gain = 500, COMP[2:0] = 1xxb		1.5		
		Gain = 1000, COMP[2:0] = 011b		89		
		Gain = 1000, COMP[2:0] = 1xxb		0.8		
SR	Slew Rate(4)	COMP[2:0] = 000b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		1.6		V/µs
		COMP[2:0] = 001b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		3.8		
		COMP[2:0] = 010b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		6.5		
		COMP[2:0] = 011b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		9.3		
		COMP[2:0] = 1xxb, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		0.17		

(4) Slew rate is the average of the rising and falling slew rates.

3.3V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 3.3V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
t_s	0.01% Settling Time	2 V Step, C_L = 10 pF, COMP[2:0] = 011b		4		µs
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2			32 **40**	mV from top rail
		R_L = 10 kΩ to V^+/2			12 **17**	
		R_L > 1 MΩ to V^+/2			7 **12**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2			28 **38**	mV from bottom rail
		R_L = 10 kΩ to V^+/2			12 **17**	
		R_L > 1 MΩ to V^+/2			8 **13**	
I_{OUT}	Output Current Sourcing	V_{OUT} tied to V^+/2	21 **15**	28		mA
	Output Current Sinking	V_{OUT} tied to V^+/2	32 **25**	37		
I_S	Supply Current	Fault detection off, $V_{IN\ DIFF}$ = 0V		1.8	2.1	mA
		Fault detection on, $V_{IN\ DIFF}$ = 0V		1.9	2.2	mA
		in Shutdown		0.014	1	µA
T_{SD_ON}	Turn-on time from Shutdown			85		µs
PS_E	Prescaler Error (Offset + Gain Error)	V_{CM} = V^+/2		5	15	mV
	Prescaler Gain Factor			0.02		V/V
I_{TEST}	Fault Detection: Test Current	Setting 1 (CUR[2:0] = 001b), V_{CM} < V^+ − 1.15V		10		nA
		Setting 2 (CUR[2:0] = 010b), V_{CM} < V^+ − 1.15V		100		nA
		Setting 3 (CUR[2:0] = 011b), V_{CM} < V^+ − 1.15V		1		µA
		Setting 4 (CUR[2:0] = 100b), V_{CM} < V^+ − 1.15V		10		µA
		Setting 5 (CUR[2:0] = 101b), V_{CM} < V^+ − 1.15V		100		µA

5.0V Electrical Characteristics

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
V_{OS}	Input Offset Voltage	V_{CM} = V^+/2		0.9	10 **15**	µV
		V_{CM} = 0V		0.9	10 **15**	
TCV_{OS}	Input Offset Voltage Temperature Drift[3]	V_{CM} = V^+/2			50	nV/°C
		V_{CM} = 0V			50	

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values indicate the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) The offset voltage average drift is determined by dividing the value of V_{OS} at the temperature extremes by the total temperature change.

5.0V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
CMRR	Common Mode Rejection Ratio	V^- − 0.1V ≤ V_{CM} ≤ V^+ − 1.4V	116 **105**	142		dB
V_{REF}RR	V_{REF} Rejection Ratio	V^- + 0.1V ≤ V_{REFF} ≤ V^+ − 1.4V	115 **105**	150		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 115 dB	**−0.1**		**3.6**	V
PSRR	Power supply Rejection Ratio	2.7V ≤ V^+ ≤ 5.5V	112 **105**	138		dB
EMIRR	Electro Magnetic Interference Rejection Ratio	+IN / −IN, V_{RF} = 100 mV_P, f = 900 MHz		83		dB
		+IN / −IN, V_{RF} = 100 mV_P, f = 1800 MHz		93		
Z_{INDM}	Differential Input Impedance			50||1		MΩ ‖ pF
Z_{INCM}	Common Mode Input Impedance			50||1		MΩ ‖ pF
V_{INDM}	Differential Mode Input Voltage				±100	mV
I_B	Input Bias Current			0.006	1.2 **2**	nA
I_{OS}	Input Offset Current			0.2	113	pA
e_n	Input Voltage Noise Density	Gain = 10, f = 1 kHz		25		nV/√Hz
		Gain = 20, f = 1 kHz		28		
		Gain = 50, f = 1 kHz		26		
		Gain = 100, f = 1 kHz		25		
		Gain = 200, f = 1 kHz		28		
		Gain = 500, f = 1 kHz		26		
		Gain = 1000, f = 1 kHz		25		
		Gain = External, f = 1 kHz		25		
e_n	Input Voltage Noise	Gain = 10, 0.1 Hz < f < 10 Hz		0.7		μV_{PP}
		Gain = 20, 0.1 Hz < f < 10 Hz		0.7		
		Gain = 50, 0.1 Hz < f < 10 Hz		0.5		
		Gain = 100, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 200, 0.1 Hz < f < 10 Hz		0.6		
		Gain = 500, 0.1 Hz < f < 10 Hz		0.5		
		Gain = 1000, 0.1 Hz < f < 10 Hz		0.6		
		Gain = External, 0.1 Hz < f < 10 Hz		0.6		
I_n	Input Current Noise Density	Gain = 100, f = 1 kHz		0.5		pA/√Hz
G_E	Gain Error	Gain = 10, 20, 50, 100, 200, 500 V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03	0.1 **0.15**	%
G_E	Gain Error	Gain = 1000 V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03	0.15 **0.25**	%
G_E	Gain Error Contribution from chip	V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		0.03		%
	Gain Error Temperature Coefficient	For all gain settings (internal and external), V_{OUT} = V_{REF} + 1V and V_{OUT} = V_{REF} − 1V		3	16	ppm/°C
NL	Non-Linearity			3	100	ppm
GBW	Gain Bandwidth	COMP[2:0] = 000b, Gain > 10		8		MHz
		COMP[2:0] = 001b, Gain > 100		24		
		COMP[2:0] = 010b, Gain > 200		80		
		COMP[2:0] = 011b, Gain > 500		240		
		COMP[2:0] = 1xxb, Gain => 1		0.8		

5.0V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
BW	−3 dB Bandwidth	Gain = 10, COMP[2:0] = 000b		930		kHz
		Gain = 10, COMP[2:0] = 1xxb		74		
		Gain = 20, COMP[2:0] = 000b		385		
		Gain = 20, COMP[2:0] = 1xxb		37		
		Gain = 50, COMP[2:0] = 001b		460		
		Gain = 50, COMP[2:0] = 1xxb		16		
		Gain = 100, COMP[2:0] = 010b		640		
		Gain = 100, COMP[2:0] = 1xxb		8		
		Gain = 200, COMP[2:0] = 010b		195		
		Gain = 200, COMP[2:0] = 1xxb		4		
		Gain = 500, COMP[2:0] = 011b		130		
		Gain = 500, COMP[2:0] = 1xxb		1.5		
		Gain = 1000, COMP[2:0] = 011b		89		
		Gain = 1000, COMP[2:0] = 1xxb		0.8		
SR	Slew Rate(4)	COMP[2:0] = 000b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		1.7		V/µs
		COMP[2:0] = 001b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		5.0		
		COMP[2:0] = 010b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		9.0		
		COMP[2:0] = 011b, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		11.0		
		COMP[2:0] = 1xxb, 10% to 90% of Step, V_{OUT} = 2 V_{PP}		0.16		
t_s	0.01% Settling Time	2 V Step, C_L = 10 pF, COMP[2:0] = 011b		4		µs
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to V^+/2			52 **62**	mV from top rail
		R_L = 10 kΩ to V^+/2			22 **30**	
		R_L > 1 MΩ to V^+/2			12 **17**	
	Output Voltage Swing Low	R_L = 2 kΩ to V^+/2			42 **55**	mV from bottom rail
		R_L = 10 kΩ to V^+/2			16 **22**	
		R_L > 1 MΩ to V^+/2			12 **17**	
I_{OUT}	Output Current Sourcing	V_{OUT} tied to V^+/2	23 **16**	31		mA
	Output Current Sinking	V_{OUT} tied to V^+/2	34 **30**	41		
I_S	Supply Current	Fault detection off, $V_{IN\ DIFF}$ = 0V		1.8	2.1	mA
		Fault detection on, $V_{IN\ DIFF}$ = 0V		1.9	2.2	mA
		in Shutdown		0.006	1	µA
T_{SD_ON}	Turn-on time from Shutdown			85		µs
PS_E	Prescaler Error (Offset + Gain Error)	V_{CM} = V^+/2		5	8	mV
	Prescaler Gain Factor			0.02		V/V

(4) Slew rate is the average of the rising and falling slew rates.

5.0V Electrical Characteristics (continued)

Unless otherwise specified, all limits are ensured for T_A = 25°C. V^+ = 5.0V , V^- = 0V, V_{REF} = V^+/2, V_{CM} = V^+/2, R_L = 10 kΩ to V_{REF}, C_L = 10 pF; Serial Control Register: G[2:0] = 110b (Gain = 1000x), COMP[2:0] = 000b, MUX[1:0] = 00b, POL, SHDN, FILT, PIN = 0b, CUR[2:0] = 000b. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
I_{TEST}	Fault Detection: Test Current	Setting 1 (CUR[2:0] = 001b), V_{CM} < V^+ − 2.25V		10		nA
		Setting 2 (CUR[2:0] = 010b), V_{CM} < V^+ − 2.25V		100		nA
		Setting 3 (CUR[2:0] = 011b), V_{CM} < V^+ − 2.25V		1		µA
		Setting 4 (CUR[2:0] = 100b), V_{CM} < V^+ − 2.25V		10		µA
		Setting 5 (CUR[2:0] = 101b), V_{CM} < V^+ − 2.25V		100		µA

Electrical Characteristics (Serial Interface)

Unless otherwise specified, all limits ensured for T_A = 25°C, $V^+ - V^- \geq$ 2.7V, $V^+ \geq$ VHSER/VLPAR, $V^- \leq$ VLSER/VHPAR, V_D = (VHSER/VLPAR) − (VLSER/VHPAR) ≥ 2.5V.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
V_{IL}	Input Logic Low Threshold				0.3 × V_D	V
V_{IH}	Input Logic High Threshold		0.7 × V_D			V
V_{OL}	Output Logic Low Threshold	I_{SDO} = 2mA			0.2	V
V_{OH}	Output Logic High Threshold	I_{SDO} = 2mA	V_D − 0.2V			
I_{SDO}	Output Source Current, SDO	V_D = 3.3V or 5.0V, CSB = 0V, V_{OH} = V^+ – 0.7V	−2			mA
	Output Sink Current, SDO	V_D = 3.3V or 5.0V, CSB = 0V, V_{OL} = 1.0V	2			
I_{OZ}	Output Tri-state Leakage Current, SDO	V_D = 3.3V or 5.0V, CSB = V_D = 3.3V or 5V			±1	µA
t_1	High Period, SCK	(3)	100			ns
t_2	Low Period, SCK	(3)	100			ns
t_3	Set Up Time, CSB to SCK	(3)	50			ns
t_4	Set Up Time, SDI to SCK	(3)	30			ns
t_5	Hold Time, SCK to SDI	(3)	10			ns
t_6	Prop. Delay, SCK to SDO	(3)			60	ns
t_7	Hold Time, SCK Transition to CSB Rising Edge	(3)	50			ns
t_8	CSB Inactive	(3)	50			ns
t_9	Prop. Delay, CSB to SDO Active	(3)			50	ns
t_{10}	Prop. Delay, CSB to SDO Inactive	(3)			50	ns
t_{11}	Hold Time, SCK Transition to CSB Falling Edge	(3)	10			ns
t_r/t_f	Signal Rise and Fall Times	(3)	1.5		5	ns

(1) All limits are specified by testing or statistical analysis.
(2) Typical Values indicate the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(3) Load for these tests is shown in the Timing Diagram Test Circuit.

Connection Diagram

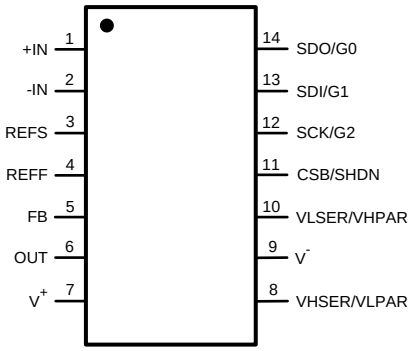


Figure 1. 14-Pin SOIC/ 14-Pin TSSOP
Top View

Pin Descriptions

Pin Name	Communication Mode	
	Serial	**Parallel**
+IN	Positive Input	
−IN	Negative Input	
REFS	Reference Sense	
REFF	Reference Force	
FB	Feedback	
OUT	Output	
V^+	Positive Supply	
VHSER/VLPAR	Set High	Set Low
V^-	Negative Supply	
VLSER/VHPAR	Set Low	Set High
CSB/SHDN	Chip Select	Shutdown (Active High)
SCK/G2	Serial Clock	Gain (MSB)
SDI/G1	Serial Data In	Gain
SDO/G0	Serial Data Out	Gain (LSB)

Block Diagram

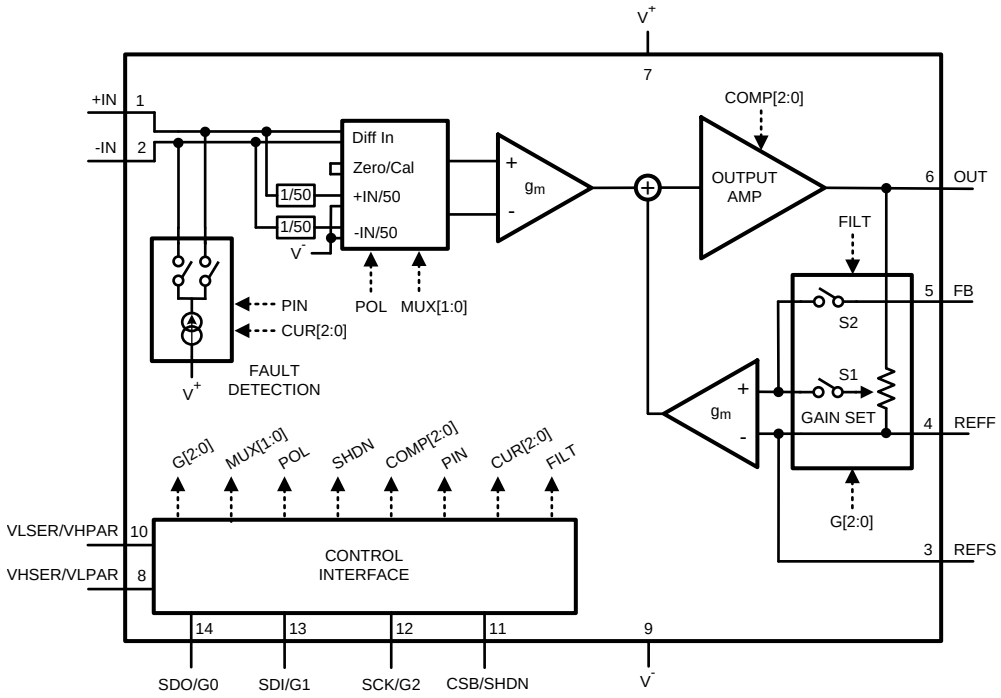


Figure 2. 14-Pin SOIC/ 14-Pin TSSOP

Timing Diagrams

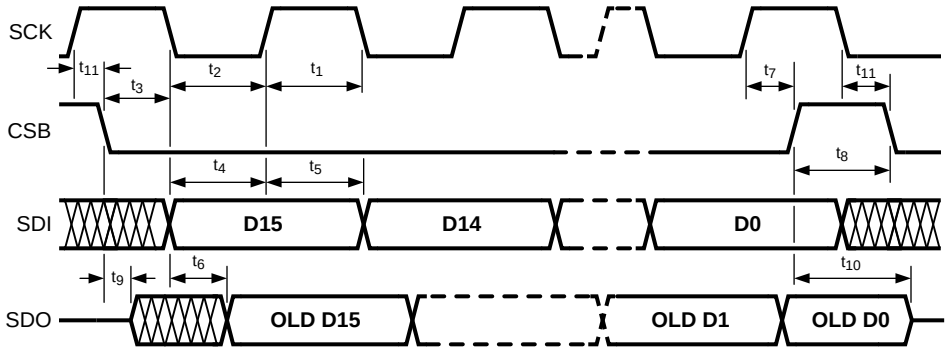


Figure 3. SPI Timing Diagram

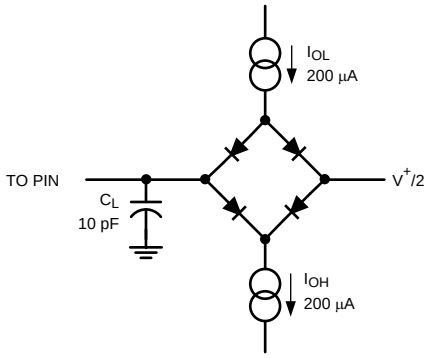


Figure 4. Timing Diagram Test Circuit

Typical Performance Characteristics

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

Gain vs. Frequency for Various COMP Settings

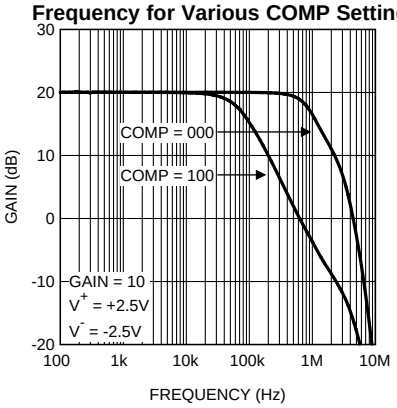


Figure 5.

Gain vs. Frequency for Various COMP Settings

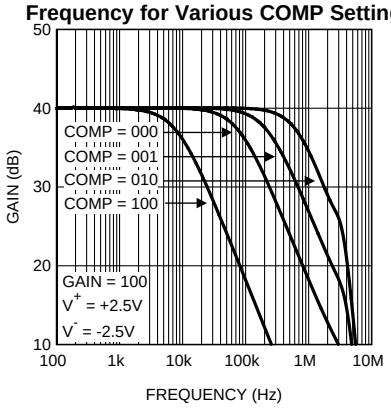


Figure 6.

Gain vs. Frequency for Various COMP Settings

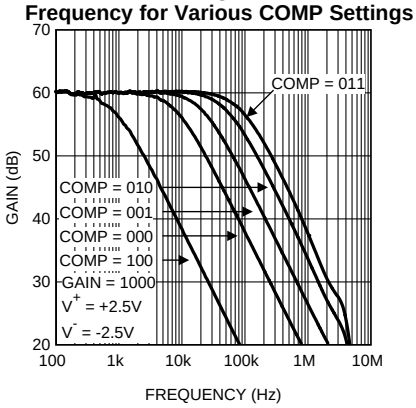


Figure 7.

Gain vs. Frequency for Various Cap Loads

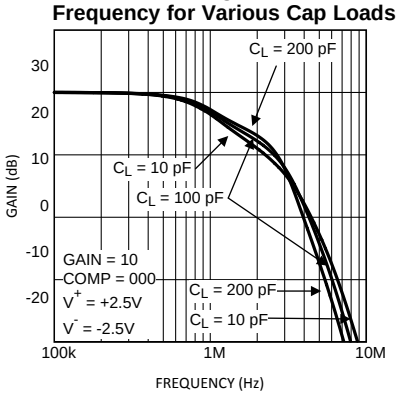


Figure 8.

Gain vs. Frequency for Various Cap Loads

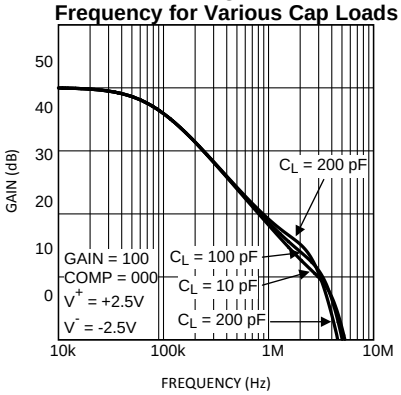


Figure 9.

Gain Error vs. Common Mode Voltage, V_S = 5V

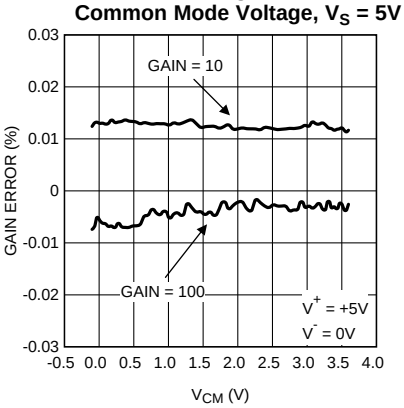


Figure 10.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

Gain Error vs. Common Mode Voltage, V_S = 3.3V

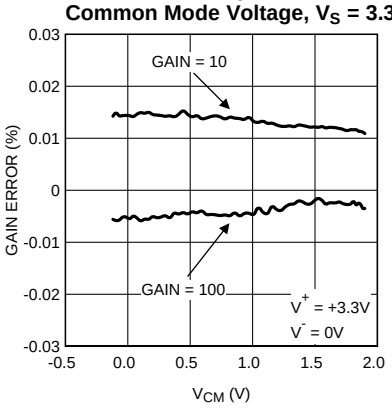


Figure 11.

Gain Error Distribution, Gain = 10, V_S = 3.3V

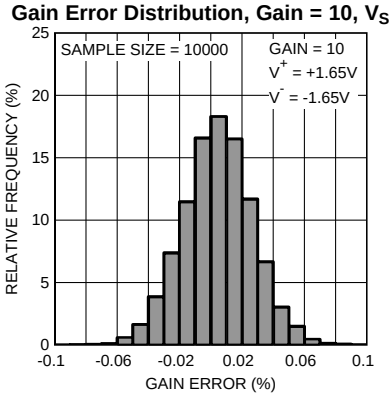


Figure 12.

Gain Error Distribution, Gain = 100, V_S = 3.3V

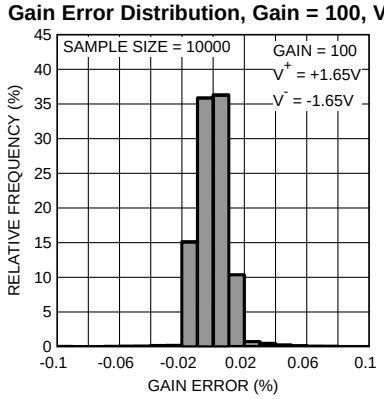


Figure 13.

Gain Error Distribution, Gain = 1000, V_S = 3.3V

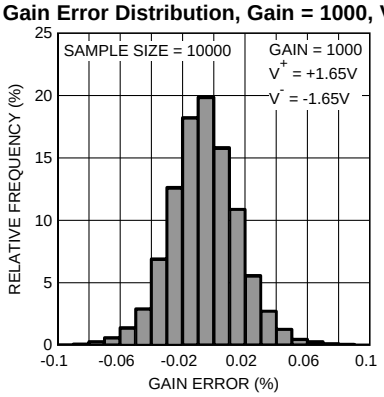


Figure 14.

V_{OS} Distribution, V_S = 3.3V

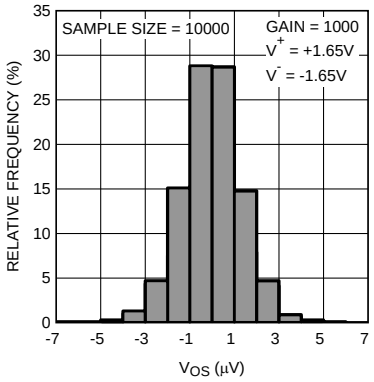


Figure 15.

V_{OS} Distribution, V_S = 5.0V

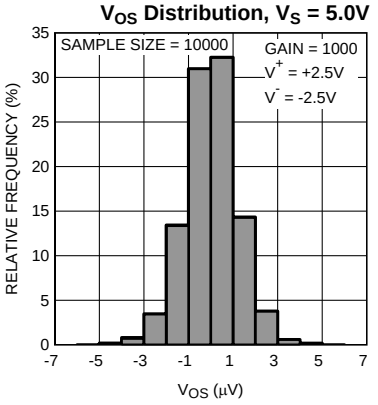


Figure 16.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

TCV_{OS} Distribution, V_S = 3.3V

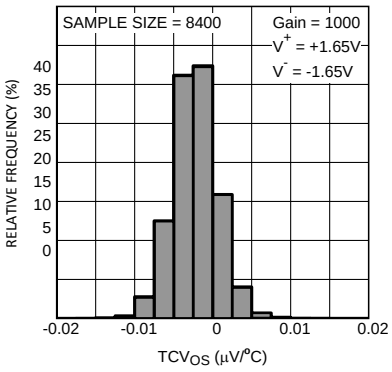


Figure 17.

TCV_{OS} Distribution, V_S = 5V

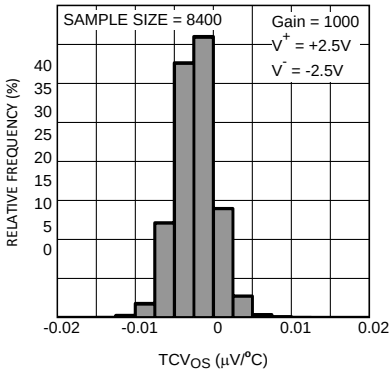


Figure 18.

V_{OS} vs. V_{CM}, V_S = 3.3V

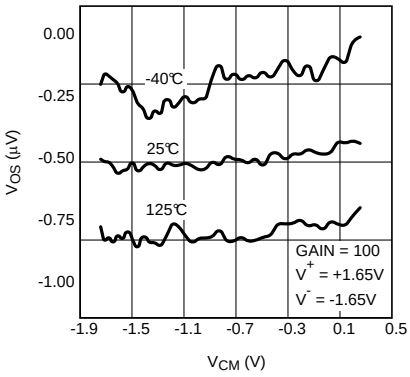


Figure 19.

V_{OS} vs. V_{CM}, V_S = 3.3V

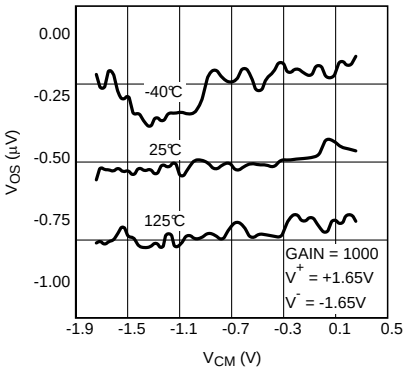


Figure 20.

V_{OS} vs. V_{CM}, V_S = 5.0V

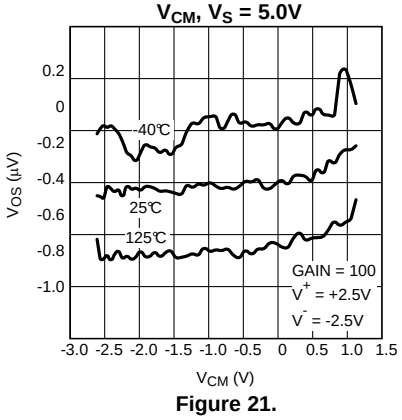


Figure 21.

V_{OS} vs. V_{CM}, V_S = 5.0V

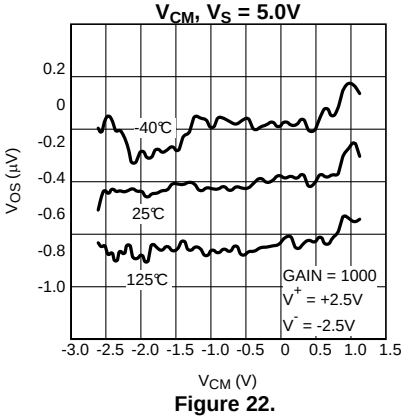


Figure 22.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

V_{OS} vs. V_{REF}, V_S = 3.3V

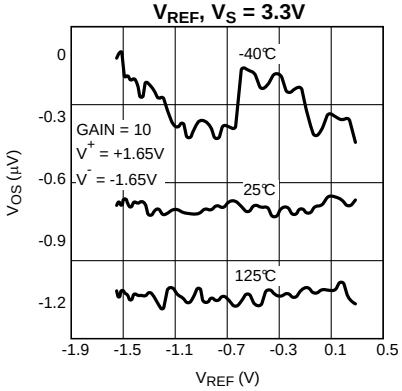


Figure 23.

CMRR vs. Frequency

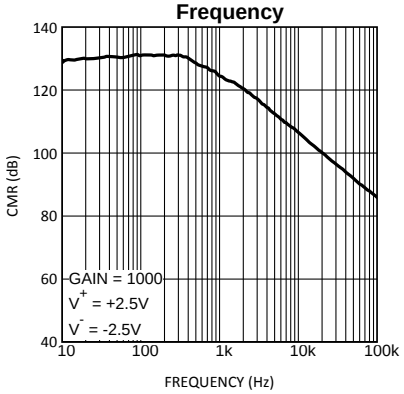


Figure 24.

CMRR vs. Frequency

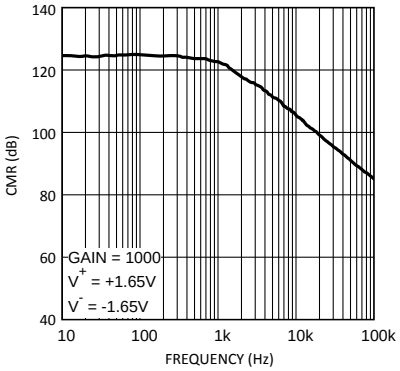


Figure 25.

PSRR vs. Frequency

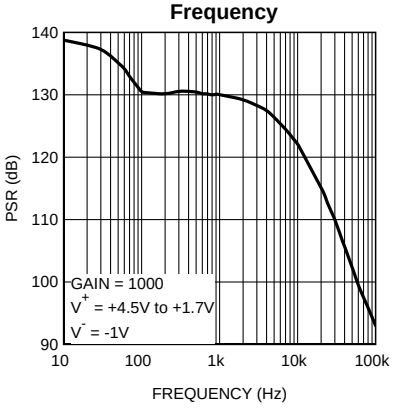


Figure 26.

Voltage Noise vs. Time

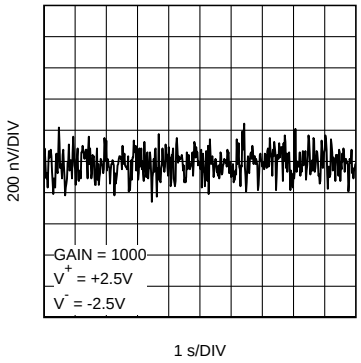


Figure 27.

Voltage Noise vs. Frequency

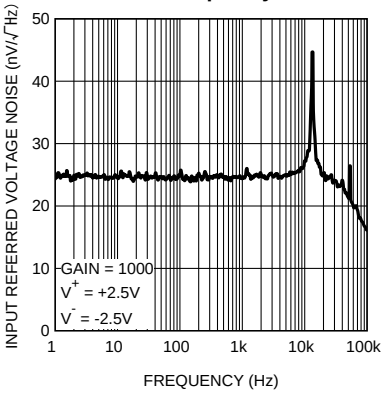


Figure 28.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

Small Signal Step Response for Various COMP Settings

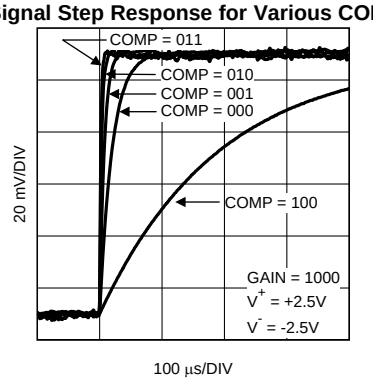


Figure 29.

Small Signal Step Response for Various COMP Settings

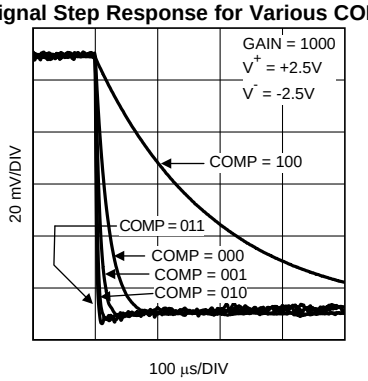


Figure 30.

Large Signal Step Response for Various COMP Settings

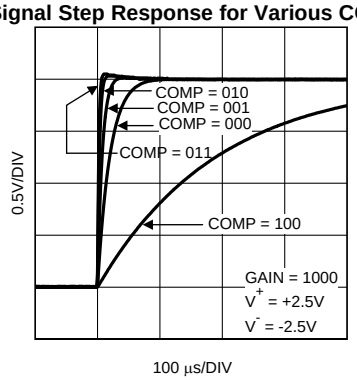


Figure 31.

Large Signal Step Response for Various COMP Settings

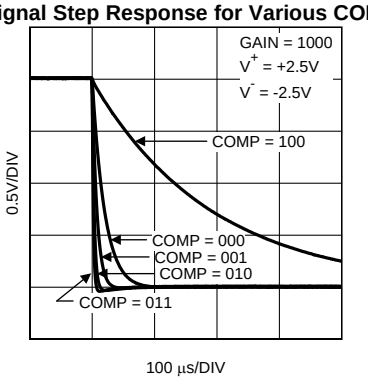


Figure 32.

Positive Overshoot vs. C_{LOAD}

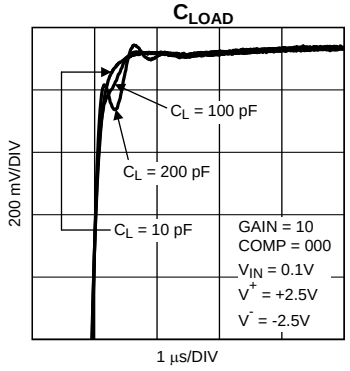


Figure 33.

Supply Current vs. Supply Voltage

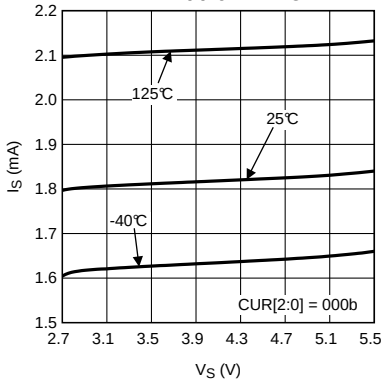


Figure 34.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

Input Bias Current vs. V_{CM}, V_S = 3.3V

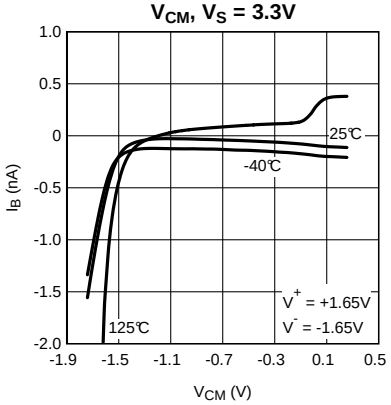


Figure 35.

Input Bias Current vs. V_{CM}, V_S = 5.0V

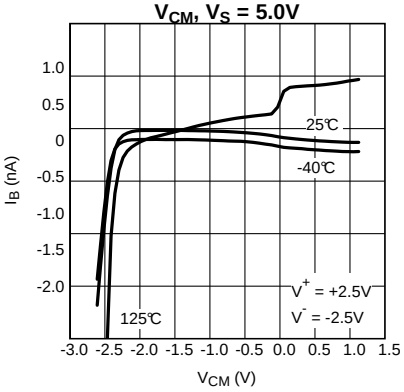


Figure 36.

THD+N vs. Frequency

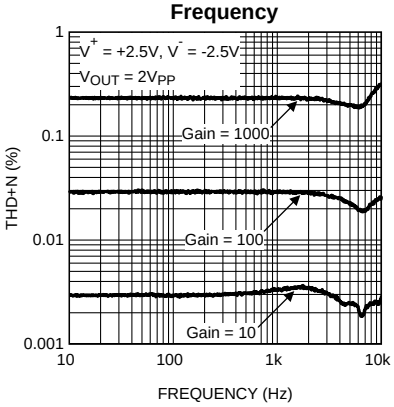


Figure 37.

THD+N vs. V_{OUT}

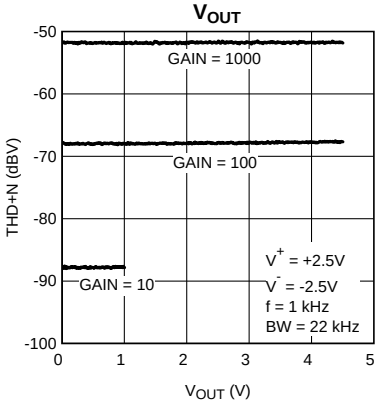


Figure 38.

I_{TEST1} vs. V_{CM}

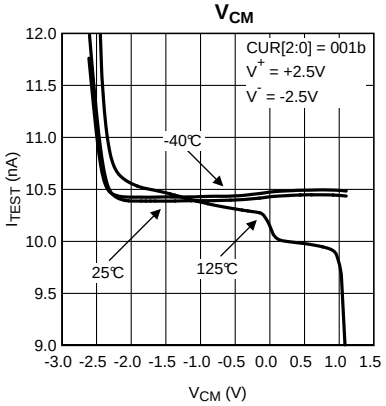


Figure 39.

I_{TEST2} vs. V_{CM}

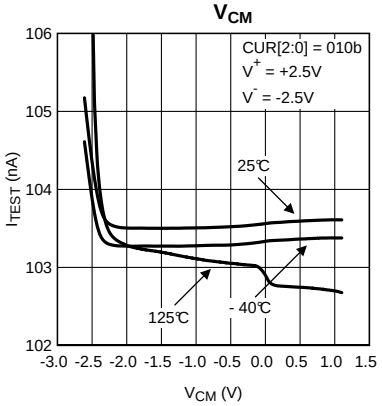


Figure 40.

Typical Performance Characteristics (continued)

V^+ = 3.3V and T_A = 25°C unless otherwise noted.

I_{TEST3} vs. V_{CM}

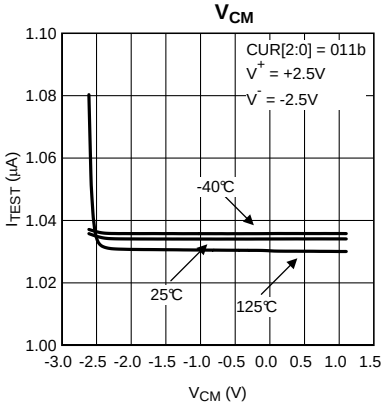


Figure 41.

I_{TEST4} vs. V_{CM}

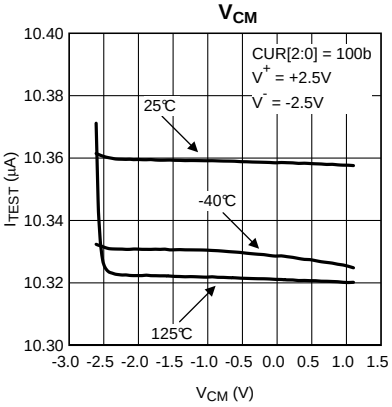


Figure 42.

I_{TEST5} vs. V_{CM}

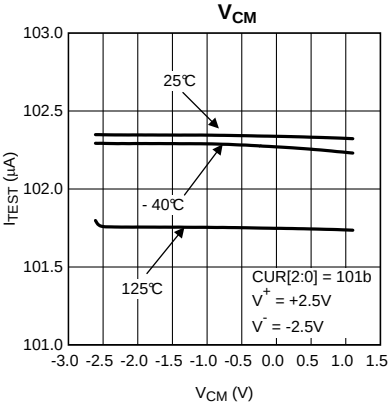


Figure 43.

Output Swing High vs. Supply Voltage

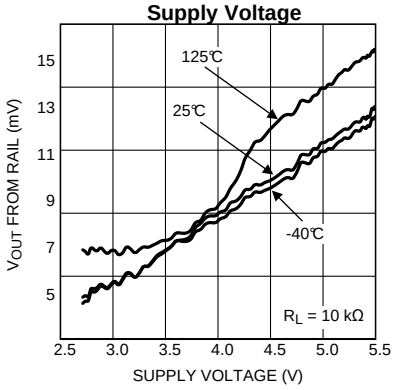


Figure 44.

Output Swing Low vs. Supply Voltage

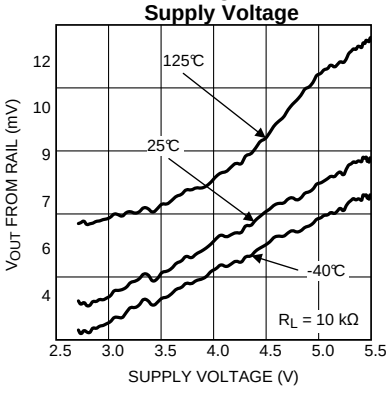


Figure 45.

EMIRR IN+ vs. Frequency

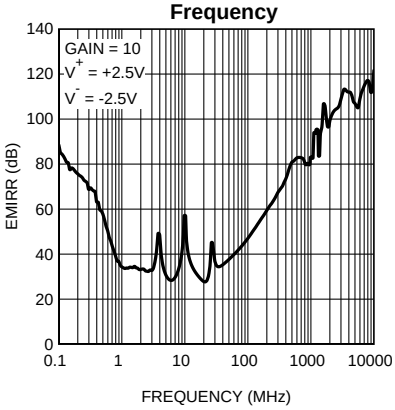


Figure 46.

APPLICATION INFORMATION

INTRODUCTION

The LMP8358 is a precision programmable gain instrumentation amplifier. Its gain can be programmed to 10, 20, 50, 100, 200, 500 or 1000 through an SPI-compatible serial interface or through a parallel interface. Alternatively, its gain can be set to an arbitrary value using external resistors. Note that at low gains the dynamic range is limited by the maximum input differential voltage of ±100mV. The LMP8358 uses patented techniques to measure and continuously correct its input offset voltage, eliminating offset drift over time and temperature, and the effect of 1/f noise. Its ground sensing CMOS input features a high CMRR and low input bias currents. It is capable of sensing differential input voltages in a common-mode range that extends from 100 mV below the negative supply to 1.4V below the positive supply, making it an ideal solution for interfacing with ground-referenced sensors, supply-referenced sensor bridges, and any other application requiring precision and long term stability. Additionally, the LMP8358 includes fault detection circuitry, so open and shorted inputs can be detected, as well a deteriorating connection to the signal source. Other features that make the LMP8358 a versatile solution for many applications are: its rail-to-rail output, low input voltage noise and high gain-bandwidth product.

TRANSIENT RESPONSE TO FAST INPUTS

The LMP8358 is a current-feedback instrumentation amplifier that consists of two auto-zeroed input stages. These two input stages are operated in a ping-pong fashion: as one stage is auto-zeroed the other stage provides the path between the input pins and the output. The auto-zeroing decreases offset, offset drift, and 1/f noise while the ping-pong architecture provides a continuous path between the input and the output. As with all devices that use auto-zeroing, care must be taken with the signal frequency used with the device. On-chip continuous auto-zero correction circuitry eliminates the 1/f noise and significantly reduces the offset voltage and offset voltage drift; all of which are very low-frequency events. For slow-changing sensor signals, below 2kHz, this correction is transparent. Higher-frequency signals as well as fast changing edges will show a settling and ramping time lasting about 1µs. Like all auto-zeroing devices, if the input frequency is above the auto-zero frequency, aliasing will occur. This can occur both at the auto-zeroing frequency of about 12kHz and the ping-pong frequency of about 50kHz. If needed, a low-pass filter should be placed on the output of the LMP8358 to filter out this disturbance.

COMMUNICATION WITH THE PART AND REGISTER DESCRIPTION

The LMP8358 supports a serial and a parallel digital interface mode as shown in Figure 47 and Figure 48.

Parallel user mode Gain is set using G0, G1 and G2 pins. The shutdown mode can be activated by asserting SHDN. Fault detection features are unavailable.

Serial user mode The part is SPI-programmable through SDI, SCK, SDO and CSB. All features are available.

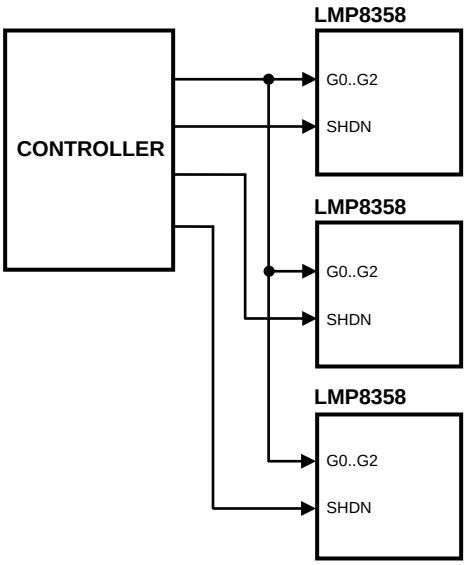


Figure 47. (A) Communication with LMP8358 in Parallel Mode

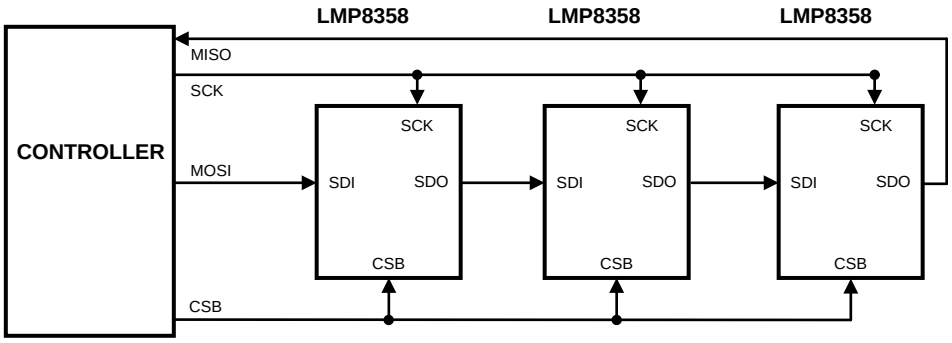


Figure 48. (B) Communication with LMP8358 in Serial Mode

Communication Mode Selection

The interface mode is determined by the two interface level pins VLSER/VHPAR and VHSER/VLPAR.

VLSER/VHPAR < VHSER/VLPAR Serial Interface. VLSER= Logic low level, VHSER = Logic high level.

VLSER/VHPAR > VHSER/VLPAR Parallel interface. VLPAR = Logic low level, VHPAR = Logic high level.

The levels applied to the VLSER/VHPAR and VHSER/VLPAR pins should be between the V^+ and V^- levels as shown in Figure 49.

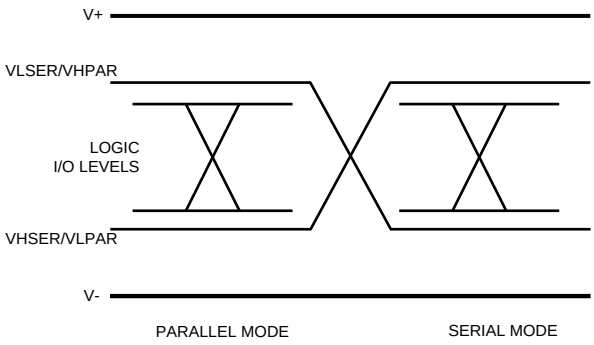


Figure 49. Communication Mode Selection.

PARALLEL CONTROL INTERFACE MODE

The LMP8358 is put into Parallel Mode by setting VLSER/VHPAR > VHSER/VLPAR. The register in the LMP8358 does not control the settings of the LMP8358 in this mode. Gain and shutdown are set by placing a high or low logic level on pins 11 (SHDN), 12 (G2), 13 (G1), and 14 (G0), as shown in Table 1 and Table 2. The logic high and low levels are defined by the voltages on the VLSER/VHPAR and VHSER/VLPAR pins. See the START UP AND POWER ON RESET section for power on requirements when using the parallel mode.

Table 1. Function of Digital IO Pins, Parallel Mode

Pin Name	Description
G0	Gain setting (LSB)
G1	Gain setting
G2	Gain setting (MSB)
SHDN	Shutdown (Active High)
VHPAR	Positive logic level
VLPAR	Negative logic level

Table 2. Pin Levels for Setting Gain, Parallel Mode

G2	G1	G0	Gain Setting	Bandwidth	Compen-sation Setting (Auto-matically Set)
0	0	0	10x (power-up default)	930 kHz	000b
0	0	1	20x	385 kHz	000b
0	1	0	50x	460 kHz	001b
0	1	1	100x	640 kHz	010b
1	0	0	200x	195 kHz	010b
1	0	1	500x	130 kHz	011b
1	1	0	1000x	89 kHz	011b
1	1	1	User defined	800 kHz	1xxb

SERIAL CONTROL INTERFACE MODE

The LMP8358 is put into Serial Mode by setting VLSER/VHPAR < VHSER/VLPAR. In the Serial Mode the LMP8358 can be programmed by using pins 11 – 14 as shown in Table 3 and the SPI Timing Diagram. The LMP8358 contains a 16 bit register which controls the performance of the part. These bits can be changed using the Serial Mode of communication. The register of the LMP8358 is shown in Table 4. Immediately after power on the register should be written with the value needed for the application. See the START UP AND POWER ON RESET section.

Table 3. Function of Digital IO Pins, Serial Mode

Pin Name	Description
SDO	Serial Data Out
SDI	Serial Data In
SCK	Serial Clock
CSB	Chip Select
VLSER	Negative Logic level
VHSER	Positive Logic Level

Table 4. LMP8358 Register Description, Serial Mode

Bit No	Name	Description
0	G0	Gain setting (LSB)
1	G1	Gain setting
2	G2	Gain setting (MSB)
3	COMP0	Frequency compensation setting (LSB)
4	COMP1	Frequency compensation setting
5	COMP2	Frequency compensation setting (MSB)
6	MUX0	Input multiplexer selection (LSB)
7	MUX1	Input multiplexer selection (MSB)
8	POL	Input polarity switch
9	SHDN	Shutdown Enable
10	FILT	Enable filtering using external cap
11	PIN	Fault detection pin selection
12	CUR0	Fault detection current setting (LSB)
13	CUR1	Fault detection current setting
14	CUR2	Fault detection current setting (MSB)
15	N/A	Unused, set to 0

Serial Control Interface Operation

The LMP8358 gain, bandwidth compensation, shutdown, input options, and fault detection are controlled by an on board programmable register. Data to be written into the control register is first loaded into the LMP8358 via the serial interface. The serial interface employs an 16-bit double-buffered register for glitch-free transitions between settings. Data is loaded through the serial data input, SDI. Data passing through the shift register is output through the serial data output, SDO. The serial clock, SCK controls the serial loading process. All sixteen data bits are required to correctly program the amplifier. The falling edge of CSB enables the shift register to receive data. The SCK signal must be high during the falling and rising edge of CSB. Each data bit is clocked into the shift register on the rising edge of SCK. Data is transferred from the shift register to the holding register on the rising edge of CSB. Operation is shown in the SPI Timing Diagram.

The serial control pins can be connected in one of two ways when two or more LMP8358s are used in an application.

Star Configuration

The configuration shown in Figure 50 can be used if each LMP8358 will always have the same value in each register. After the microcontroller writes, all registers will have the same value. Using multiple CSB lines as shown in Figure 51 allows different values to be written into each register.

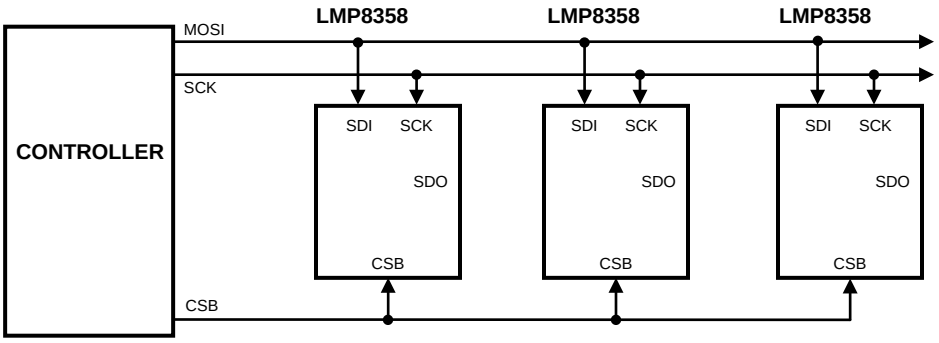


Figure 50. Star Configuration for Writing the Same Value Into Each Register

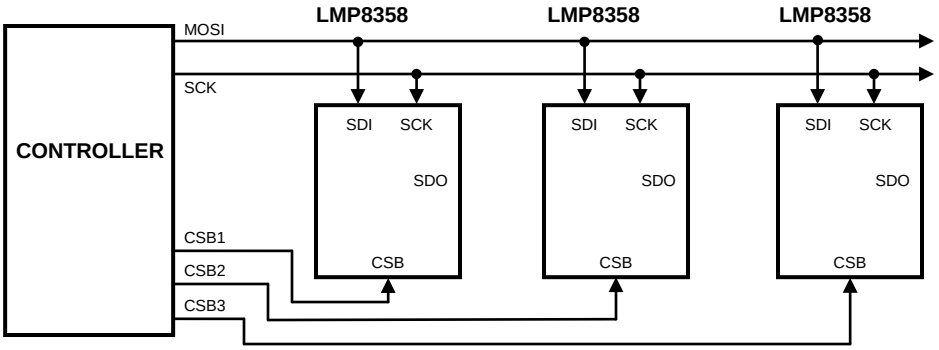


Figure 51. Star Configuration for Writing Different Values Into Each Register

Daisy Chain Configuration

This configuration can be used to program the same or different values in the register of each LMP8358. The connections are shown in Figure 52. In this configuration the SDO pin of each LMP8358 is connected to the SDI pin of the following LMP8358.

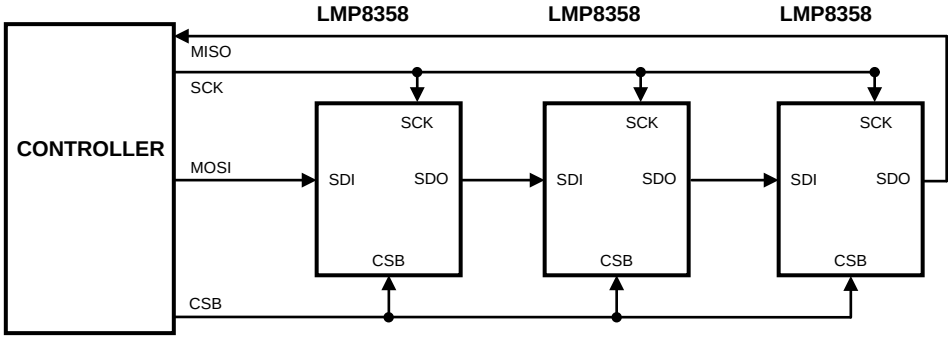


Figure 52. Daisy Chain Configuration

The following two examples show how the registers are written in the Daisy Chain Configuration.

Table 5. If all three LMP8358s need a gain of 100 with a compensation level of 010. (0000 0000 0001 0011)

	Register of LMP8358 #1	Register of LMP8358 #2	Register of LMP8358 #3	Notes
Power on	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	Default power on state

Table 5. If all three LMP8358s need a gain of 100 with a compensation level of 010. (0000 0000 0001 0011) (continued)

After first two bytes are sent	0000 0000 0001 0011	0000 0000 0000 0000	0000 0000 0000 0000	The data in the register of LMP8358 #1 is shifted into the register of LMP8358 #2, the data in the register of LMP8358 #2 is shifted into the register of LMP8358 #3.
After second two bytes are sent	0000 0000 0001 0011	0000 0000 0001 0011	0000 0000 0000 0000	
After third two bytes are sent	0000 0000 0001 0011	0000 0000 0001 0011	0000 0000 0001 0011	

Table 6. If LMP8358 #1 needs a gain of 20 (0000 0000 0000 0001), LMP8358 #2 needs a gain of 1000 with a compensation level of 011 (0000 0000 0001 1110), and LMP8358 #3 needs a gain of 100 with a compenstation level of 010 (0000 0000 0001 0011).

	Register of LMP8358 #1	Register of LMP8358 #2	Register of LMP8358 #3	Notes
Power on	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	Default power on state
After first two bytes are sent	0000 0000 0001 0011	0000 0000 0000 0000	0000 0000 0000 0000	The data in the register of LMP8358 #1 is shifted into the register of LMP8358 #2, the data in the register of LMP8358 #2 is shifted into the register of LMP8358 #3
After second two bytes are sent	0000 0000 0001 1110	0000 0000 0001 0011	0000 0000 0000 0000	
After third two bytes are sent	0000 0000 0000 0001	0000 0000 0001 1110	0000 0000 0001 0011	

LMP8358 SETTINGS

Gain (Serial, Parallel)

When the LMP8358 is in Parallel Mode the gain can be set by applying a high or low level to pins 12 (G2), 13 (G1), and 14 (G0), as shown in Table 2. The Frequency Compensation bits are automatically set as shown in Table 2 to optimize the bandwidth. In Serial Mode the gain is determined by setting G[2:0] as shown in Table 7 and the bandwidth can be changed using the Frequency Compensation bits in the register.

Table 7. Gain Setting (Register bits 2:0)

G2	G1	G0	Gain Setting
0	0	0	10x (power-up default)
0	0	1	20x
0	1	0	50x
0	1	1	100x
1	0	0	200x
1	0	1	500x
1	1	0	1000x
1	1	1	User Defined

When G[2:0] = 000b to 110b switch S1 is closed and switch S2 is open as shown in the Block Diagram.

When G[2:0] = 111b in either serial or parallel mode switch S1 is open and S2 is closed and the LMP8358 gain is set by external resistors as shown in Figure 53. The gain is:

$$GAIN = 1 + (Z1/Z2) \quad (1)$$

When the gain is set by external resistors and COMP[2:0] = 1xxb, a capacitor can be used to implement a noise reduction low pass filter. See the Filter and External Filter Capacitor (Serial) section. R1and C_{FILTER} are placed between the OUT and FB pins. R2 is placed between the FB and REFS pins.

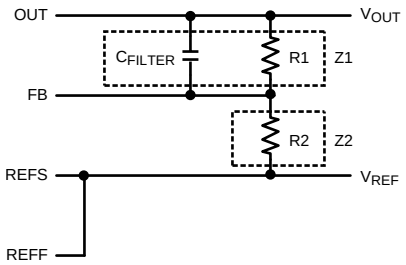


Figure 53. External Gain Set Resistors and Filter Capacitor

Frequency Compensation (Serial)

The gain-bandwidth compensation is set to one of five levels under program control. The amount of compensation can be decreased to maximize the available bandwidth as the gain of the amplifier is increased. The compensation level is selected by setting bits COMP[2:0] of the control register with 000b, 001b, 010b, 011b, or 1xxb. Table 8 shows the bandwidths achieved at the selectable gain and compensation settings. Note that for gains 10X and 20X, the recommended compensation setting is 000b. For the gain setting 50X, compensation settings may be 000b and 001b. Gain settings 100X and 200X may use the three bandwidth compensation settings 000b, 001b, and 010b. At gains of 500X and 1000X, all bandwidth compensation ranges may be used. Note that for lower gains, it is possible to under compensate the amplifier into instability.

Table 8. Frequency Compensation (Register bits 5:3)

	Bandwidth				
Gain\COMP [2:0]	000	001	010	011	1xx
10	930 kHz	n/a	n/a	n/a	74 kHz
20	385 kHz	n/a	n/a	n/a	37 kHz
50	160 kHz	460 kHz	n/a	n/a	16 kHz
100	80 kHz	225 kHz	640 kHz	n/a	8 kHz
200	38 kHz	95 kHz	195 kHz	n/a	4 kHz
500	16 kHz	40 kHz	85 kHz	130 kHz	1.5 kHz
1000	8 kHz	22 kHz	50 kHz	89 kHz	0.8 kHz
User Defined Gain GBW Product	> 10x 8 MHz	> 30x 24 MHz	> 100x 80 MHz	> 300x 240 MHz	> 1x 0.8 MHz (For external filter cap)

Input Multiplexer and Polarity Switch (Serial)

The Input Multiplexer Selection bits MUX[1:0] and Polarity bit POL can be used to set the inputs of the LMP8358 to the states shown in Table 9.

Table 9. Input Multiplexer and Polarity (Register bits 8:6)

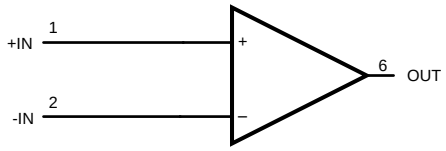
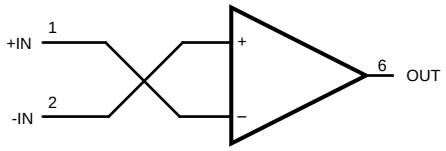
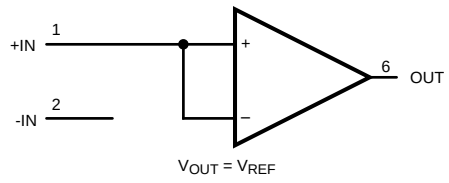
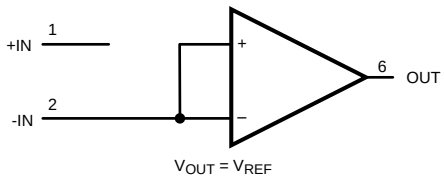
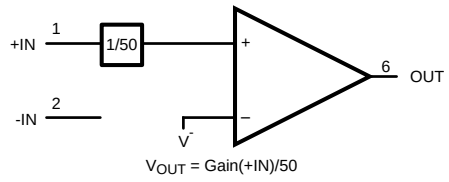
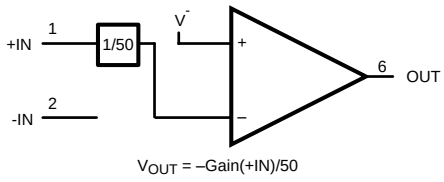
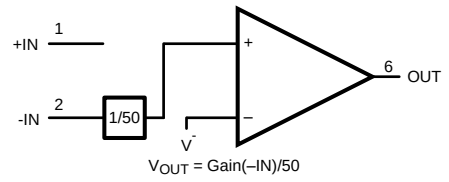
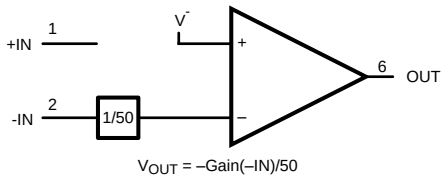
MUX1	**MUX0**	**Diff Input for POL = 0**	**Diff Input for POL = 1**
0	0	 V_{OUT} = Gain((+IN) – (–IN))	 V_{OUT} = Gain((–IN) – (+IN))

Table 9. Input Multiplexer and Polarity (Register bits 8:6) (continued)

MUX1	MUX0	Diff Input for POL = 0	Diff Input for POL = 1
0	1		
1	0		
1	1		

Polarity Reversal

When MUX[1:0] = 00b and POL = 0b the LMP8358 has the input of a normal instrumentation amplifier. The input for the LMP8358 is defined as Gain × (V_{+IN} − $V_{–IN}$). When POL = 1b, the input for the LMP8358 is defined as Gain × ($V_{–IN}$ – V_{+IN}). Polarity reversal can be used to do system level calibration, for example, to compensate for thermocouple voltages, residual offset of the LMP8358, or offsets of the sensor or ADC.

Short Inputs

When MUX[1:0] = 01b and POL = 0b both inputs are connected to the +IN pin of the LMP8358. The –IN pin is left floating. When MUX[1:0] = 01b and POL = 1b both inputs are connected to the -IN pin of the LMP8358. The +IN pin is left floating.

Compare Input to V-

When MUX[1:0] = 10b or 11b one external input of the LMP8358 is floating. The other external input is divided by 50 as shown in Table 9. The internal instrumentation amplifier input that is not connected to the external pin is connected to V^-. With a scale factor of 1/50 this gives an overall gain of 0.2x, 0.4x, 1x, 2x, 4x, 10x, or 20x depending on what the gain is set to with G[2:0] bits as shown in Table 10.

Table 10. Overall Gain using G[2:0], MUX[1:0] and POL

G[2:0]	MUX[1:0]	Overall System Gain	
		POL = 0b	POL = 1b
000b	10b or 11b	0.2	−0.2
001b	10b or 11b	0.4	−0.4
010b	10b or 11b	1	−1
011b	10b or 11b	2	−2
100b	10b or 11b	4	−4
101b	10b or 11b	10	−10
110b	10b or 11b	20	−20

Shutdown Enable (Serial, Parallel)

When the SHDN bit of the LMP8358 register is set to 1b the part is put into shutdown mode. It will use less than 1µA in this state.

Table 11. Shutdown (Register bit 9)

SHDN	Mode
0	Active mode
1	Shutdown mode

Filter and External Filter Capacitor (Serial)

The FILT bit controls the state of switch S2 shown in the Block Diagram. When G[2:0] = 000b to 110b, switch S2 will be open if FILT = 0b and S2 will be closed if FILT = 1b. When G[2:0] = 111b switch S2 is always closed and does not depend on the value in the FILT bit.

When FILT = 1b and COMP[2:0] = 1xxb the LMP8358 is unity-gain stable and an external filter cap can be applied as shown in Figure 53. The corner filter of the filter is:

$$F_{-3dB} = 1/(2\pi R_{FILTER} C_{FILTER}) \quad (2)$$

R_{FILTER} depends on the gain of the part and is shown inTable 13.

Table 12. Filter (Register bit 10)

FILT	Mode
0	No external filter cap used
1	External filter cap used

Table 13. R_{FILTER} Value

Gain	R_{FILTER} Value
10	18.5 kΩ
20	112 kΩ
50	168 kΩ
100	187 kΩ
200	1.12 MΩ
500	1.68 MΩ
1000	1.87 MΩ
User-Defined Gain	External Resistor R1

The tolerance of the R_{FILTER} value for the pre-defined gains is about ±3%. If an external filter cap is not used FILT should be set to 0b to prevent errors related to leakage currents on the FB pin.

Fault Detection Pin and Current Setting (Serial)

The LMP8358 has an internal current source that can be used to detect faults in the overall system. See the FAULT DETECTION METHODS Section. When PIN = 0b this current source is connected to the +IN pin. When PIN = 1b the current source is connected to the −IN pin.

Table 14. Pin Current Source (Register bit 11)

PIN	Current source is connected to
0	+IN pin
1	−IN pin

The Fault Detection Current bit, CUR[2:0] controls the amount of current that sent to the input pin as shown in Table 15.

Table 15. Fault Detection Current Source (Register bits 14:12)

CUR2	CUR1	CUR0	
0	0	0	disconnected and powered down *
0	0	1	10 nA
0	1	0	100 nA
0	1	1	1 µA
1	0	0	10 µA
1	0	1	100 µA
1	1	0	disconnected, but powered *
1	1	1	Do Not Use

* Leaving the fault detection current source powered allows it to switch between current levels faster, particularly when supplying currents less than 1 µA.

FAULT DETECTION METHODS

Using the Multiplexer, Polarity, and Current features the end user can detect faults in the system between the sensor and the LMP8358. These examples will use the set up shown in Figure 54 which shows a bridge sensor connected through some cabling to a supply and the LMP8358. The fault detection methods are described below.

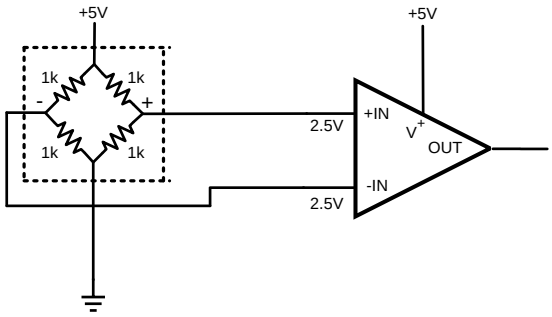


Figure 54. Bridge Connected to the LMP8358 With No Problems

Common Mode Out of Range

Figure 55 shows an example of a degraded connection between the bottom of the bridge and ground. This fault is shown by the 1.5 kΩ resistor placed between the bridge and ground. This will raise the common mode at the inputs of the LMP8358 to 4V, which is out of the CMVR. To determine the common mode voltage at the input pins, use the 1/50 feature by setting MUX[1:0] to 10b to test the +IN pin or to 11b to test the −IN pin, POL to 0b, and G[2:0] to 010b for a gain of 50 (0082x or 00C2x). This will give an overall gain of 1 and the output will read 4V for either MUX setting.

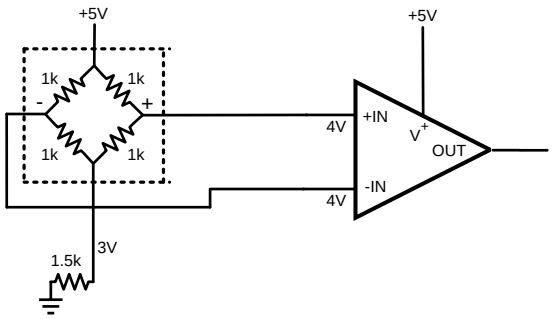


Figure 55. Degraded Connection Between the Bottom of the Bridge and Ground

Open Input

Figure 56 shows an example of an open input fault. To sense this type of fault use the 1/50 feature by setting MUX[1:0] to 10b to test the +IN pin or to 11b to test the −IN pin, POL to 0b, PIN to 1b to test the −IN pin, and G[2:0] to 010b for a gain of 50, and inject 100µA current by setting CUR[2:0] = 101b (5082x or 58C2x). Since the input is open the input pin will be pulled to V+. With an overall gain of 1 the output will read 5V for open input.

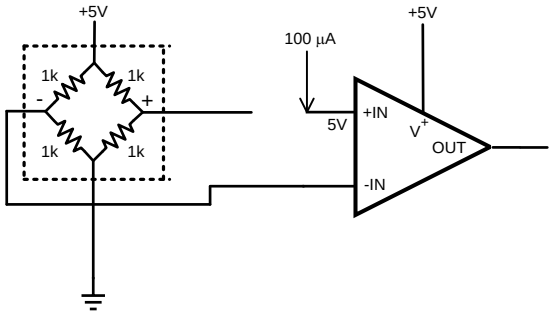


Figure 56. Open Input

Input Shorted to V+ or V−

Figure 57 shows an example of an input pin shorted to V+ or V−. To sense this fault, use the 1/50 feature by setting MUX[1:0] to 10b to test the +IN pin or to 11b to test the −IN pin, POL to 0b, and G[2:0] to 010b for a gain of 50 (0082x or 00C2x). This will give an overall gain of 1 and the output will read either V+ or V− depending on whether the input pin is shorted to V+ or V−.

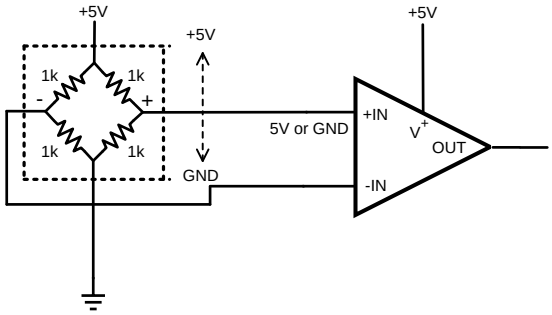


Figure 57. Input Shorted to V+ or V−

Shorted Inputs

Figure 58 shows the inputs of the LMP8358 shorted. To detect this fault set CUR[2:0] = 101b to inject a 100µA current and set the gain to 10× (5000x). The LMP8358 is set up with normal differential inputs. The output will read about 0.07V because of the voltage drop across the internal ESD resistor, which has a value between 60Ω to 90Ω. If the gain is set to 100× with an injected current of 100µA the output will be about 0.7V.

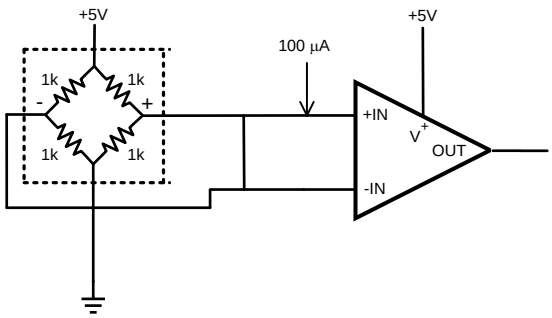


Figure 58. Shorted Inputs

Degraded Input Line

Figure 59 shows an example of a degraded connection between the bridge and the +IN pin of the LMP8358. This fault is shown by the 1 kΩ resistor placed between the bridge and the LMP8358. To detect this fault use the 1/50 feature by setting MUX[1:0] to 10b to test the +IN pin, POL to 0b, and G[2:0] to 010b for a gain of 50. This will give an overall gain of 1. Set CUR[2:0] = 101b to inject a 100µA current and read the output voltage (5082x). Next set MUX[1:0] to 11b and PIN to 1b to test the −IN pin as shown in Figure 60 and read the output (58C2x). If the voltages of these two measurements are different a degraded input fault exists.

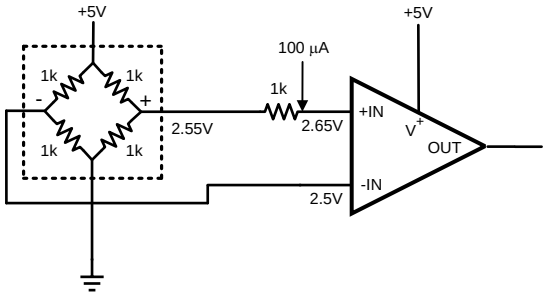


Figure 59. Degraded Input Line, Step 1

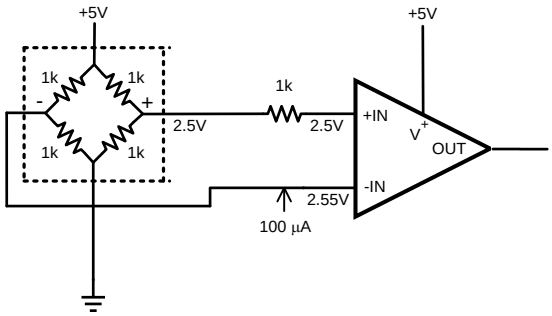


Figure 60. Degraded Input Line, Step 2

Fault Detection Example

Using the fault detection features of the LMP8358 an end product, such as a scale, can periodically test that no damage has occurred to the system. A routine can be written that could, for example, run on start up, that will step through the fault detection features shown above and compare the output voltage to a table like that shown in Table 16. If the circuit shown in Figure 54 is used the values shown in column 2 of Table 16 would show that the system is working correctly, the values in the columns under the Possible Faults heading would show that there is a potential problem and that operator attention is needed.

Table 16. Fault Detection Matrix

	No Faults	Possible Faults					
LMP8358 Register	V_{OUT}	V_{OUT}	Possible Cause	V_{OUT}	Possible Cause	V_{OUT}	Possible Cause
00 82x	2.5V	V_{OUT} < CMVR or V_{OUT} > CMVR	Input is out of CMVR	V^+	+IN shorted to V^+	0V	+IN shorted to GND
00 C2x	2.5V	V_{OUT} < CMVR or V_{OUT} > CMVR	Input is out of CMVR	V^+	−IN shorted to V+	0V	−IN shorted to GND
50 00x	0.61V	V^+	+IN Open	0.07V	Inputs shorted		
50 03x	4.97V	V^+	−IN	0.7V	Inputs shorted		
50 82x	2.55V	2.65V*	Degraded +IN line				
58 C2x	2.55V	2.55V*	Degraded +IN line				
50 82x	2.55V	2.55V*	Degraded −IN line				

Table 16. Fault Detection Matrix (continued)

58 C2x	2.55V	2.65V*	Degraded −IN line				

* The values shown for a degraded input line will vary depending on the resistance in the line. This table uses the value in Figure 59 and Figure 60, 1kΩ.

START UP AND POWER ON RESET

During power on, 50µs after $V^+ - V^-$ > 1V the LMP8358 resets the internal register to 0000x. If the digital supplies and inputs are undefined after the Power On Reset transients could occur which can cause erroneous data to be written over the default values in the register. The following should be done to prevent this from happening:

• Bring all supplies up at the same time. All power supplies, analog and digital, should be brought up together within 40µs so that the supplies are not undefined after the Power On Reset at 50µs. This is easiest done by tying the VHSER/VLPAR and VLSER/VHPAR pins to the analog supplies. — Parallel Mode

• Immediately after power on, write to the register the value needed for the application. (This is always recommended.) — Serial Mode

LAYOUT

The LMP8358 is a precision device that contains both analog and digital sections as shown in the Block Diagram. The PCB should be carefully designed to minimize the interaction between the analog and digital sections and to maximize the performance of the part. This should include the following:

0.1µF ceramic capacitors should be placed as close as possible to each supply pin. If a digital supply pin is tied to an analog pin only one 0.1µF capacitor is needed for both pins. A larger 1µF or 10µF capacitor should be located near the part for each supply.

Digital and analog traces should be kept away from each other. Analog and digital traces should not run next to each other, if they do the digital signal can couple onto the analog line. The LMP8358 pinout is set up to simplify layout by not having analog, power, and digital pins mixed together. Pins 1 — 6 are the analog signals, pins 7 — 10 are the power pins, and pins 11 — 14 are the digital signals.

Be aware of the signal and power return paths. The return paths of the analog, digital, and power sections should not cross each other and the return path should be underneath the respective signal or power path. The best PCB layout is if the bottom plane of the PCB is a solid plane.

The REFF and REFS pins are connected to the bottom side of the gain resistors of the LMP8358 as shown in the Block Diagram. Any impedance on these pins will change the specified gain. If the REFF and REFS pins are to be connected to ground they should be tied directly to the ground plane and not through thin traces that can add impedance. If the REFF and REFS pins are to be connected to a voltage, the voltage source must be low impedance. This can be done by adding an op amp, such as the LMP7701, set up in a buffer configuration with the LMP7701 output connected to REFF, the negative input of the op amp connected to REFS, and the desired reference voltage connected to the positive input of the op amp as shown in Figure 61.

DIFFERENTIAL BRIDGE SENSOR

Non-amplified differential bridge sensors, which are used in a variety of applications, typically have a very small differential output signal. This small signal needs to be accurately amplified before it can be used by an ADC.

The high DC performance of the LMP8358 makes it a good choice for use with a differential bridge sensor. This performance includes low input offset voltage, low input offset voltage drift, and high CMRR. The on chip EMI rejection filters available on the LMP8358 help remove the EMI interference introduced to the signal as shown in Figure 61 and improves the overall system performance.

The circuit in Figure 61 shows a signal path solution for a typical bridge sensor using the LMP8358. The typical output voltage of a resistive load cell is 2mV/V. If the bridge sensor is using a 5V supply the maximum output voltage will be 2mV/V × 5V = 10mV. The bridge voltage in this example is the same as the LMP8358 and ADC161S626 supply voltage of +5V. This 10mV signal must be accurately amplified by the LMP8358 to best match the dynamic range of the ADC. This is done by setting the gain of the LMP8358 to 200 which will give an output from the LMP8358 of 2V. To use the complete range of the ADC161S626 the V_{REF} of the ADC should be set to half of the input or 1V. This is done by the resistor divider on the V_{REF} pin of the ADC161S626. The

negative input of the ADC and the REFF and REFS pins of the LMP8358 can be set to +2.5V to set the signal at the center of the supply. A resistor divider supplies +2.5V to the positive input of an LMP7701 set up in a buffer configuration. The LMP7701 acts as a low impedance source for the REFF pin. The $V_{IO}$and VHSER/VLPAR pins should all be set to the same voltage as the microcontroller, +3.3V in this example. The VLSER/VHPAR pin should be connected to ground. The resistor and capacitor between the LMP8358 and the ADC161S626 serve a dual purpose. The capacitor is a charge reservoir for the sampling capacitor of the ADC. The resistor provides isolation for the LMP8358 from the capacitive load. The values listed in the ADC161S626 datasheet are 180Ω for the resistor and the 470pF for the capacitor. These two components also form a low pass filter of about 1.9MHz. If a filter is needed to attenuate disturbance from the internal auto−zeroing at 12kHz and the ping−pong frequency at 50kHz of the LMP8358 these values could be changed to 7870Ω and 0.01µF which will make a filter with a corner of about 2kHz.

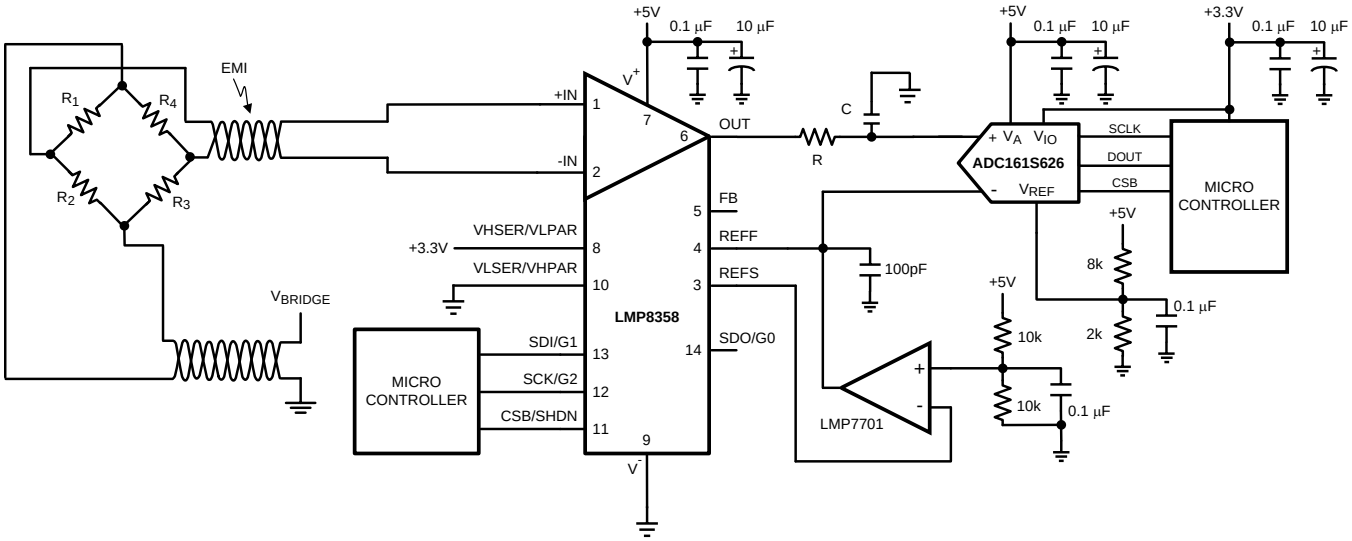


Figure 61. Differential Bridge Sensor

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	32

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8358MA/NOPB	ACTIVE	SOIC	D	14	55	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP8358 MA	Samples
LMP8358MAX/NOPB	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP8358 MA	Samples
LMP8358MT/NOPB	ACTIVE	TSSOP	PW	14	94	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP835 8MT	Samples
LMP8358MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LMP835 8MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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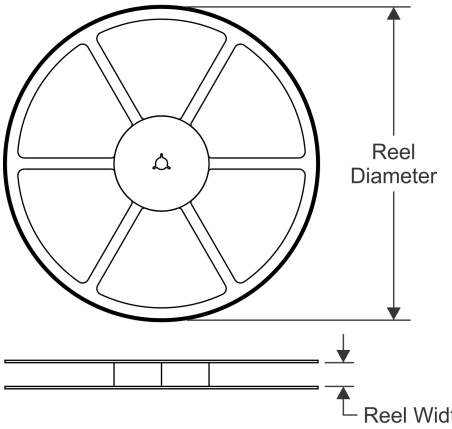
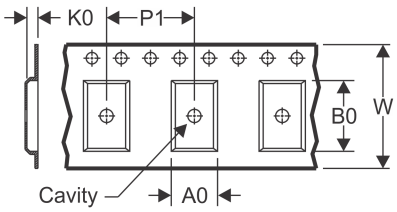
TAPE AND REEL INFORMATION

REEL DIMENSIONS

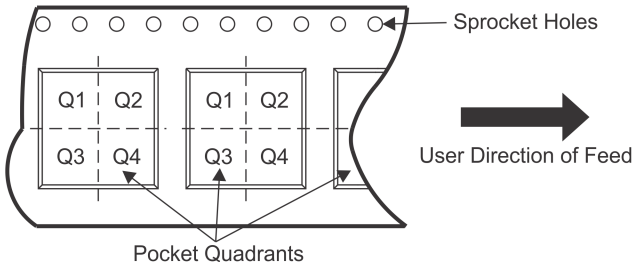


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

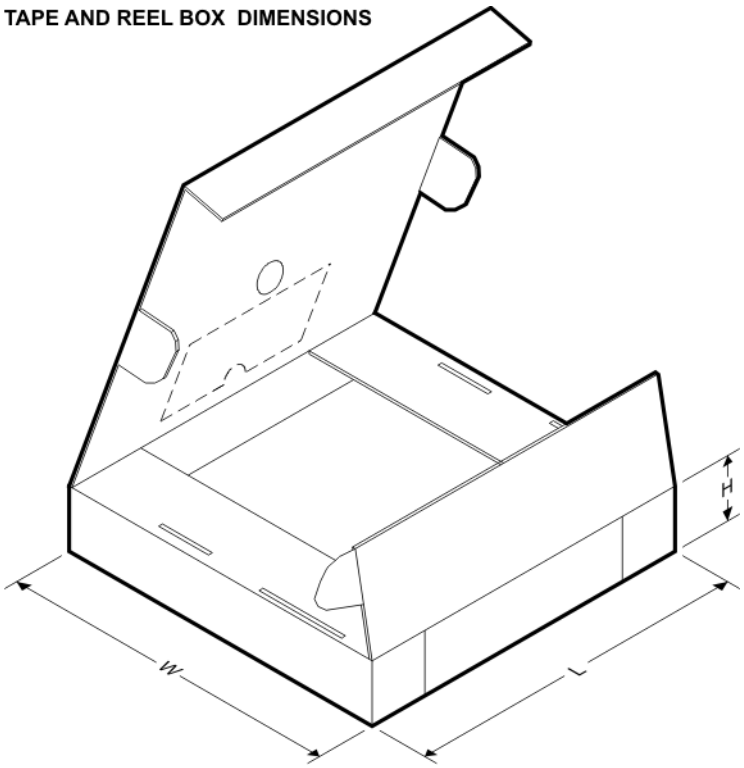
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8358MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMP8358MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

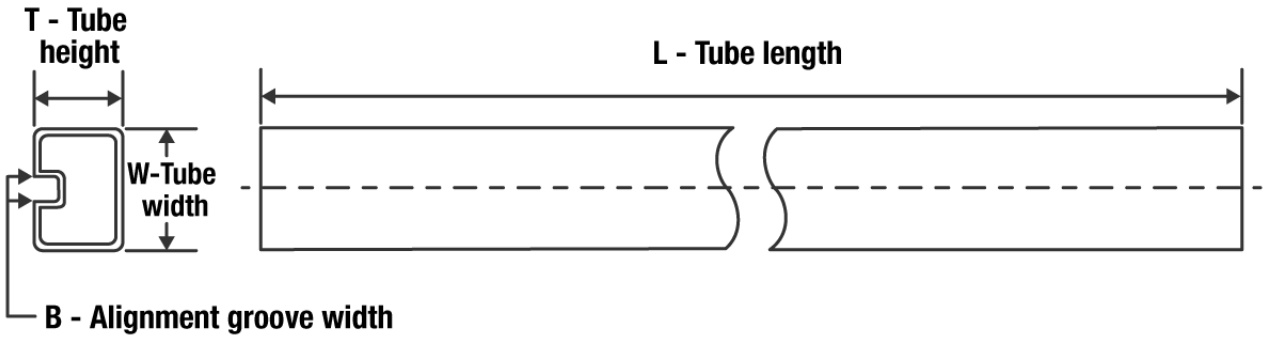
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8358MAX/NOPB	SOIC	D	14	2500	356.0	356.0	35.0
LMP8358MTX/NOPB	TSSOP	PW	14	2500	356.0	356.0	35.0

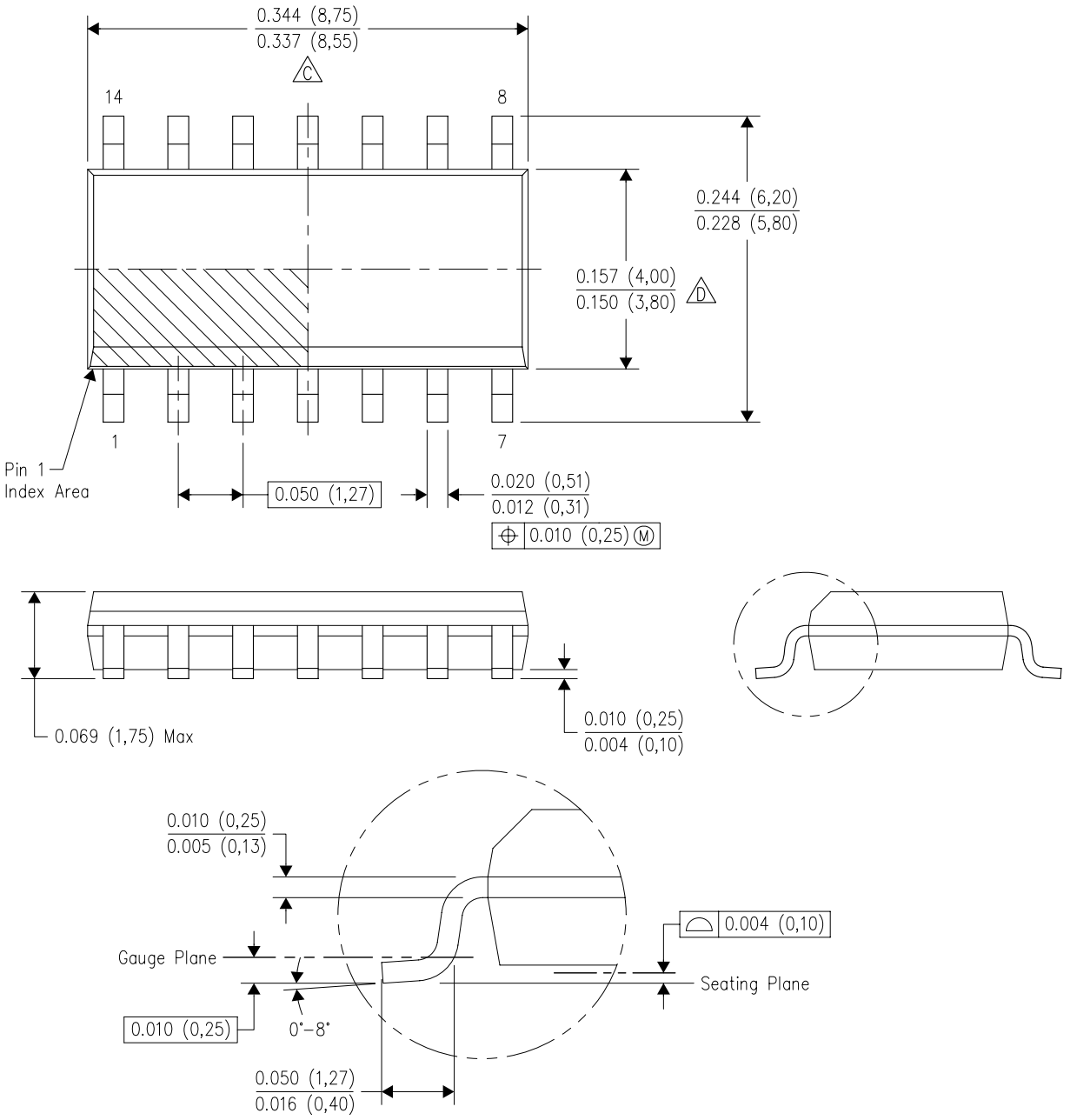
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMP8358MA/NOPB	D	SOIC	14	55	495	8	4064	3.05
LMP8358MT/NOPB	PW	TSSOP	14	94	495	8	2514.6	4.06

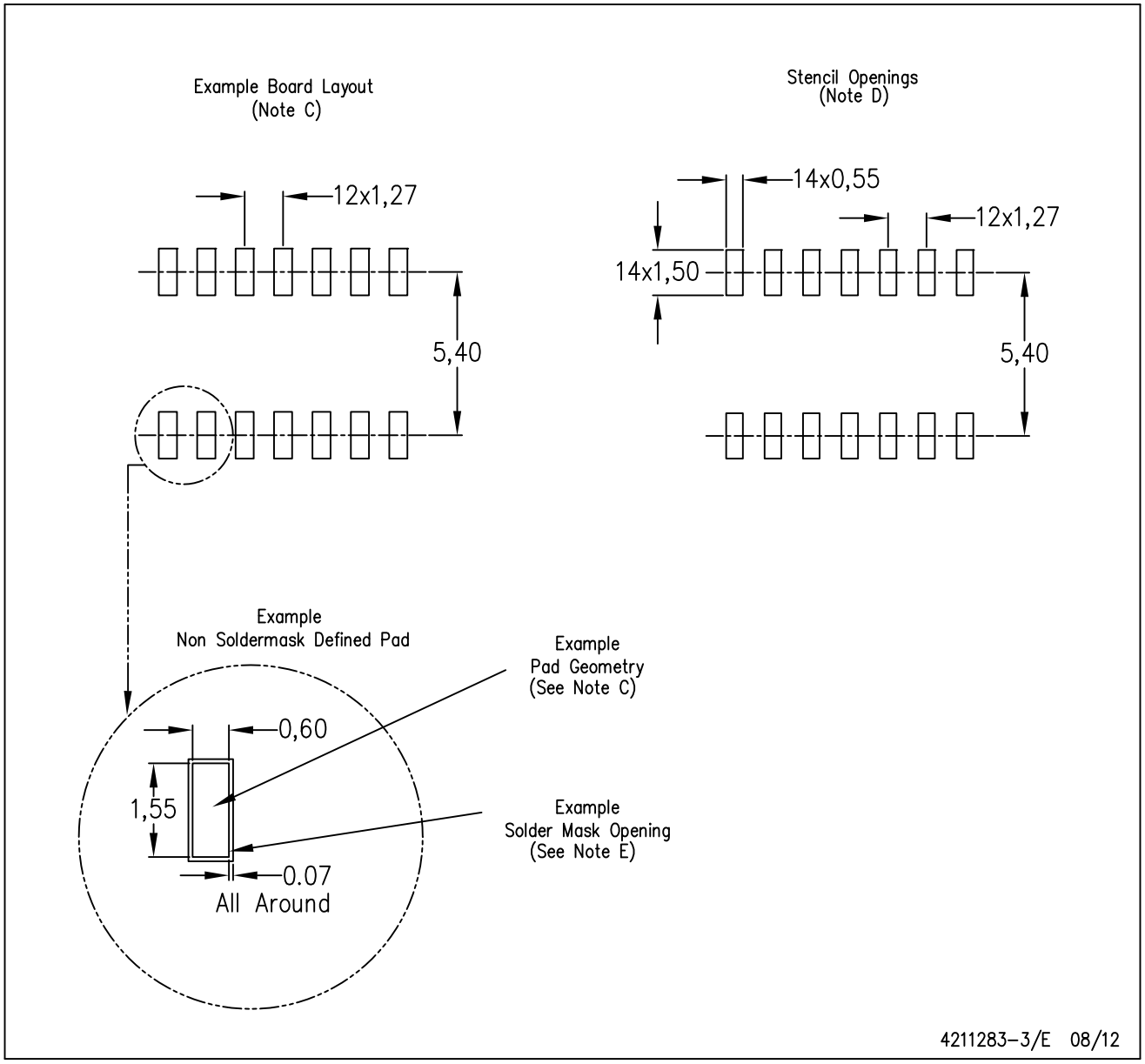
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

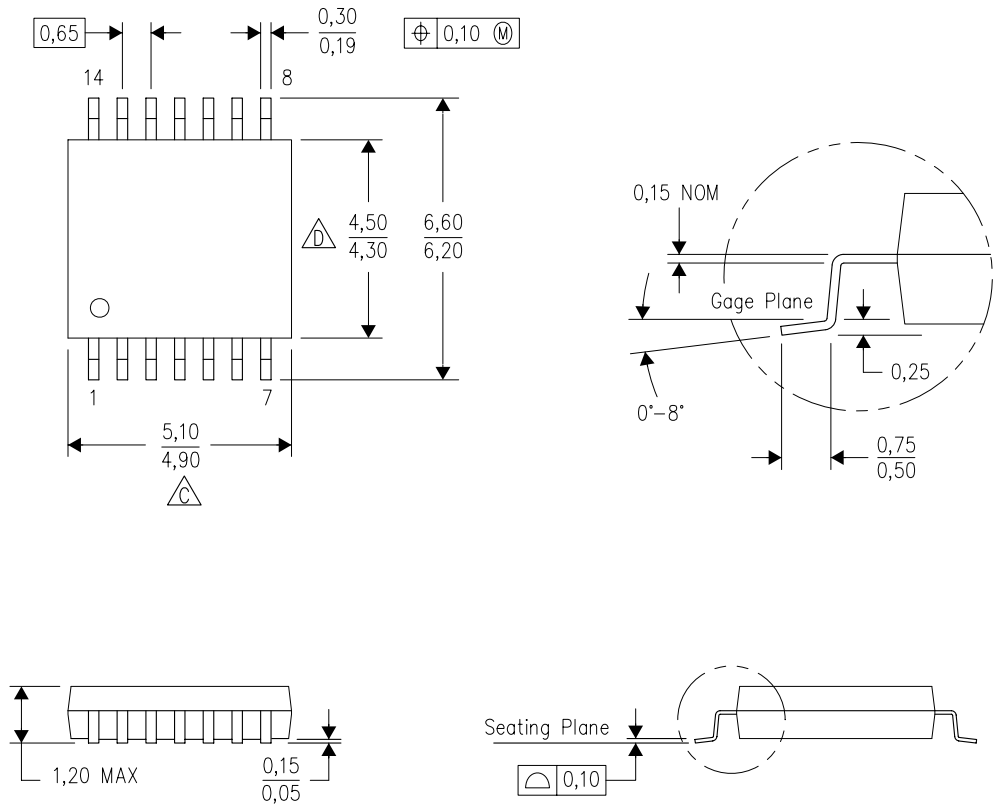
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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