

AN-1373 LM3200 Evaluation Board

1 Introduction

The LM3200 evaluation board is a working demonstration of a buck converter. This document contains information about the board. For further information on buck converter topology and component selection please see the data sheet.

2 General Description

The LM3200 converts high input voltages to lower output voltages with high efficiency. It does this through a inductor based switching topology, applying the input voltage to the inductor for a certain portion of the cycle. The duty cycle in PWM mode will be V_{OUT}/V_{IN} , which can be seen on the SW pin.

There are three modes of operation: Fixed Frequency PWM (Pulse Width Modulation), Forced Bypass, and Shutdown mode. Setting the BYP pin low ($\leq 0.4V$) or leaving floating places the device in PWM mode. Setting the BYP pin high ($\geq 1.2V$) places the device in Forced Bypass mode. Setting the EN pin low ($\leq 0.4V$) places the device in Shutdown mode. Setting the EN pin high ($\geq 1.2V$) enables normal operation.

At the PWM mode, the output voltage is setting by the voltage of the V_{CON} pin, as in the following formula:

$$V_{OUT} = 3 \times V_{CON} \tag{1}$$

3 Operating Conditions

The board will operate under the following conditions:

$$2.7V \leq V_{IN} \leq 5.5V$$

$$0.267V \leq V_{CON} \leq 1.2V$$

$$0 \text{ mA} \leq I_{OUT} \leq 300 \text{ mA}$$

4 Schematic

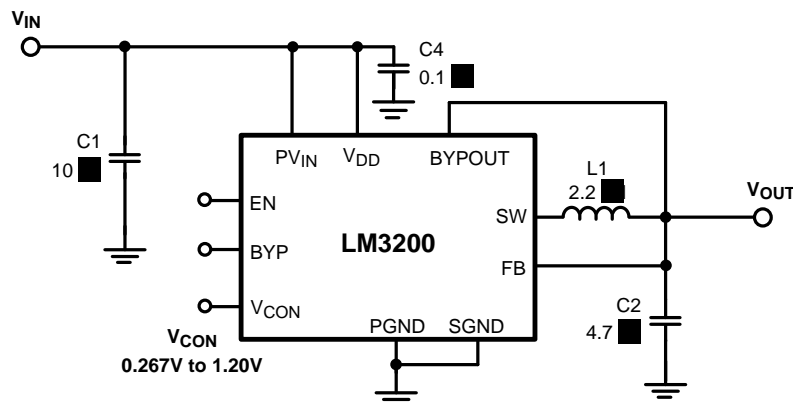


Figure 1. Typical Operating Circuit

5 Board Layout

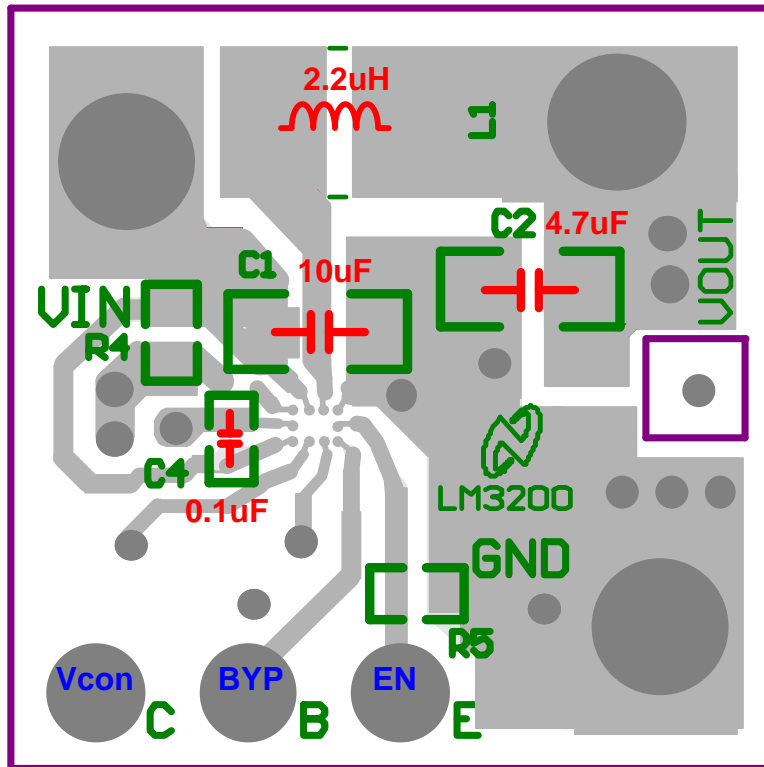


Figure 2. Top Layer

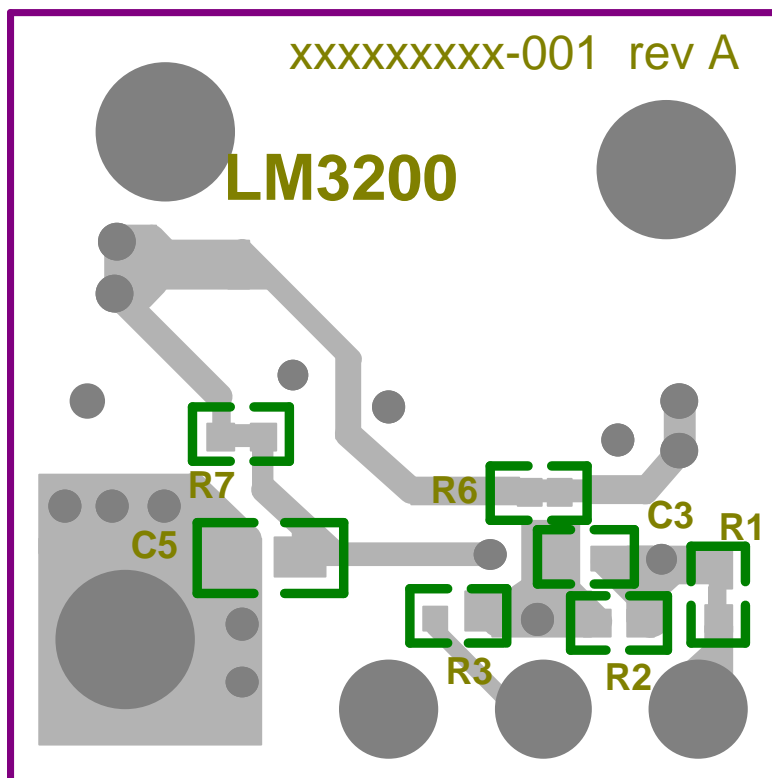


Figure 3. Bottom Layer

6 Connection Diagrams

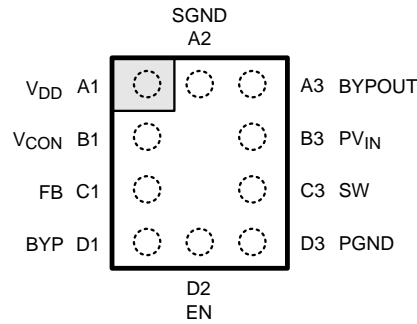
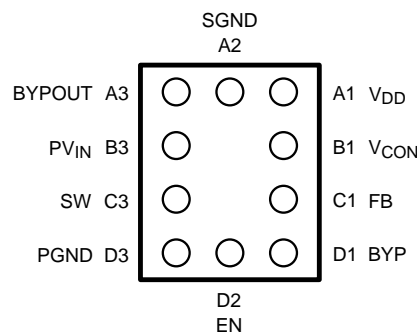


Figure 4. Top View



A 10-Bump Thin DSBGA Package, Large Bump

Figure 5. Bottom View

Table 1. Pin Description

Pin #	Name	Description
A1	V _{DD}	Analog Supply Input. A 0.1 μ F ceramic capacitor is recommended to be placed as close to this pin as possible.
B1	V _{CON}	Voltage Control Analog input. V _{CON} controls V _{OUT} in PWM mode. Set: V _{OUT} = 3 x V _{CON} . Do not leave floating.
C1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
D1	BYP	Bypass. Use this digital input to command operation in Bypass mode. Set the BYP pin high (> 1.2V) for Bypass mode. Set BYP low (< 0.4V) for normal operation.
D2	EN	Enable Input. Set this digital input high (> 1.2V) after V _{in} > 2.7V for normal operation. For shutdown, set low (< 0.4V).
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3200.
B3	PV _{IN}	Power Supply Voltage Input to the internal PFET switch and Bypass FET.
A3	BYPOUT	Bypass FET Drain. Connect to the output capacitor. Do not leave floating.
A2	SGND	Analog and Control Ground

7 BOM

	Manufacture	Manufacture #	Description
C1 (input C)	TDK	C3216JB1A106K	10 μ F,10V,20%,1206(3216)
C2 (output C)	TDK	C2012JB0J475K	4.7 μ F,6.3V,20%,0805(2012)
C4 (input C)			0.1 μ F,10V,20%,0402(1005)
L1 (inductor)	Coilcraft	DO3314-222	2.2 μ H inductor,1.6A Isat,0.2 Ω max.
COMMON TO ALL			
V _{IN} banana jack - red	Johnson Components	108-0902-001	conn banana jack insul nylon red
V _{OUT} banana jack - yellow	Johnson Components	108-0907-001	conn banana jack insul nylon yellow
GND banana jack - black	Johnson Components	108-0903-001	conn banana jack insul nylon black

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