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Application Report

AN-1380 Design Challenges in 5 Gbps Copper Backplanes

ABSTRACT

This application report examines the challenges in designing 5 Gbps backplanes and outlines solutions to these challenges.

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1 Introduction

With the migration of desktops to Gigabit Ethernet, and the ever-increasing demand for higher port density and lower cost per port, system designers of switches and routers are faced with the need to increase the capacity of backplanes that move traffic among line cards and switch fabric cards. They can design newer backplanes for higher speeds but this usually comes with the penalty of higher development costs and resistance from end customers for more costly new systems. Another approach is to re-use existing chassis and upgrade the switch cards to higher speeds, offering end customers an upgrade path with newer line cards when needed. This approach is more cost-effective, but it is technologically more challenging to upgrade older generation backplanes designed for lower speeds.

Today, most backplanes are running at speeds of 600 Mbps to 2.5 Gbps. Moving forward to 5 Gbps or beyond presents huge challenges to signal integrity engineers, system designers and IC designers alike. Migrating from 2.5 Gbps to 5 Gbps doubles the data rate, but usually comes with an exponential increase in transmission problems.

2 Backplane Impairments

There are several transmission impairments from a high speed backplane. These impairments include transmission loss, parasitic capacitance from plated-through holes used in the backplane, and crosstalk from adjacent channels. The impairments and their impact on data transmission are described in details in the following sections.

2.1 Transmission Loss

Below 2.5 Gbps, the transmission loss of a backplane is dependent on printed circuit board properties such as skin loss and dielectric loss. Above 2.5 Gbps, the transmission loss of a backplane is highly influenced by the backplane connectors, which are mostly high-density, press-fit connectors for reliability reasons. The small pitch of high-density connectors restricts useable trace width, typically 5–8 mils, resulting in even higher transmission loss.

Figure 1 shows the transmission loss of a 20-inch FR4 board trace using a 6-mil trace width versus a 20-inch backplane using an 8-mil trace width. Figure 2 illustrates the dominating effect of the backplane connector by comparing a 20-inch backplane versus a 10-inch backplane.
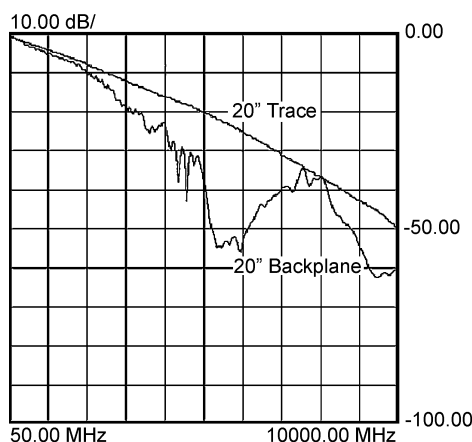
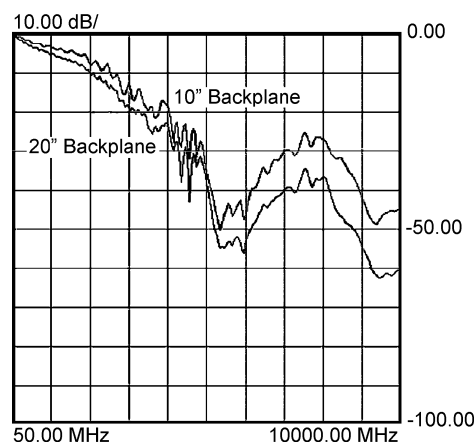**Figure 1. Comparing a 20-inch FR4 Board Trace versus a 20-inch Backplane**

Figure 2. Comparing a 20-inch versus a 10-inch FR4 Backplane

2.2 Connector Via and Via Stubs

For historical and reliability reasons, most of today's connectors use press-fit technology. Press-fit connectors mandate the use of relatively large plated-through holes, usually called via's. These plated-through holes interact with many layers of power and ground planes in a backplane, and cause excessive parasitic capacitance. A typical backplane thickness is about 200-mil, and a typical line card thickness is about 100-mil. Depending on which inner layer the differential signals are being routed, the length of via below the signal layer presents a stub. The signal layer closer to the top of the board has longer stub length, and consequently, has larger parasitic capacitance and higher transmission loss than the signal layers closer to the bottom of the board.

Figure 3 is a differential TDR plot showing the impedance profile of a backplane. The two dips on the left of the plot show the impedance drop due to the via of the connector at the line card and the via at the backplane. This drop in impedance presents an excess parasitic capacitance of about 0.5 pF–1.5 pF hanging at the connector.
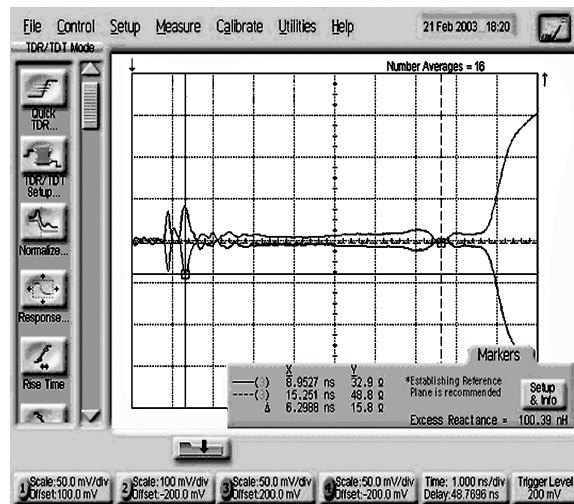

Figure 3. Impedance Profile of a Backplane

2.3 Inter-Symbol Interference (ISI)

The effect of transmission loss on a serial bit stream is higher deterministic jitter. The bandwidth limited transmission channel acts as a low-pass filter and introduces attenuation distortion to the higher frequency components of a data bit stream. Figure 4 illustrates the effect of transmission loss on a K28.5 bit stream. As shown in Figure 4, the lower frequency 5-bit continuous 1's bit stream has larger amplitude than a higher frequency one-bit pulse. Depending on their starting amplitude, the data transitions follow different paths, resulting in variations from their nominal positions. These variations in data transition position introduce jitter that is dependent on the data pattern. This type of jitter is commonly called data dependent jitter.

Figure 5 illustrates and Table 1 summarizes the pulse shape of a 1-bit pulse at the end of a backplane at 1.25, 2.5 and 5 Gbps. The pulse amplitude shrinks as speed and transmission loss increase. At 5 Gbps, the complimentary signals do not cross each other, resulting in eye closure. The pulse width is also much greater than one bit period because of edge rate degradation from the backplane. The residual voltage of the previous transition that extends into the next symbol influences the next data transition.

The variation in data transitions in a passive backplane is pattern dependent. The pattern dependent jitter is bounded and is commonly referred to as deterministic jitter. This increase in jitter makes it difficult for the downstream receiver to correctly recover data. Figure 6 depicts the eye diagrams of a pseudo-random bit stream after a backplane at 1.25, 2.5 and 5 Gbps. The eye closure for a 5 Gbps copper backplane poses a huge challenge to system designers.
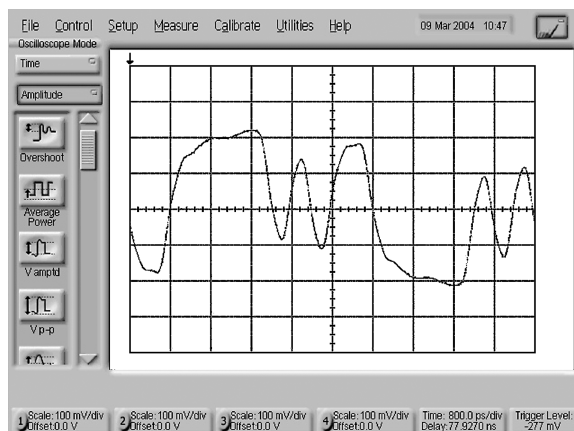
Figure 4. Waveform of a K28.5 Bit Stream at 2.5 Gbps

(a) 1.25 Gbps, 1-Bit Pulse

(b) 2.5 Gbps, 1-Bit Pulse
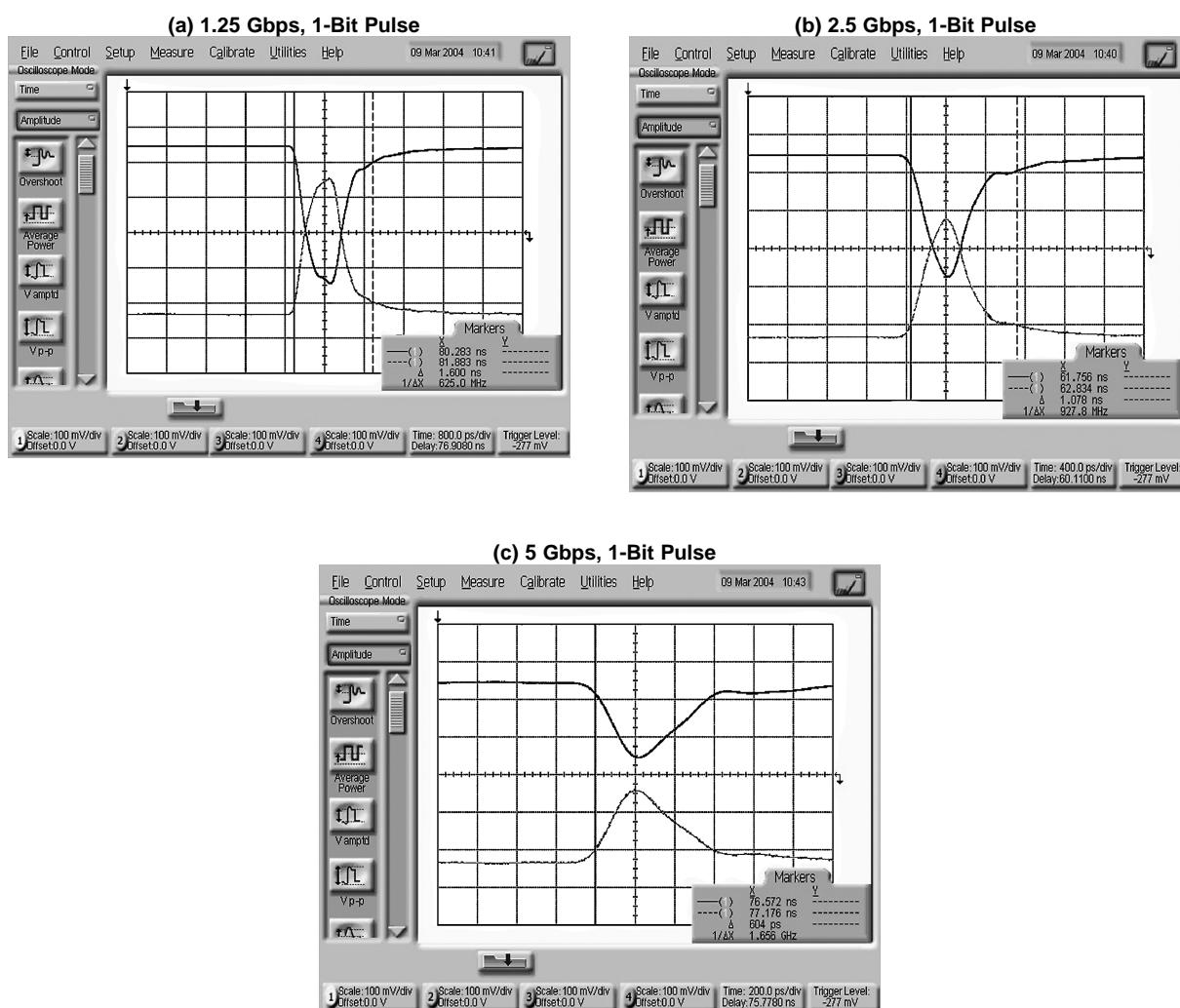
(c) 5 Gbps, 1-Bit Pulse

Figure 5. 1-Bit Pulses at 1.25 Gbps, 2.5 Gbps, and 5 Gbps

Table 1. Summary of 1-Bit Pulse Duration as Shown in Figure 5

	Symbol Width (1 UI)	Approximate Pulse Duration
1.25 Gbps	800 ps	1600 ps (2.0 UI)
2.5 Gbps	400 ps	1100 ps (2.75 UI)
5 Gbps	200 ps	604 ps (3 UI)

(a) 1.25 Gbps   **(b) 2.5 Gbps**

(c) 5 Gbps

Figure 6. Eye Diagrams of Pseudo-Random Bit Stream at 1.25 Gbps, 2.5 Gbps, and 5 Gbps Running (2^{10}-1) Pattern

2.4 Crosstalk

In addition to transmission loss, near-end-crosstalk (NEXT) is the second most important factor affecting data integrity of high-speed backplanes operating beyond 2.5 Gbps. The conducting elements inside a connector create electromagnetic fields, which are coupled to conductors in the adjacent pairs of the connector. Similar coupling occurs in the cylindrical vias used by adjacent connector pairs.

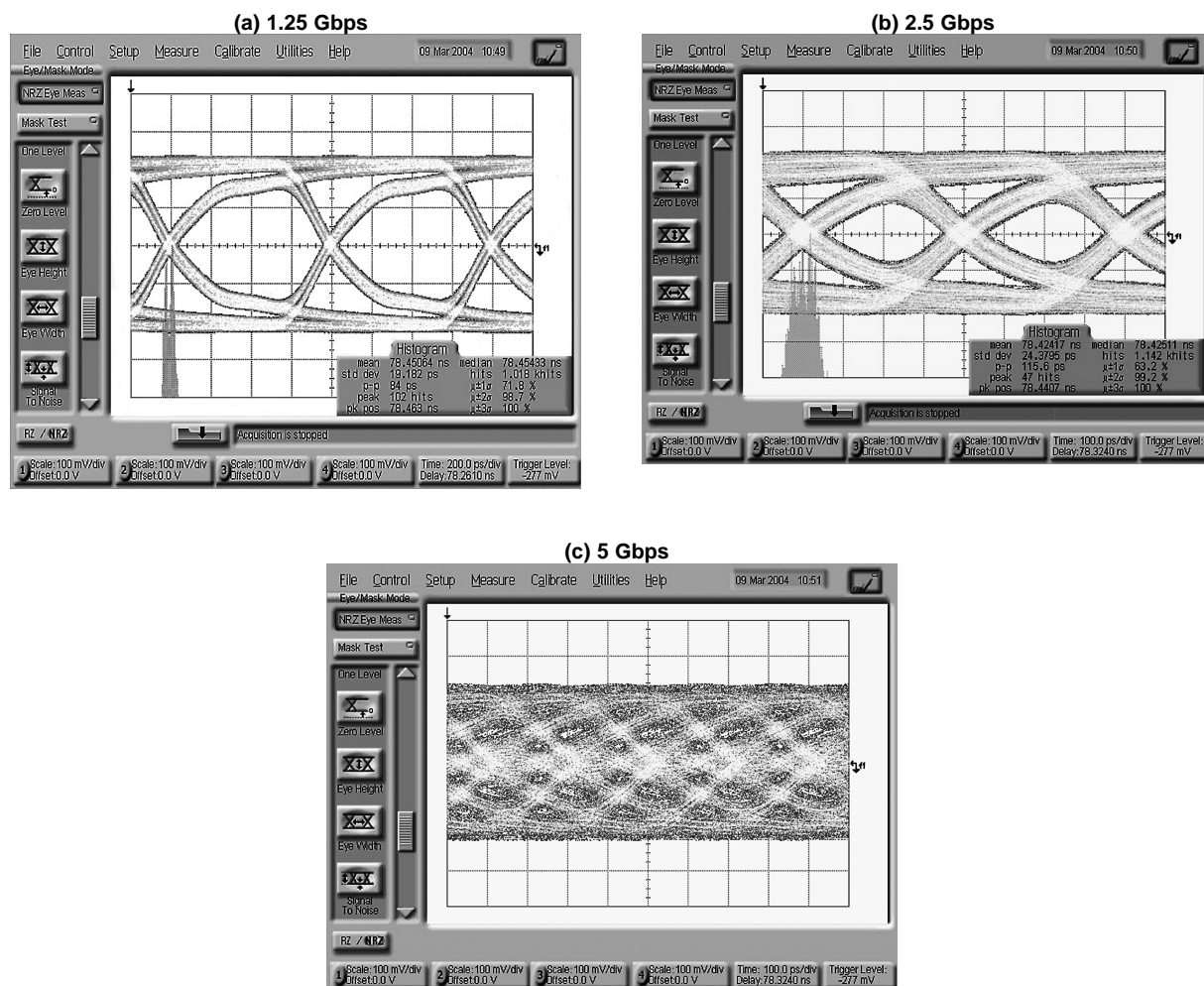On a line card, the transmitters are driving the backplane at full amplitude, usually higher than 1000 mV$_{PP}$. The transmitted signal is heavily attenuated by the backplane and becomes a weak signal when it reaches the receiver at the other end of the backplane. The near-end-crosstalk from the strong local driver superimposes onto the weaker receive signal, resulting in a poor signal-to-noise ratio. At 5 Gbps, it is not uncommon to have 20 dB transmission loss in the data path and 28 dB of near-end-crosstalk, resulting in a S/N ratio of merely 8 dB. Figure 7 shows the signal paths illustrating the significance of NEXT.
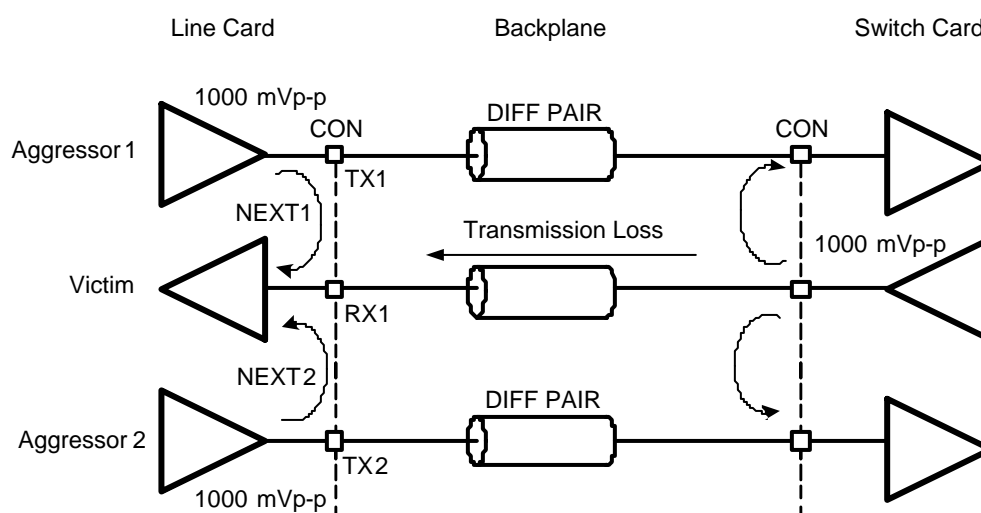

Figure 7. Signal Paths of Victim and Agressors

2.4.1 Crosstalk Amplitude Increases With Speed

Each data transition in the aggressor driver introduces an asymmetric crosstalk pulse on the victim channel. The crosstalk pulse usually spans a few hundred picoseconds in duration. At lower data rates, the crosstalk pulse fades in amplitude within one symbol width. At higher data rates with smaller bit width, the crosstalk pulse duration is comparable or larger than one symbol width. Figure 8a shows an aggressor running at 2.5 Gbps with repeating pattern of ten 1's and ten 0's. The crosstalk caused by one data transition at the aggressor has faded before another crosstalk pulse appears. Figure 8b shows the same aggressor running at 5 Gbps. Before one crosstalk pulse fades, another crosstalk pulse arrives, superimposing on the previous crosstalk pulses. As a result of this additive effect, crosstalk amplitude increases as speed increases and symbol width shrinks. The effect of NEXT is critical in high data rates, such as 5 Gbps, where system engineers have to battle high transmission loss in the victim channel and increased crosstalk from the aggressor channels. Figure 9 illustrates the increase in NEXT amplitude with data rate.

(a) 2.5 Gbps   **(b) 5 Gbps**
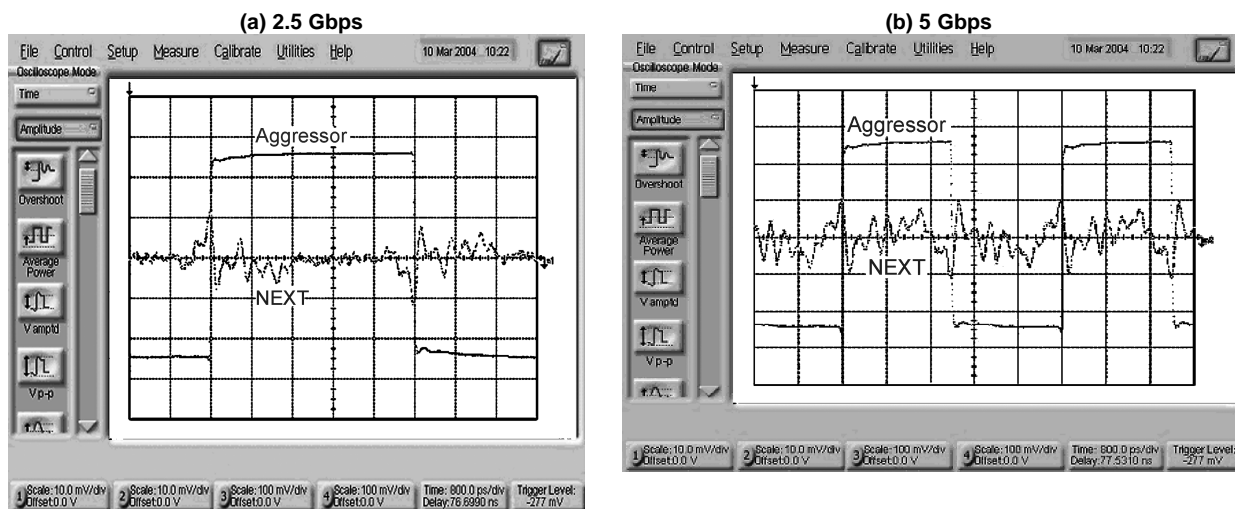
Figure 8. Cumulative Effect of NEXT Pulses as Bit Width Shrinks at 2.5 Gbps and 5 Gbps

(a) 1.25 Gbps   **(b) 2.5 Gbps**
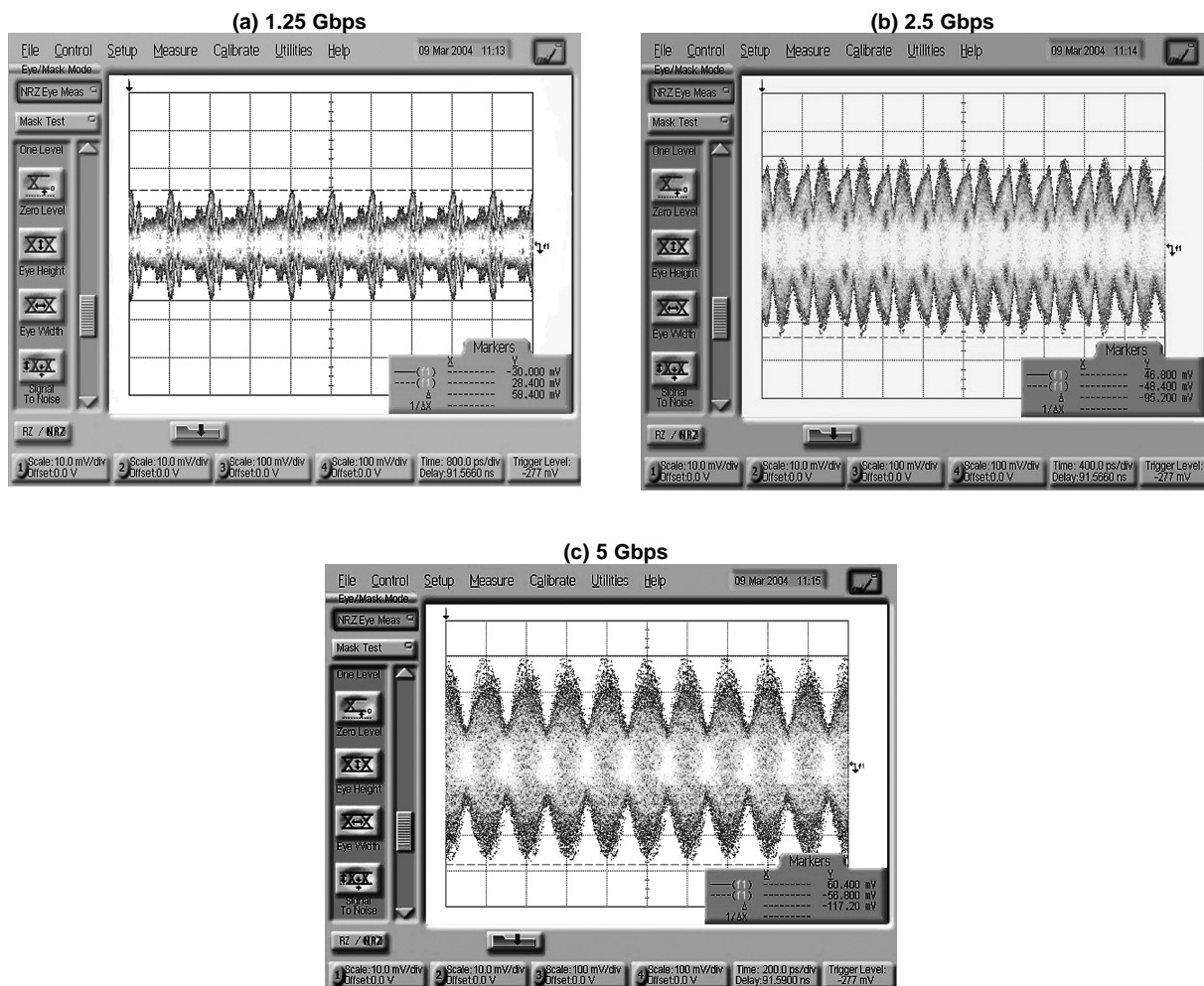
(c) 5 Gbps

Figure 9. NEXT Amplitude at 1.25 Gbps, 2.5 Gbps, and 5 Gbps, Running (2^{10}-1) Pattern

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2.4.2   Crosstalk Decreases the Receiver's Timing Margin

Crosstalk results in high frequency jitter in the victim channel. The weak receive signal is contaminated by crosstalk which disturbs the positions of the receive data transitions. Figure 10 illustrate the effect of severe crosstalk on an alternating-1-0-pattern at 5 Gbps, with the aggressor channel running $(2^{10}-1)$ pattern at 5 Gbps. Crosstalk reduces the receiver's timing margin in data recovery. In severe crosstalk situations, it becomes difficult to sample the data correctly. This results in a high error rate and affects system performance.

Figure 10. Alternating-1-0-Pattern at 5 Gbps Without and With Crosstalk

2.5 Not All Backplanes are the Same

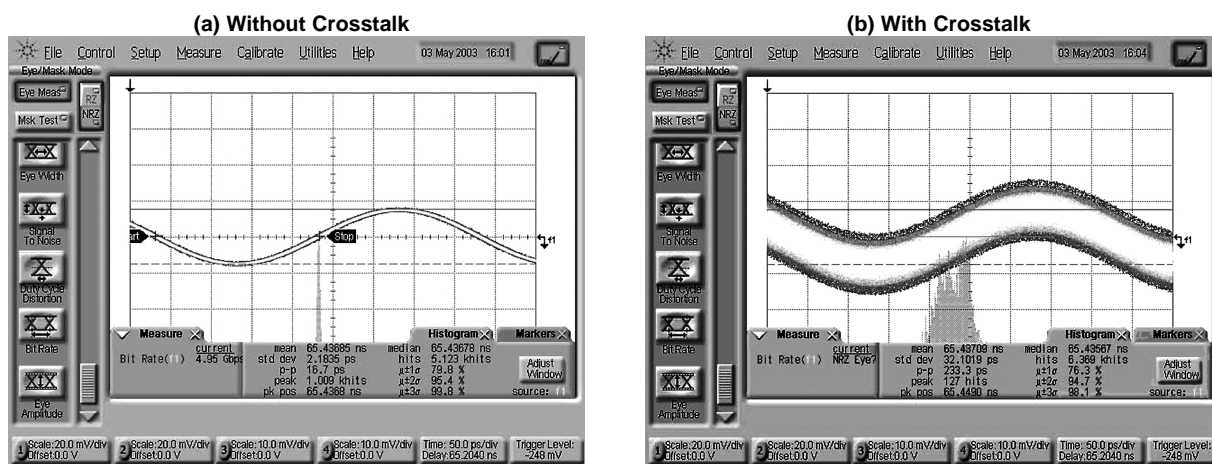The transmission impairments are directly affected by connector's performance, board geometry used in the backplane design (such as via structure, trace width, board thickness, board stack-up and board material) and how differential pairs are assigned within the connector. Newer backplane designs make use of newer and high-speed friendly connectors with less impedance mismatch and lower crosstalk. These new connectors, along with high-speed printed circuit board design techniques, have eased the routing constraints at the connector interface. Legacy backplanes usually built years ago, used older generation connectors designed for lower speed operation. These legacy backplanes are not high-speed friendly because of higher impedance mismatch and higher crosstalk coupling. Upgrading these legacy backplanes to 5 Gbps requires the use of high performance transceiver integrated circuits that are more tolerant to transmission impairments. A few examples are shown in Figure 11 illustrating the channel characteristics in transmission loss and crosstalk. At 5 Gbps, the point of interest is the transmission loss and the ratio of transmission loss to NEXT at 2.5 GHz.
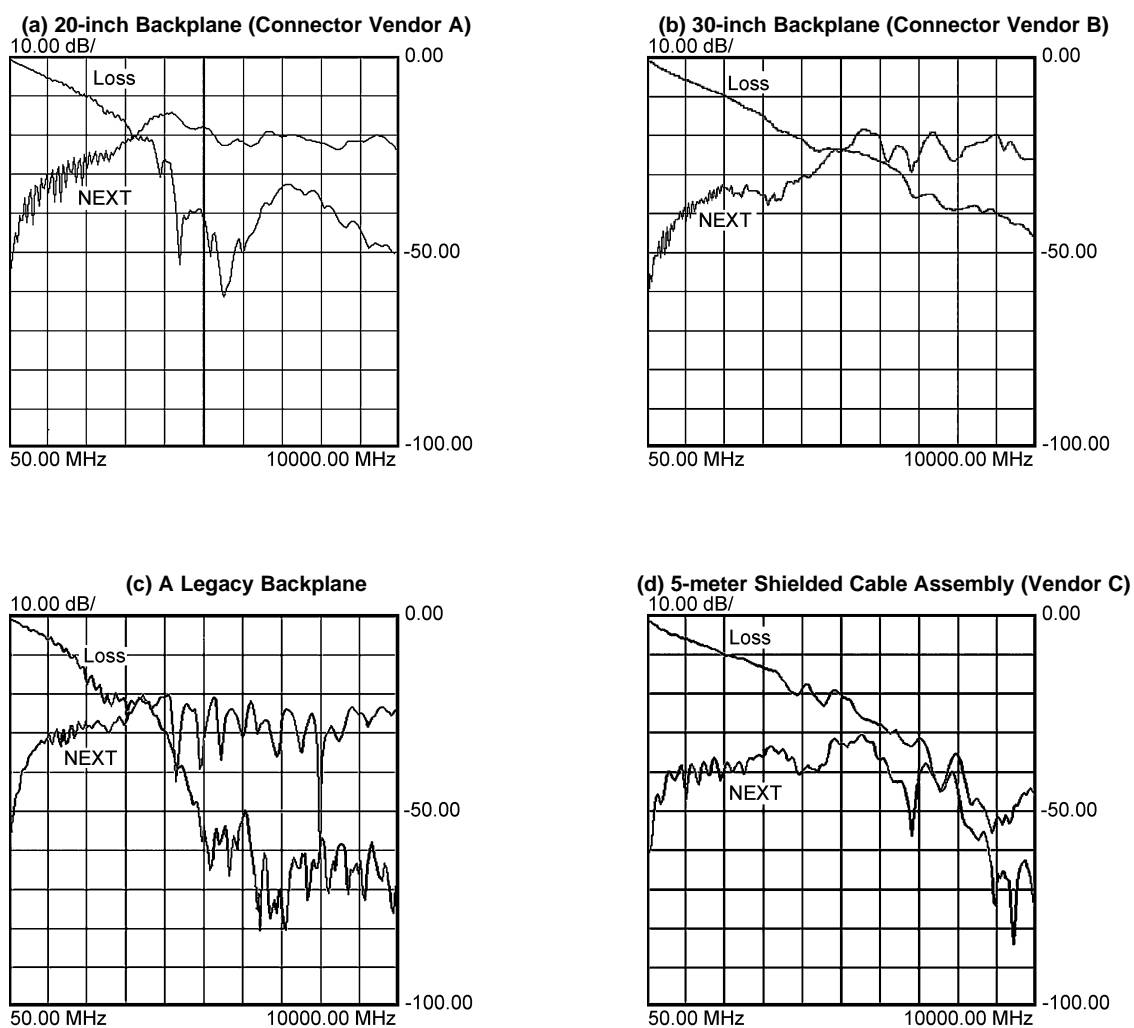
Figure 11. Loss and NEXT of Several Types of Transmission Channels

3 Multi-Gbps Backplane is Feasible

The success of a 5 Gbps backplane design relies on careful jitter management and the use of high performance backplane transceiver components. In newer backplane designs, system engineers can reduce the transmission loss through the use of high-speed board design techniques and newer and better high speed connectors. Coded bit streams, such as 8b/10b coding, are commonly used to limit the span of the spectral components to control the amount of ISI distortion. The use of newly introduced high-performance SerDes and signal conditioning integrated circuits makes the migration path to 5 Gbps a reality.

The techniques that enable 5Gbps copper backplanes are described in details in the following sections.

3.1 Receive Equalization

Through the use of receive equalization technique, designing 5 Gbps is feasible for newer and better backplanes, as well as the older legacy backplanes. Because the transmission loss between the shortest and the longest channels only vary by a few dB, a fixed equalizer is able to equalize the longest channel without causing a negative impact to the shorter channels. Located at the receive end of the backplane, the equalizer compensates the channel loss by boosting the higher frequency components of the signal, thereby minimizing the amplitude difference between the low and high frequency components of the bit stream. Equalization reduces the ISI caused by the backplane and restores an ample eye opening for successful data recovery. A stand-alone equalizer design, such as Texas Instruments EQ50F100, allows system designers to place the equalizer close to the connector on a line card. After equalizing the backplane channel, it re-shapes the waveform and feeds the signal to a SerDes for data recovery. A stand-alone equalizer also allows system designers to use different equalizer designs to optimize against different channel characteristics.
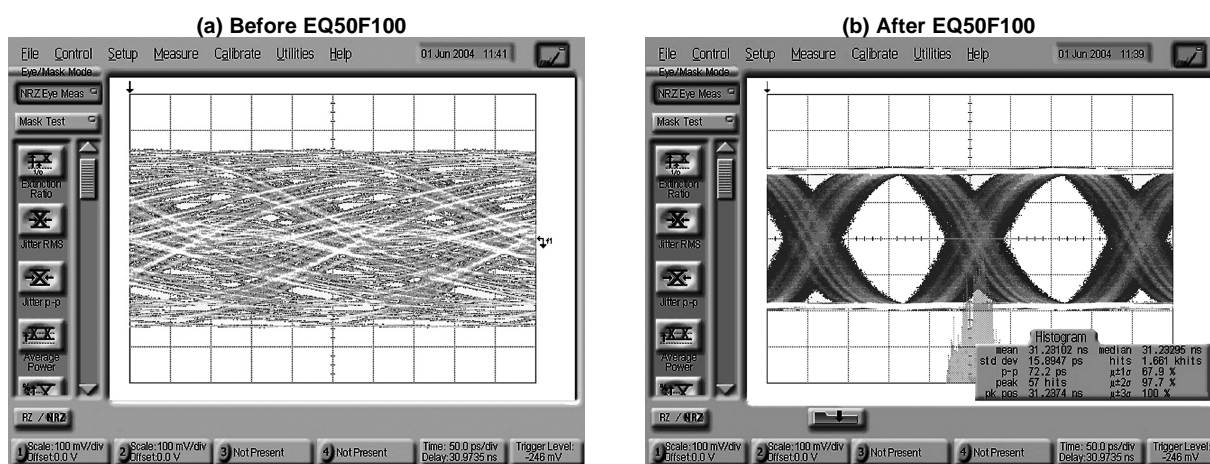

Figure 12. Eye Diagrams Before and After EQ50F100 Used In a Legacy Backplane

3.2 Driver De-Emphasis

In a less lossy backplane where the eye is not severely attenuated, a small amount of equalization is needed to reduce the ISI distortion. A de-emphasis technique, implemented in the transmit driver, reduces the driving amplitude of the lower frequency components of the bit stream to a level comparable to the higher frequency components after the channel loss. Figure 13 shows a driver waveform with de-emphasis. This technique is more crosstalk-friendly. Unlike traditional pre-emphasis technique used by other lower speed SerDes, de-emphasis does not increase the drive amplitude and thus will not worsen critical crosstalk problems at higher data rates. The newly introduced SCAN50C400 5 Gbps backplane transceiver features programmable de-emphasis for its transmit drivers.
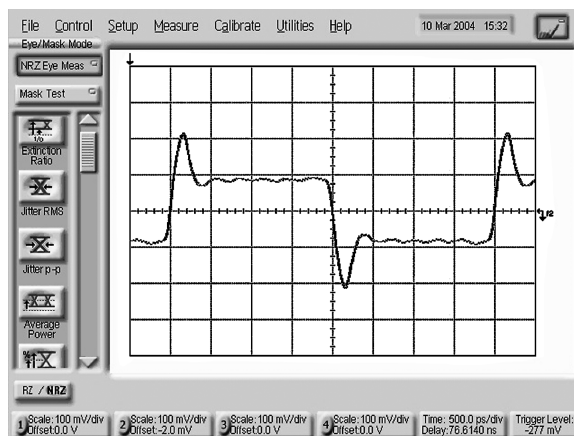

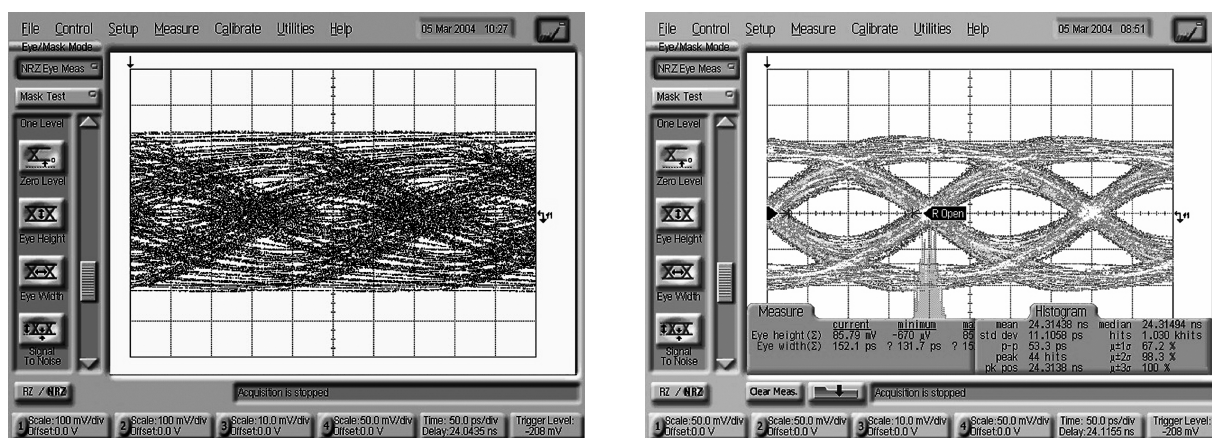**Figure 13. De-Emphasis Waveform from Driver**

Figure 14. Eye Diagrams With and Without De-Emphasis After a 30-inch Backplane

3.3   Crosstalk Management

Crosstalk introduces high frequency jitter into the input data bit stream of a receiver. The receive PLL is unable to track (follow) the high frequency jitter that is beyond its PLL bandwidth, and consequently causes a reduction in the receiver's timing margin to recover data correctly. A receiver with high input jitter tolerance is necessary to withstand the reduction in timing margin. One way users can reduce crosstalk is the use of the smallest transmit drive level acceptable to the downstream receiver. System designers can reduce crosstalk significantly by avoiding transmit and receive signals using adjacent pins of the connector. Having transmit and receive pairs adjacent to each other maximizes signal coupling and unwanted crosstalk.

3.4   High Performance Transceiver

Texas Instruments SCAN50C400 is a high performance SerDes transceiver designed for 5 Gbps backplane applications. It is equipped with high receive input sensitivity (< 100mV), and is able to recover data from a weak signal due to a lossy backplane. Its receive PLL has an input jitter tolerance of about 150ps, providing ample timing margin to recover data amidst ISI, noise and crosstalk impairments from the backplane. The SCAN50C400 also features low transmit jitter, programmable output drive amplitude to minimize crosstalk and programmable driver de-emphasis to compensate for transmission loss of backplane.

3.5   Avoid Noisy Power Supplies

It is important for system engineers to avoid excessive power supply noise within the bandwidth of the transmitter's PLL of a SerDes transceiver. Noise in the passband of the PLL will be translated directly into periodic jitter at the transmitter's output. If this noise induced periodic jitter is within the PLL bandwidth of the downstream receiver, the PLL will track the jitter and produces no harm. In a multi-supplier environment, it is hard to know which supplier's receiver will be used. A good engineering practice is to minimize the supply noise induced jitter. To further enhance the performance of the SCAN50C400 in a system, Texas Instruments offers a very low noise down-converting switching regulator LM27262. It has a fixed switching frequency of about 300 KHz and switching noise less than a few millivolt. Cleaner power supplies such as Texas Instruments LM27262 improve overall jitter performance and result in low error rate performance in the system.

4   Solution

Texas Instruments offers a total solution to enable 5 Gbps backplane while maintaining backward compatibility to legacy 1.25 Gbps or 2.5 Gpbs line cards. Figure 15 shows this solution. The total solution consists of the following components:

- SCAN50C400: Quad 1.25, 2.5 or 5 Gbps backplane transceiver with programmable output level and programmable de-emphasis. *SCAN50C400A 1.25/2.5/5.0 Gbps Quad Multi-Rate Backplane Transceiver* (SNOSA22).
- EQ50F100: Single 1–6.25 Gbps PCB equalizer. *EQ50F100 1Gbps - 6.25 Gbps Backplane Equalizer* (SNOSAB8).
- LM27262: Voltage regulator controller. *LM27262 Intel CPU Core Voltage Regulator Controller for VRD10 Compatible PCs* (SNVS262).
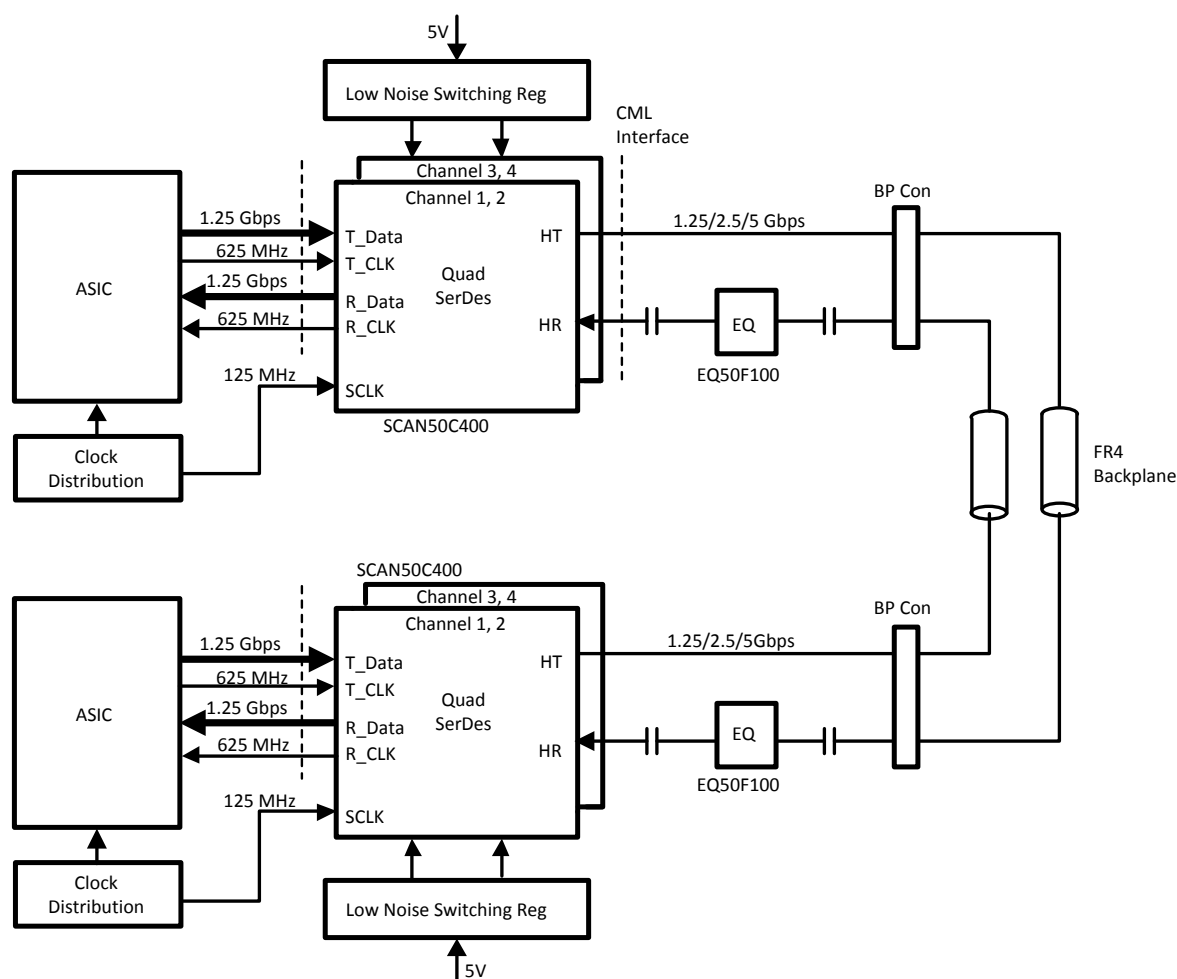
Figure 15. Texas Instruments Total Solution for 5 Gbps Backplane

5   Conclusion

System designers face many challenges in designing multi-gigabit backplanes. Texas Instruments SCAN50C400 quad backplane transceiver and EQ50F100 receive equalizer address these challenges. By managing crosstalk and jitter through careful system designs, legacy backplanes can be upgraded to 5Gbps operation, while minimizing development time and cost.

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