

AN-1391 LM3204 Evaluation Board

1 Introduction

The LM3204 evaluation board is a working demonstration of a buck converter. This document contains information about the board. For further information on buck converter topology and component selection, see the device-specific data sheet.

2 General Description

The LM3204 converts high input voltages to lower output voltages with high efficiency. It does this through a inductor based switching topology, applying the input voltage to the inductor for a certain portion of the cycle. The duty cycle in pulse width modulation (PWM) mode will be V_{OUT} / V_{IN} , which can be seen on the SW pin.

There are three modes of operation. These are fixed frequency PWM, forced bypass, and shutdown mode. Setting the BYP pin low (<0.4 V) or leaving floating places the device in PWM mode. Setting the BYP pin high (>1.2 V) places the device in forced bypass mode. Setting the EN pin low (<0.4 V) places the device in shutdown mode. Setting the EN pin high (>1.2 V) enables normal operation.

At the PWM mode, the output voltage is setting by the voltage of the V_{CON} pin, as in [Equation 1](#):

$$V_{OUT} = 3 \times V_{CON} \tag{1}$$

3 Operating Conditions

The board will operate under the following conditions:

$$2.7 \text{ V} \leq V_{IN} \leq 5.5 \text{ V}$$

$$0.267 \text{ V} \leq V_{CON} \leq 1.2 \text{ V}$$

$$0\text{mA} \leq I_{OUT} \leq 300\text{mA} \text{ (PWM mode)}$$

$$0\text{mA} \leq I_{OUT} \leq 500\text{mA} \text{ (Bypass mode)}$$

4 Schematic

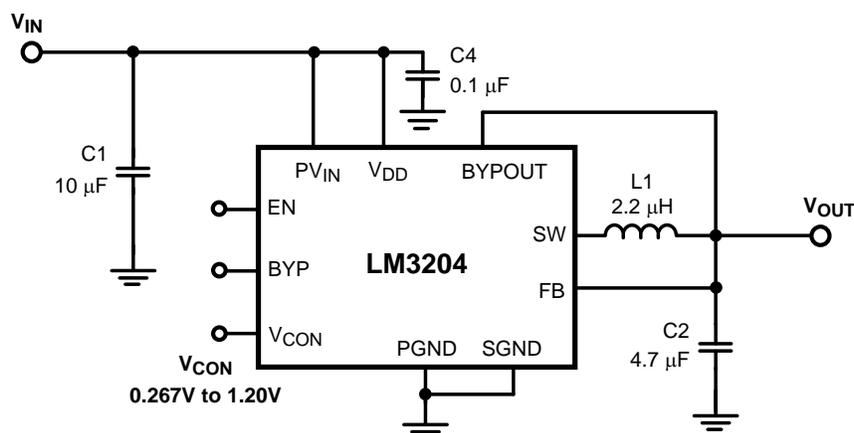


Figure 1. Typical Operating Circuit

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5 Board Layout

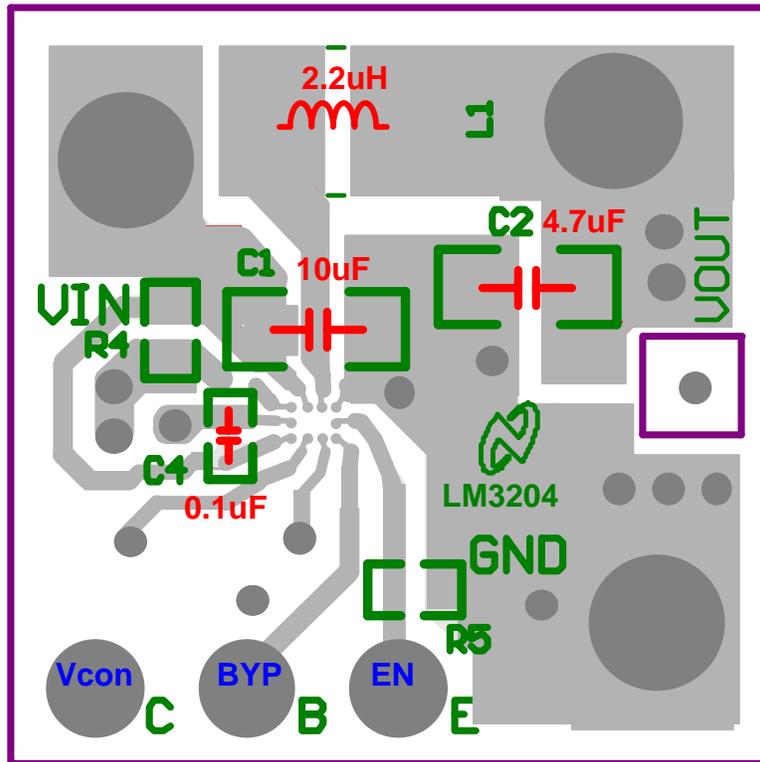


Figure 2. Top Layer

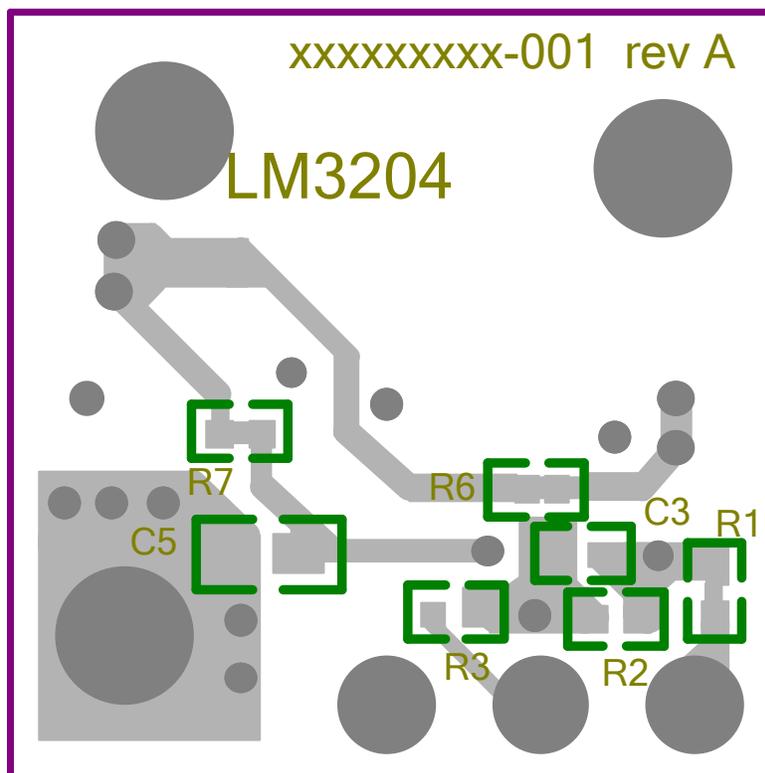


Figure 3. Bottom Layer

6 Board Schematic

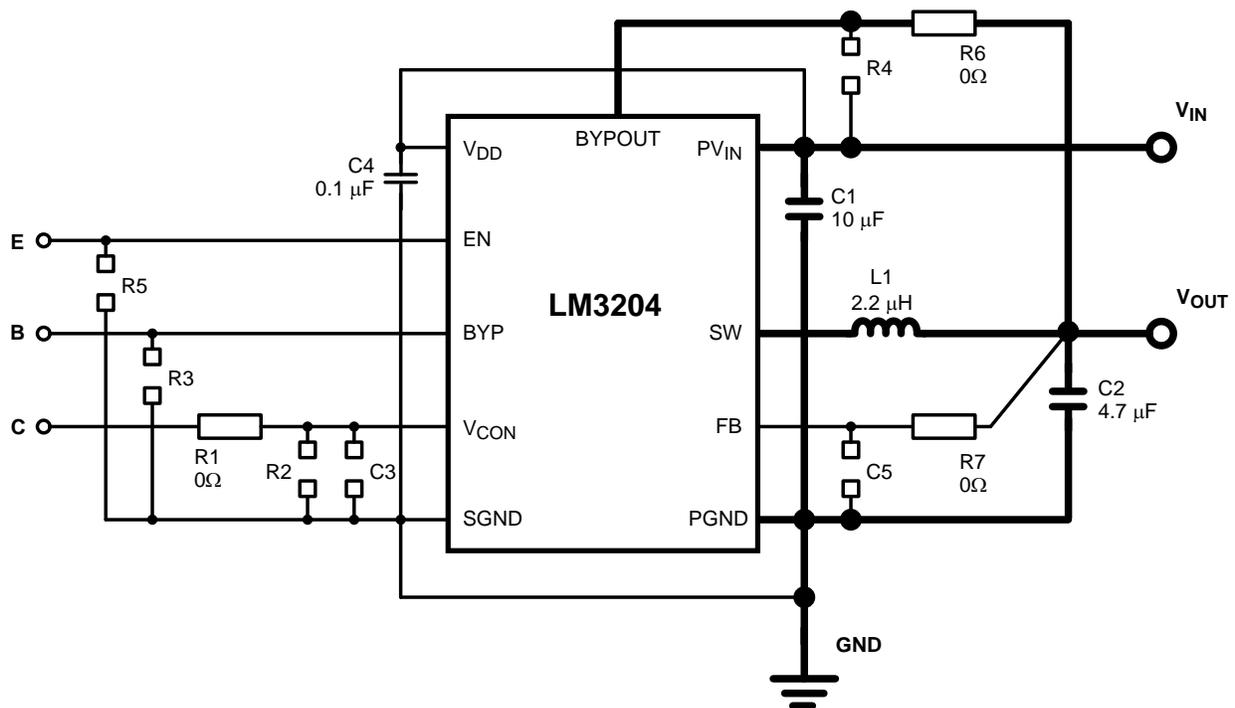


Figure 4. Complete Evaluation Board Schematic

7 PCB Guidelines

For your application circuit, proper layout for the buck regulator should be implemented by following a few simple guidelines. (Also, see the *Board Layout Considerations* section in the device-specific data sheet.)

- Place C1 right next to the device between PV_{IN} and PGND pin.
- Place C4 right next to the device between V_{DD} and SGND pin.
- Make the traces drawn with heavy lines, which are Power lines, as short and as wide as possible.
- Making the traces drawn with heavy lines on the same layer should be good. However, place as many vias as possible if traces are on multiple layers.

8 Bill of Materials (BOM)

Table 1. Bill of Materials

Designator	Footprint	Manufacture	Manufacture #	Description
C1 (input C)	1206 (3216)	TDK	C3216JB1A106K	10 μ F, 10 V, 20%
C2 (output C)	1206 (3216)	TDK	C2012JB0J475K	4.7 μ F, 6.3 V, 20%
C3	0603 (1608)			optional
C4 (input C)	0402 (1005)			0.1 μ F, 10 V, 20%
C5	0805 (2012)			optional
L1 (inductor)		Coilcraft	DO3314-222	2.2 μ H inductor, 1.6A Isat, 0.2 Ω max.
R1	0603 (1608)			0 Ω
R2	0603 (1608)			optional
R3	0603 (1608)			optional
R4				Do not use
R5	0603 (1608)			optional
R6	0603 (1608)			0 Ω
R7	0603 (1608)			0 Ω
COMMON TO ALL				
V _{IN} banana jack - red		Johnson Components	108-0902-001	conn jack banana insul nylon red
V _{OUT} banana jack - yellow		Johnson Components	108-0907-001	conn jack banana insul nylon yellow
GND banana jack - black		Johnson Components	108-0903-001	conn jack banana insul nylon black

9 Connection Diagrams

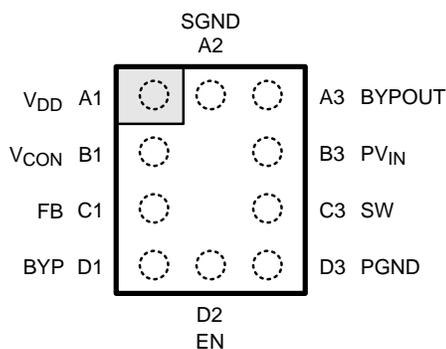


Figure 5. Top View

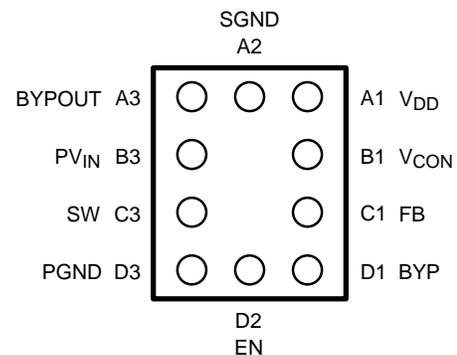


Figure 6. Bottom View

Figure 7. 10-Bump Thin DSBGA Package, Large Bump

Table 2. Pin Descriptions

Pin No	Name	Description
A1	V _{DD}	Analog Supply Input. A 0.1μF ceramic capacitor is recommended to be placed as close to this pin as possible.
B1	V _{CON}	Voltage Control Analog input. V _{CON} controls V _{OUT} in PWM mode. Set: V _{OUT} = 3 x V _{CON} . Do not leave floating.
C1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
D1	BYP	Bypass. Use this digital input to command operation in Bypass mode. Set the BYP pin high (> 1.2 V) for Bypass mode. Set BYP low (< 0.4 V) for normal operation.
D2	EN	Enable Input. Set this digital input high (> 1.2 V) after V _{IN} > 2.7 V for normal operation. For shutdown, set low (< 0.4 V).
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3204.
B3	PV _{IN}	Power Supply Voltage Input to the internal PFET switch and Bypass FET.
A3	BYPOUT	Bypass FET Drain. Connect to the output capacitor. Do not leave floating.
A2	SGND	Analog and Control Ground

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