AN-1428 LM3370 Evaluation Board

1 Introduction

The LM3370 evaluation board is a working demonstration of a DUAL step down DC-DC converter. This application note contains information about the evaluation board. For more details and electrical characteristic on the dual buck converter operation, see the *LM3370 Dual Synchronous Step-Down DC-DC Converter with Dynamic Voltage Scaling Function Data Sheet* (SNVS406).

2 General Description

The LM3370 is a dual step-down DC-DC converter optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. Automatic intelligent switching between PWM low-noise and PFM low current mode offers improved system efficiency. The I^2C compatible offers dynamic controls of the output voltages, Auto PFM/PWM mode selection and other enabling enchantment features such as power-on-reset (nPOR) and spread spectrum.

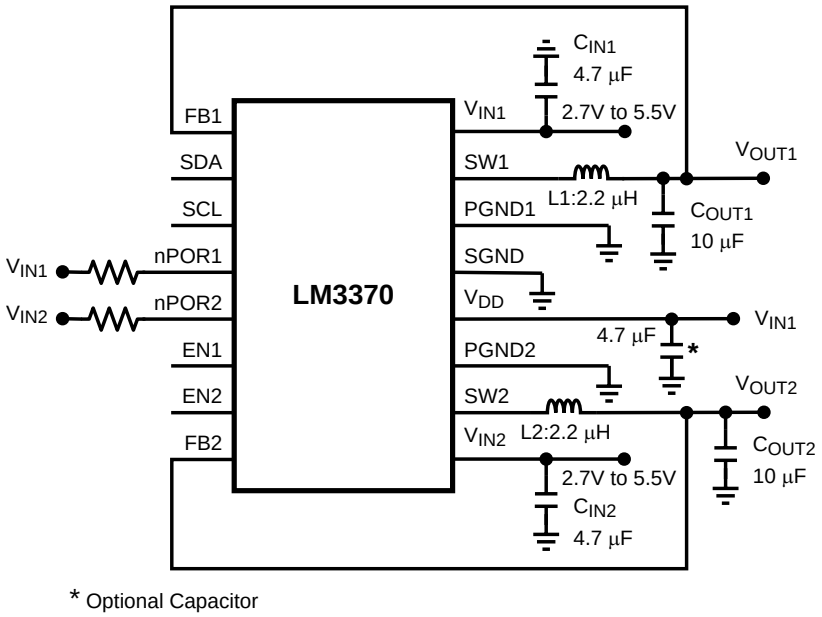
3 Operating Conditions

- V_{IN} range: 2.7V ≤ V_{IN} ≤ 5.5V
- Recommended load current: 0 to 600mA

  I^2C Compatible Interface
- V_{OUT1} (1V to 2V at 50mV step increment)
- V_{OUT2} (1.8V to 3.3V at 100mV steps increment).

  Package
- TLA20CWA micro SMD, (3.0mm x 2.0mm x 0.6mm)
- LLP16 non-pullback, (4mm x 5mm x 0.8mm)

4 Typical Application



* Optional Capacitor

Figure 1. Typical Application Circuit

5 Operating Information

The LM3370SD evaluation board is pre-programmed to 1.2V at V_{OUT1} and 3.3V at V_{OUT2} for evaluation purpose (no additional interface hardware is needed). If different default output option is desired, the same evaluation board can be used to demount the existing device and replace with a new voltage option (voltage option can be ordered from TI's website at www.ti.com).

The device comes with the following default setting: Auto PFM and PWM transition mode when the I^2C compatible interface is not enabled. For other settings, I^2C compatible interface must be used to enable all other functions. Registers information are listed on page 4 for I^2C compatible interface.

6 Powering Up the Evaluation Board

- Apply a voltage at the "Vin_EXT" pin only (not Vin_IO).
- All logic pins are tied to "Vin" on the evaluation board
- Do not power the “Vin_IO” pin unless powering the logic pins via an external source. (Jumper at Vin_IO must be removed.)
- V_{DD} pin is tied to V_{IN1} & V_{IN2} on the evaluation board, no additional connection required. (For any reason if V_{DD} is not directly tied to V_{IN}, V_{DD} needs to be equal or greater than the two inputs (V_{IN1} or V_{IN2}) for proper operation.)

7 I^2C Interface Ready

If interface capability is available via I^2C compatible, the SDA & SCL test pins of the evaluation board are brought out for such function. The SDA & SCL pins of the evaluation board are connected to 2 kΩ resistors and pulled up to V_{IN} pin.

8 Package Marking Information

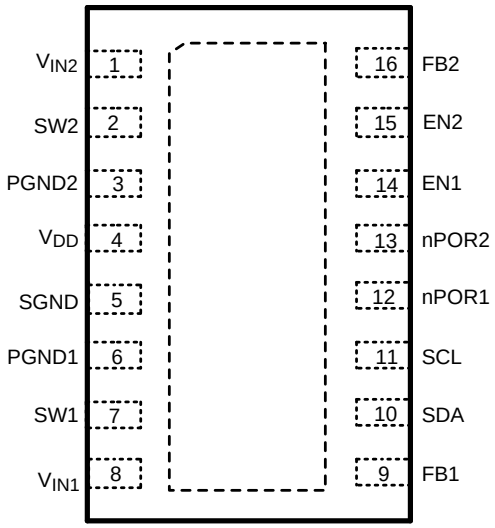


Figure 2. Top View

9 Pin Descriptions (WSON)

Table 1. Pin Descriptions (WSON)

1	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck2
2	SW2	Buck 2 Switch pin
3	PGND2	Buck 2 Power Ground
4	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} or V_{IN2})
5	SGND	Signal GND
6	PGND1	Buck 1 Power Ground
7	SW1	Buck 1 Switch pin
8	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck1
9	FB1	Analog feedback input for Buck 1
10	SDA	I^2C Compatible Data, a 2 kΩ pull up resistor is required
11	SCL	I^2C Compatible Data, a 2 kΩ pull up resistor is required
12	nPOR1	Power ON Reset for Buck 1, Open drain output low when Buck 2 output is 92% of target output. A 100 kΩ pull up resistor is required
13	nPOR2	Power ON Reset for Buck 2, Open drain output low when Buck 2 output is 92% of target output. A 100 kΩ pull up resistor is required
14	EN1	Buck 1 Enable
15	EN2	Buck 2 Enable
16	FB2	Analog feedback input for Buck 2

10 Package Marking Information (DSBGA)

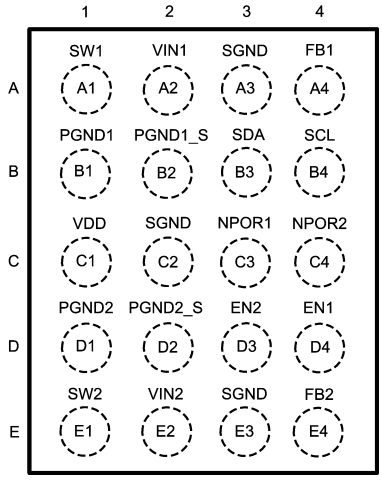


Figure 3. Top View

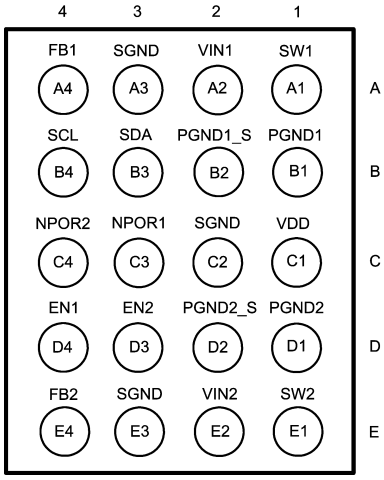


Figure 4. Bottom View

11 Pin Descriptions (DSBGA)

Table 2. Pin Descriptions (DSBGA)

Pin No	Name	Description
A1	SW1	Buck 1 Switch Pin
A2	V_{IN1}	Power supply voltage input to PFET and NFET switches for Buck 1
A3	SGND	Signal GND
A4	FB1	Analog Feedback Input for Buck 1
B1	PGND1	Buck 1 Power Ground
B2	PGND1_S	Buck 1 Power Ground Sense
B3	SDA	I^2C Compatible Data, a 2 kΩ pull up resistor is required
B4	SCL	I^2C Compatible Clock, a 2 kΩ pull up resistor is required
C1	V_{DD}	Signal supply voltage input, V_{DD} must be equal or greater of the two inputs (V_{IN1} & V_{IN2})
C2	SGND	Signal GND
C3	nPOR1	Power ON Reset for Buck 1, Open drain output Low when Buck 1 output is 92% of target output. A 100 kΩ pull up resistor is required
C4	nPOR2	Power ON Reset for Buck 2, Open drain output Low when Buck 2 output is 92% of target output. A 100 kΩ pull up resistor is required
D1	PGND2	Buck 2 Power Ground
D2	PGND2_S	Buck 2 Power Ground Sense
D3	EN2	Buck 2 Enable
D4	EN1	Buck 1 Enable
E1	SW2	Buck 2 Switch Pin
E2	V_{IN2}	Power supply voltage input to PFET and NFET switches for Buck 2
E3	SGND	Signal GND
E4	FB2	Analog feedback for Buck 2

Table 3. Output Selection Table via I²C Programing

Buck Output Voltage Selection Codes		
Data Code	**Buck_1 (V)**	**Buck_2 (V)**
00000	NA	NA
00001	NA	1.8
00010	NA	1.85 or 1.9(1)
00011	NA	2.0
00100	NA	2.1
00101	1.00	2.2
00110	1.05	2.3
00111	1.10	2.4
01000	1.15	2.5
01001	1.20	2.6
01010	1.25	2.7
01011	1.30	2.8
01100	1.35	2.9
01101	1.40	3.0
01110	1.45	3.1
01111	1.50	3.2
10000	1.55	3.3
10001	1.60	NA
10010	1.65	NA
10011	1.70	NA
10100	1.75	NA
10101	1.80	NA
10110	1.85	NA
10111	1.90	NA
11000	1.95	NA
11001	2.00	NA

(1) Can be trimmed at the factory at 1.85V or 1.9V using the same trim code.

12 Registers Information

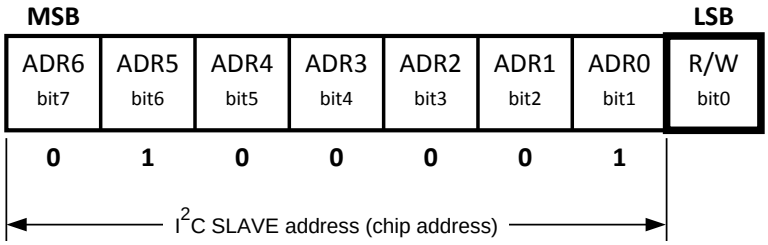


Figure 5. Device Address

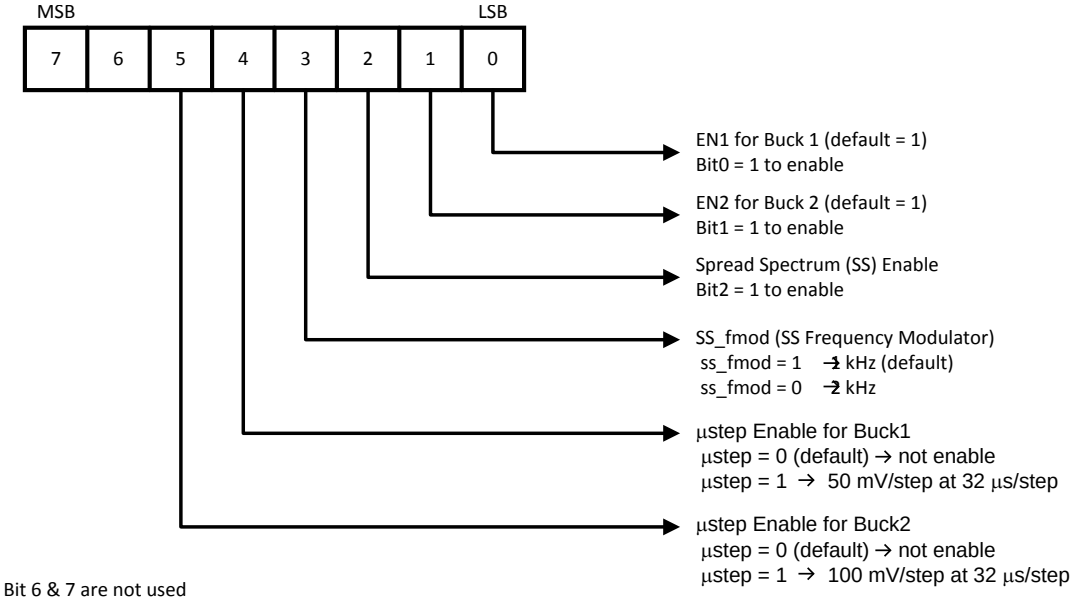


Figure 6. Register 00

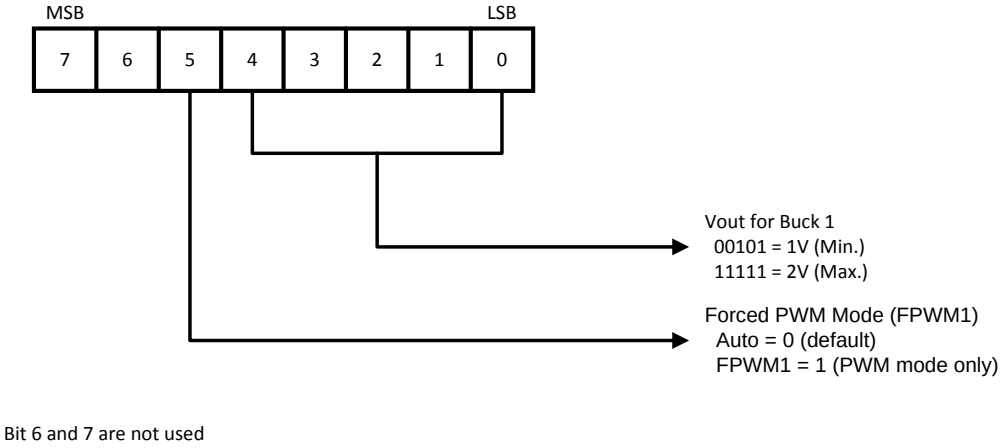


Figure 7. Register 01

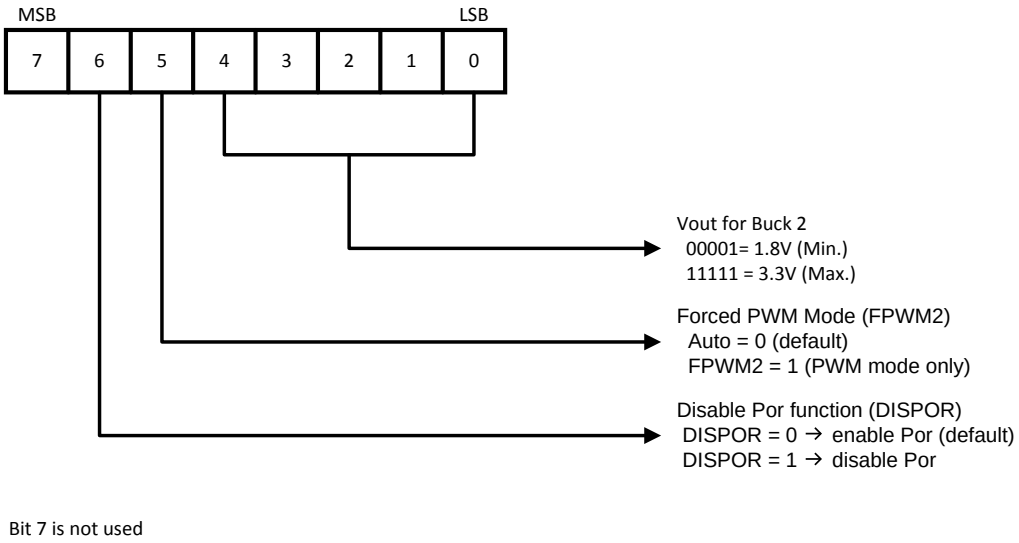


Figure 8. Register 02

13 Evaluation Board Layout (WSON)

LM3370SD is a 4-layer board designed to maximize the performance fo the device.

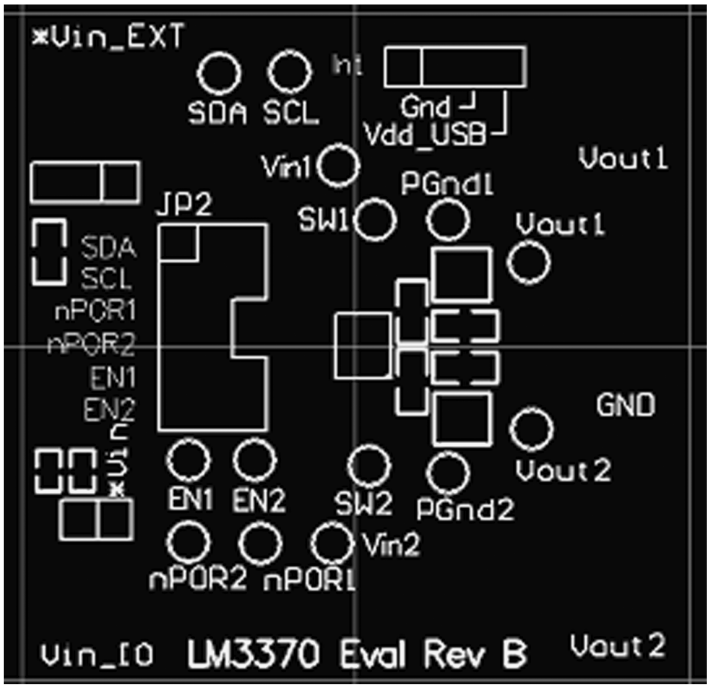


Figure 9. Silk Screen

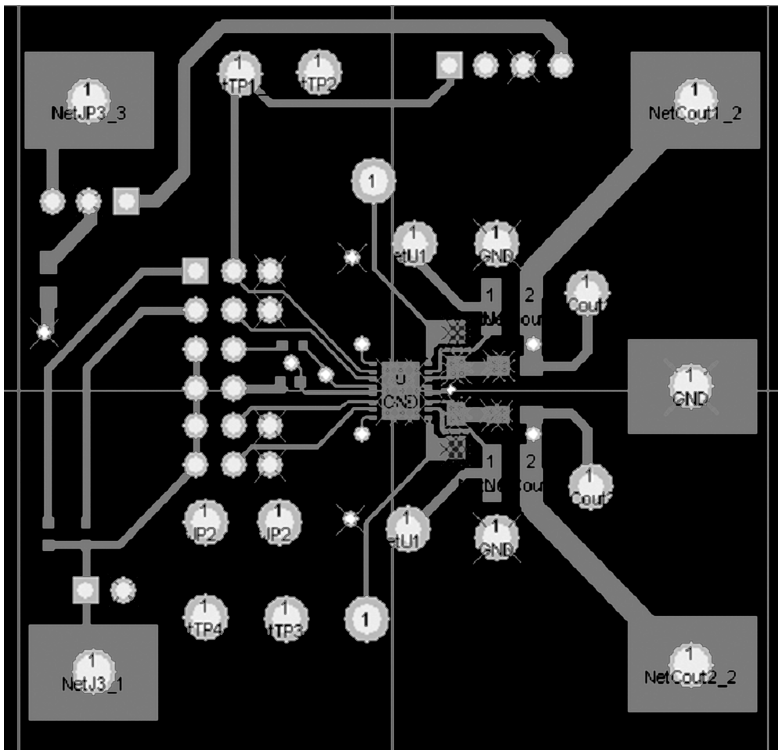


Figure 10. Top Layer

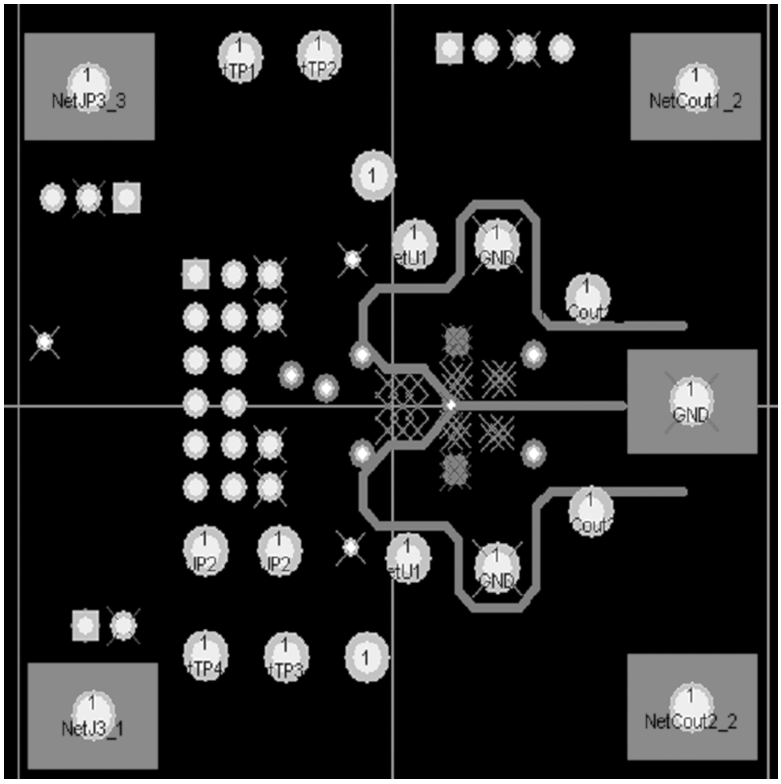


Figure 11. Mid Layer 1

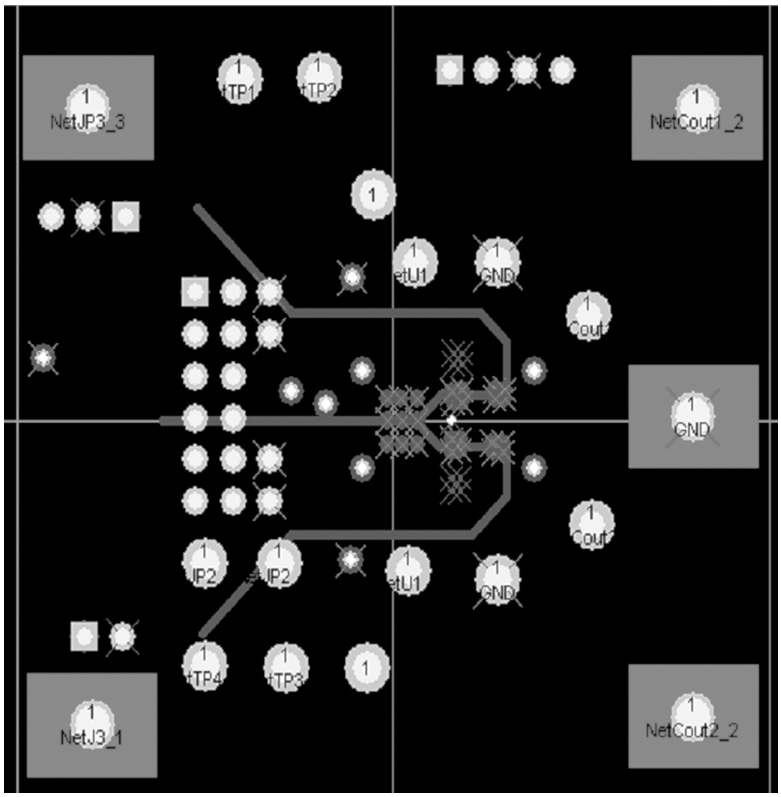


Figure 12. Mid Layer 2

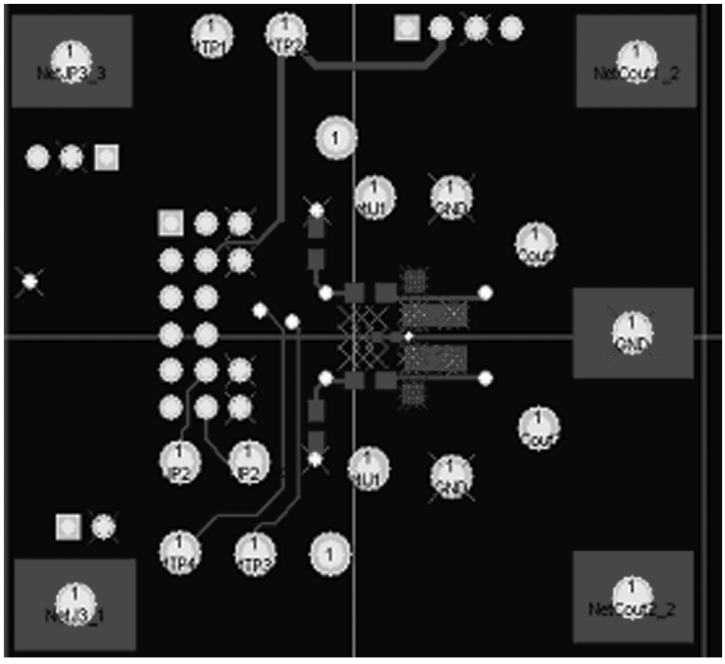


Figure 13. Bottom Layer

14 Evaluation Board Layout (DSBGA)

The LM3370TL applications is of similar layout to the LLP board with the exception of the SCL, SDA pins. When using the USB interface cable the order of these pins is reversed.

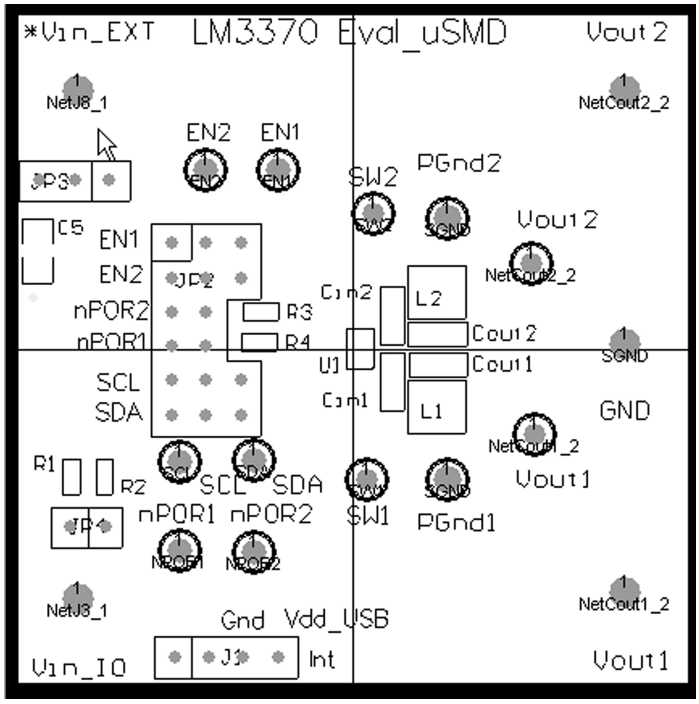


Figure 14. Silk Screen

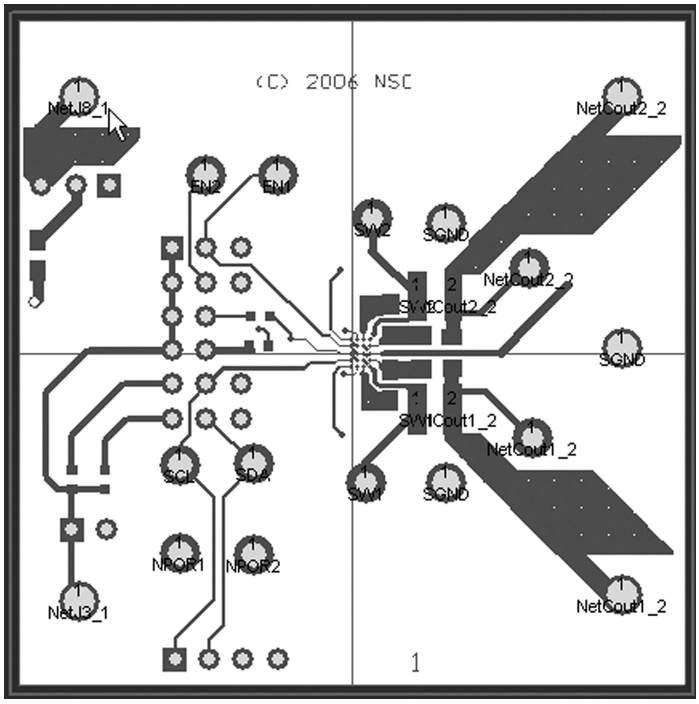


Figure 15. Top Layer

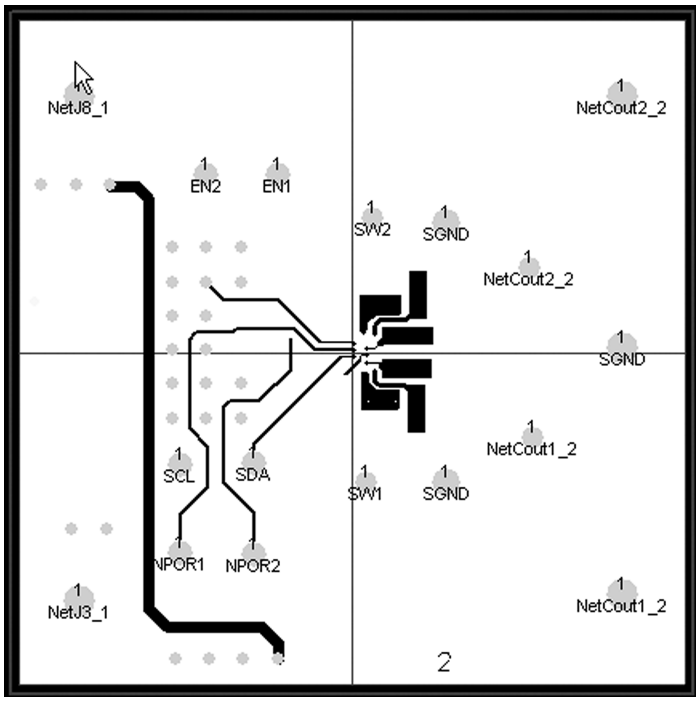


Figure 16. Mid Layer 1

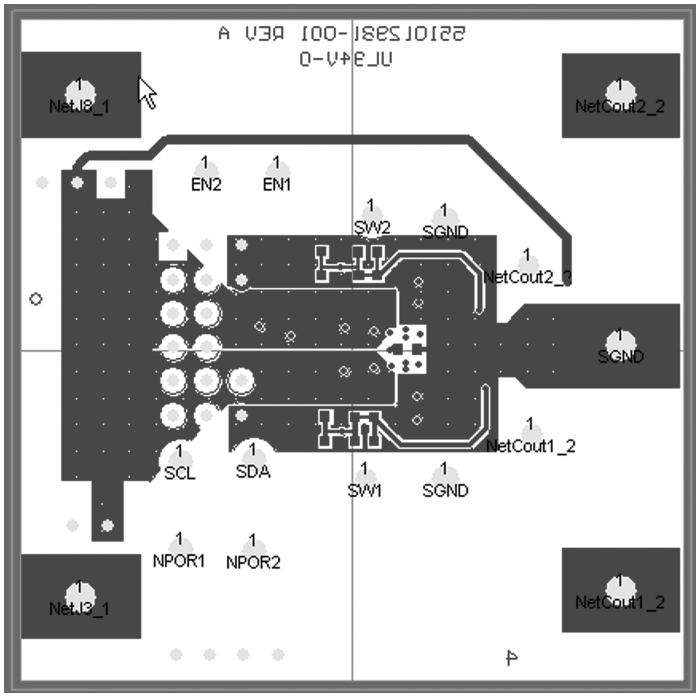


Figure 17. Bottom Layer

15 Bill of Materials (BOM)

Component Name	Manufacture	Manufacture No		Specification
LM3370				
C_{IN1} and C_{IN2}	TDK	C2012X5R0J475K		4.7µF/6.3V/0805/X5R
	muRata	GRM219R60J475KE19D		
C_{OUT1} and C_{OUT2}	TDK	C2012X5R0J106K		10µF/6.3V/0805/X5R
	muRata	GRM219R60J106KE19D		
L1 & L2	Taiyo-Yuden	NR3015T-2R2M		2.2µH
R1-2(SDA+SCL)	Vishay			2k Ωs
R3-4 (nPOR1-2)	Vishay			100k Ωs
TEST Pins and Connectors				
V_{OUT1},V_{OUT2}, GND, *Vin_EXT, Vin_IO				Turret 0.09 in
nPOR1. nPOR2, SDA, SCL, PGND1, PGND2, V_{IN1}, V_{IN2},				Turret 0.072 in
Jumper				
SDA/SCL/nPOR1	Jumpers Female(Handle centerline)			A26242-ND
nPOR2/EN1/EN2				
*VIN & *VIN_IO				
*VIN_IO	Berk stick		Header	2 in series (2x1)
*VIN_EXT				2 in series (2x1)
Int				4 in series (4x1)
JP2:SDA & SCL				6 in series(6x2)
nPOR1/ nPOR2/EN1& EN2				2 in series 2(2x1)

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