

AN-1608 Powering Portable Media Players (PMP) With Innovative Solutions

ABSTRACT

Understanding Portable Media Players system and power requirements are keys to selecting power designs for fast time-to-market constraints. PMICs such as the LP3910 address both the needs and the challenges implementing power solutions.

This complete device features buck-boost for HDD, DVS for system power savings, power sequencing for multiple rails, Li-Ion battery charger and battery monitoring. This integrated solution not only powers PMPs effectively, it is also an ideal space-saving solution by reducing the number of regulators with the ability to handle multiple tasks for advanced designs with many requirements. Using the new PMIC's, power designers can meet the challenges required in a wide variety of portable devices, while increasing performance.

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Introduction

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1 Introduction

In the past, when system designers were handed a project, they basically purchased off-the-shelf discrete power solutions from the various vendors. The list of issues the power designer must consider has greatly increased as power systems have become more complicated. Some of the key areas where these new design challenges exist are:

- Multiple outputs due to feature-rich devices, LDOs, Bucks, battery chargers; overall more control of the system is required to obtain better efficiencies during battery operation.
- To ensure stable multiple voltage supplies to the host processor, IC systems now require increased flexibility, programmability, and power sequencing to allow for powering down unused power functions when left unused.
- Finding an easy to implement, correct and easy-to-use power management solution can become a critical part of rapid system development and improved cycle time-to-market.
- By having a high level of integration in such a PMIC reduces overall system cost and size constraint significantly when compared to equivalent discrete solutions.
- Extending battery life now requires higher efficiencies and dynamic voltage scaling (DVS) to reduce overall power consumption.

2 General Description

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The system diagram in Figure 1 details the many power requirements of a typical personal media player (PMP). Using smart power control in your design can yield improved performance in many areas including:



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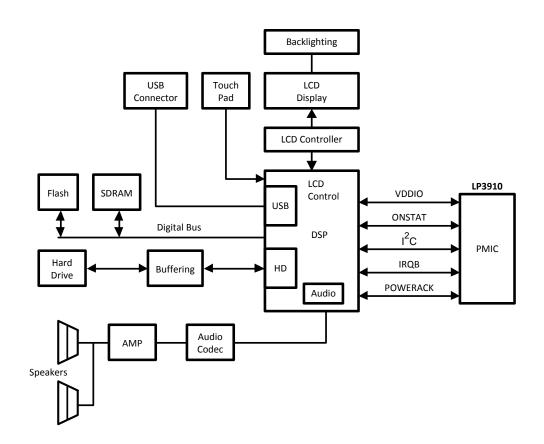


Figure 1. Portable Media System Level Diagram

- Digital signal processor
- Hard drive for storage of the downloaded media
- · Touch pad to select software driven functions of the media player
- LCD display
- Audio amplifier
- Audio Codec
- Flash memory used to store the operating system; upon system boot up of the DSP, the bootloader instructs the DSP to download the OS image from Flash to the SDRAM
- SDRAM storage of the OS image, SDRAM has faster access time than flash so the DSP can access information quickly
- USB interface to download music content from a computer

Many of these challenges can be seen when designing in power requirements for PMPs. These devices have a multitude of constraints and unique needs that can be better handled when using smart, programmable power controllers. Section 3 includes details of the design specifics on powering the main subsystems. Section 3 discusses the integration of various power and control functions into a common IC can solve system issues such as: powering subsystems, digital application/peripheral, audio amplifier block, DSP (I/O, Core), and memory, hard disk drive, and LCD backlight display.



Operation

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In Section 4, key features that affect design and power management are reviewed such as: battery charging and monitoring, battery charger linear charger, smart control parameters, power prioritization routing, power sequencing, soft-start, and communication between the PMIC and the DSP.

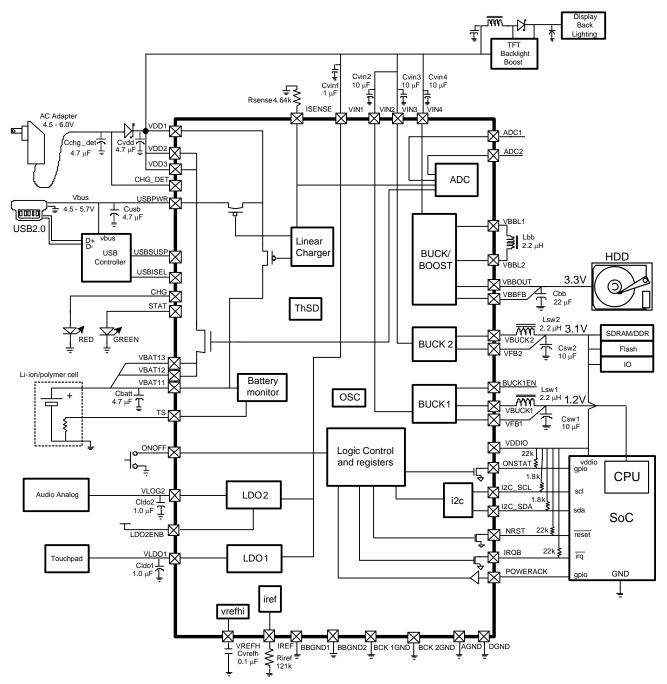


Figure 2. Detailed Power Requirements for a Portable Media Player System

3 Operation

3.1 Powering the Digital Application/Peripheral

Typically Low Drop Out (LDO) regulators are used to power digital peripherals. Voltages are usually 1.2 V to 3.3 V with a current requirement of 150 mA. Good external output filtering is also required. Digital loads require LDOs to have good load transient response to keep the output voltage in regulation.



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3.2 Powering the Audio Amplifier Block

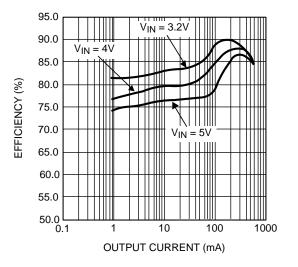
An LDO is required in this application as the noise generated from a switch mode supply will introduce excessive noise into sensitive analog circuits. Here, the important parameter to consider is the power supply rejection ratio (PSRR). If transients on the power supply line are not suppressed, harmonics will appear at the speaker output. Attention to good output filtering and PCB layout is important.

3.3 Powering the DSP (I/O, CORE), and Memory

Typically, magnetic buck switching regulators are used to power the DSP and memory due to the high load demand and high efficiency requirement.

Buck 1 and 2 are high efficiency synchronous FET (low rds) switching regulators. A multiphase switching scheme has been implemented such that NFET, and PFET of buck 1 are turned on/off at fixed phase intervals in time, which are different to that of buck 2 using counter logic. This reduces the overall demand from the main DC source or battery.

The output voltages can be changed via I²C if dynamic voltage scaling is required. The concept is to dynamically scale the output voltage up or down based on the load demand at that moment in order to maximize the overall system power saving. For example, when the DSP is running in a mode where it is reading or writing large amounts of data to memory or doing intensive numerical calculations where the power needs to change dramatically. By using the I²C the voltages can be changed. Once the function is completed the DSP informs the PMIC to go back to the lower voltage setting. This type of power management technique increases the longevity of the battery. The bucks operate at 2 MHz, which means the physical dimensions of the external inductor are considerably reduced. Figure 3 shows a typical efficiency plot for a magnetic switching buck regulator.





3.4 Powering the Hard Disk Drive

The Buck-Boost is required when extending the device runtime 3.3 V for the hard drive during battery operation. This voltage is lower than the maximum battery of 4.2 V and higher than the minimum battery of 2.8 V. In addition it needs to supply a peak current initially of about 500 mA for the motor on the hard drive spindle to turn. During read write cycles to the hard drive the current averages about 200 mA.



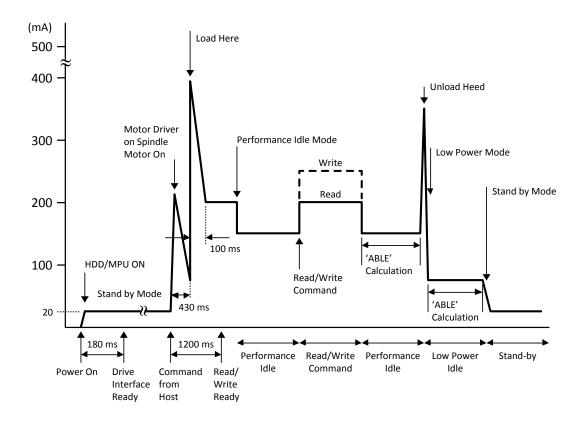


Figure 4. Hard Drive Load Demand During Start Up and Normal Read Write Operation

3.5 Powering the LCD Backlight Display

A Boost circuit is required to power the LCD backlight display. This is required to produce a large voltage, which tends to be greater than the supply voltage for the lighting supply to the LCD display. A magnetic or switched capacitor boost regulator can be used as an LED backlight driver.

4 **Connection Descriptions**

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4.1 **Battery Charging and Monitoring**

The A/D converter multiplexes the battery voltage and the battery charger current.

Battery voltage measurement is then scaled and can be used to monitor the battery voltage during (constant current, constant voltage) charging, or when the battery is being used in the system.

If the Li-lon battery voltage drops below the battery low threshold voltage, the battery low alarm interrupt is pretriggered prior to event occurring, by setting a "voltage low-value threshold" higher than the battery-low alarm. The DSP is informed earlier so that it can take precautions before the battery voltage drops and causes a system failure. This informs you that the battery needs to be charged via the DC source, otherwise the system will gracefully shutdown without the loss of media content.



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A dual voltage comparator with hysteresis prevents battery chattering. Once the battery trips the low threshold, it is disengaged from the system. However, the battery voltage can float back up. By setting the hysteresis window with a high enough upper threshold, the battery cannot re-power the system.

4.2 Battery Charger Linear Charger

Prequalification mode is the mode when the battery is charged, at a lower current rate initially about 10% of the full rate if a DC source is connected. The reason for this is, if the battery is damaged and full charging is initiated, this could create a potentially hazardous condition. In addition, the battery has a low effective standard resistance by charging the battery at full rate could create a voltage spike on the battery, creating a false condition that the battery is fully charged. This mode terminates once the full rate charging voltage is reached, typically 2.85 V.

The module provides CC charging and CV charging to charge the battery. Full charging mode occurs once the pre-qualification charging is completed. In CC mode, the appropriate battery charging current is supplied.

In CV mode, the voltage on the battery increases rapidly during the full charging mode. Once it reaches the programmable termination voltage, which is typically 4.1 V, it is complete – known as EOC.

Top off mode enables once the battery is in the EOC cycle, which is about 5% to 10% of the full rate charge. CV charging continues a little longer to squeeze more capacity into the battery.

The beauty of the integrated charger in the PMIC is that status of the battery charger can be accessed via internal registers. There is no need to write firmware (Microcontroller or DSP) to control the battery charger, as its intelligence is self contained where the DSP acts upon the messages and takes the appropriate action.

4.3 Power Prioritization Routing

Power routing allows system usage immediately after an external power source has been detected. System power takes precedence over the battery charging, so when the user has the DC source connected and wants to use the device, power from the DC is allocated to the normal operation of the media player, whatever power is leftover is used for charging the battery.

Battery disconnect is a feature that allows longer battery shelf life in products. When the system is being shipped, the unit uses the "disconnect circuit" that prevents discharging of the battery. You "open" the circuit by simply connecting DC source to the media player, where the DSP wakes up and connects the battery as necessary.

4.4 PMIC Enables Power Sequencing

Power sequencing of the supplies occurs when there are multiple voltage domains where the highest voltage needs to come on first (typically the I/O pins) followed by all the other voltage rails in a high to low order sequence. With the DSP core being last. In addition one supply rail is not to exceed another by more than a diode drop; otherwise, excessive current flow backward from the I/O voltage through the IC, into the lower voltage DSP core. From a system standpoint, the power supplies need to be present in a particular sequence and handshaking and acknowledgment signals between the DSP and the PMIC need to occur for this to happen.

4.5 Soft-Start

Soft start provides a smooth linear ramping of the buck regulator's output voltage. By actively limiting the inrush current to the active devices gives the system added reliability.

4.6 Communication Between the PMIC and the DSP

I²C interface bus permits communication between the DSP master to the PMIC slave via a clock and data line. Registers can be read over this communication link and information on the status of the overall system can be proactive with this data.



Connection Descriptions

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The PMIC has the ability to interrupt the DSP through the IRQB open drain pin, which transitions to a logic low level upon the following events: removal and insertion of the DC source, USB power detected and disconnected, battery low alarm, thermal alarm, ADC conversion completed, charger safety timeout (after 10 hours of charging.)

Once an event occurs, the DSP can then read the interrupt register bits via I²C and then service them appropriately. This interrupt message can be relayed to the application software layer informing the user an event has occurred.

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