Application Report
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# LP8860-Q1 Boost Compensation Registers

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**ABSTRACT**

The LP8860-Q1 device is an automotive LED driver with boost converter to support infotainment display, automotive cluster, and lighting applications. In order to support a wide range of application conditions for automotive, the LP8860-Q1 offers various settings for boost compensation with EEPROM registers. This document provides additional details for several device EEPROM registers and expands on descriptions in the *LP8860-Q1* data sheet.

**Contents**



**List of Figures**



**List of Tables**



## Trademarks

# 1 Boost Compensation Registers of LP8860-Q1

**Table 1. Boost Compensation Registers**

| EEPROM addr(Hex) | Bit | Name | Data Sheet Description |
|---|---|---|---|
| 70 | 5 | BOOST_EN_IRAMP_DELAY | Boost current ramp delay enable (for adjusting conversion ratio/stability, 35% of period) |
| 71 | 6:5 | BOOST_SEL_IND | Boost artificial current ramp peak value, A/s. Select value higher than $I_{RAMP\_GAIN}$: $I_{RAMP\_GAIN}$ =1.2 × 0.5 × ($V_{OUTmax}$ – $V_{INmin}$) / (0.7 x L × 60000), where $V_{IN}$, $V_{OUT}$ are boost input and output voltage, L - inductance, H. 25-mΩ $R_{SENSE}$ is suggested |
| | 4:3 | BOOST_SEL_IRAMP | |
| 74 | 7:6 | BOOST_LLC_SEL | Light load comparator control. Selects boost PFM entry threshold (compensator current) |
| | 5:4 | BOOST_SEL_JITTER_FILTER | Boost jitter filter selection |
| | 3:2 | BOOST_SEL_I | Boost PI compensator control: integral part |
| | 1:0 | BOOST_SEL_P | Boost PI compensator control: proportional part |
| 75 | 7:6 | BOOST_OFFTIME_SEL | Boost time off selection |
| | 5:4 | BOOST_BLANKTIME_SEL | Boost blank time selection |

## 1.1 EEPROM Address 0x70[5] - BOOST_EN_IRAMP_DELAY

Boost artificial current ramp ($I_{RAMP}$) is disabled for the first 35% of period for every switching cycle when the bit is high. This gives more margin of boost compensator current from the given minimum available compensator current decided by the boost design. This can be useful at low switching frequency (a few hundred kHz) where required compensator current is higher than high switching frequency; hence, low switching frequency tends to have less current margin from the minimum available compensator current.

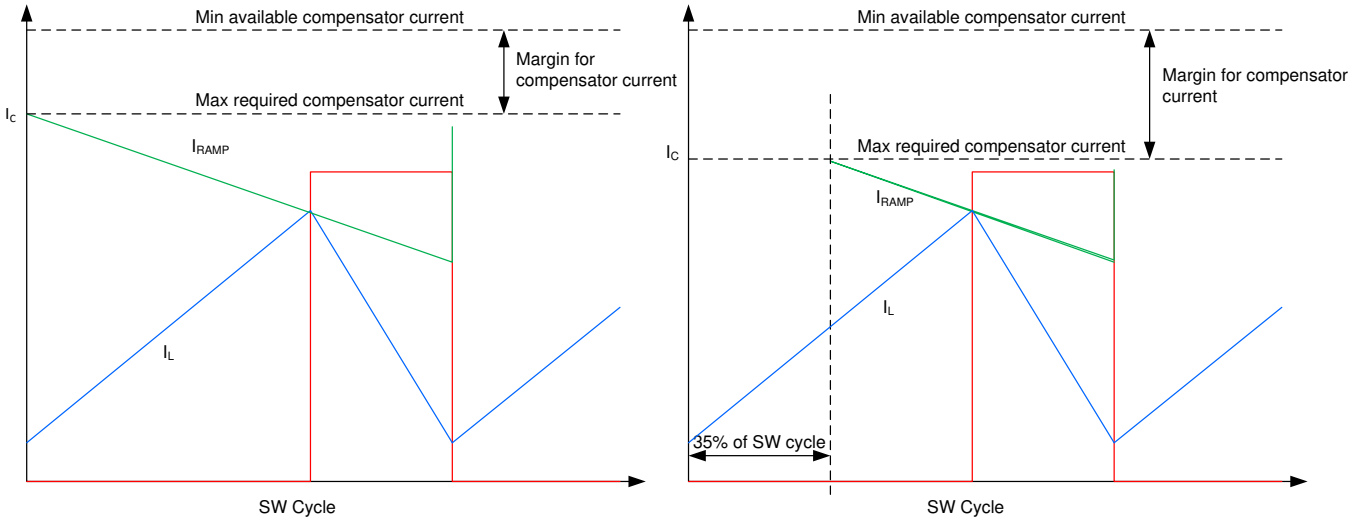


**Figure 1. Boost $I_{RAMP}$ Delay Function**

**Recommended setting:** Enable this function for low switching frequency (100 kHz to 600 kHz) while monitoring the boost output waveform. If boost output waveform is stable and reaches target voltage at maximum load condition, this function is not needed.

## 1.2 EEPROM Address 0x71[6:3] – BOOST_SEL_IND, BOOST_SEL_IRAMP

Boost artificial current ramp ($I_{RAMP}$ shown in Figure 1) peak value, A/s. For a peak current mode boost converter without an artificial current ramp, sub-harmonic oscillation occurs with a duty cycle > 50%. By adding a current ramp greater than the down slope of the inductor current, the oscillation can be damped. Use Equation 1 to calculate required $I_{RAMP\_GAIN}$:

$$I_{RAMP\_GAIN} = 1.2 \times 0.5 \times (V_{OUTmax} - V_{INmin}) / (0.7 \times L \times 60000) \quad (1)$$

where

- L : Inductance

**Recommended setting:** Select 20% or a little higher value than calculated value from Table 2.

**Table 2. Boost $I_{RAMP}$ Settings**

| | BOOST_SEL_IND[1:0] | | | |
|---|---|---|---|---|
| **BOOST_SEL_IRAMP[1:0]** | **00** | **01** | **10** | **11** |
| **00** | 130 | 65 | 34 | 29 |
| **01** | 88 | 43 | 23 | 20 |
| **10** | 56 | 28 | 15 | 13 |
| **11** | 37 | 18 | 10 | 8.5 |

## 1.3 EEPROM Address 0x74[7:6] – BOOST_SEL_LLC

BOOST_SEL_LLC is a light load comparator control — it selects boost PFM entry threshold. The load current of entering PFM is a function of the LLC setting, the slope of artificial current ramp, and inductor current ramp. Lower current value sets PWM operation threshold to lighter load.

00 = 5 µA (boost switches from PFM to PWM early at light loads)

01 = 10 µA

10 = 15 µA

11 = 20 µA (boost operates in PFM mode to higher loads)

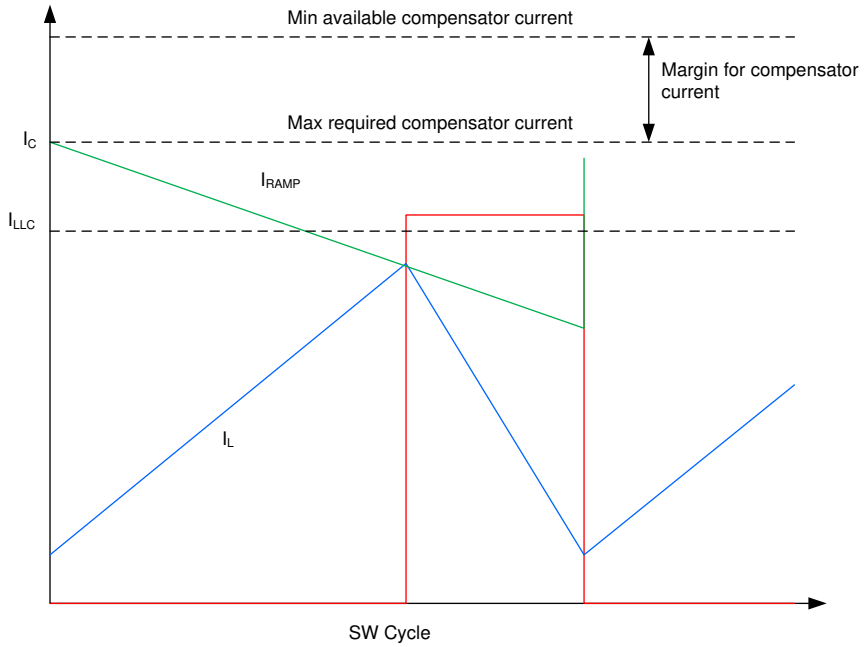


**Figure 2. Boost LLC Current Setting**

**Recommended setting:**

- High LLC setting : efficiency ↑, chance of audible noise ↑(high $V_{OUT}$ ripple by PFM mode switching)
- Low LLC setting : efficiency ↓, chance of audible noise ↓(low $V_{OUT}$ ripple by PWM mode switching)
- For automotive applications, audible noise matters more than efficiency; therefore, the lowest LLC is recommended.

### 1.4 EEPROM Address 0x74[5:4] – BOOST_SEL_JITTER_FILTER

EEPROM Address 0x74[5:4] is a low-pass filter added on the internal FB signal to filter out noise to improve output switching jitter:

00 = bypass

01 = 300 kHz

10 = 60 kHz

11 = 30 kHz

**Recommended setting:** Use the default value (may vary with EEPROM versions). A higher setting (lower frequency) can lower the phase margin of AC loop.

### 1.5 EEPROM address 0x74[3:0] – BOOST_SEL_I, BOOST_SEL_P

EEPROM address 0x74[3:2] BOOST_SEL_I controls the DC gain of loop control.

EEPROM Address 0x74[1:0] BOOST_SEL_P controls the proportional term of the loop.

**Recommended setting:** Use default value(01b) for both BOOST_SEL_I[1:0] and BOOST_SEL_P[1:0], which is an optimal value from simulation and IC validation. Avoid using any other values.

### 1.6 EEPROM Address 0x75[7:6] – BOOST_OFFTIME_SEL

EEPROM Address 0x75[7:6] sets the off time of every boost switching period to control the maximum duty ratio of boost:

00 = 131 ns

01 = 68 ns

10 = 38 ns

11 = 24 ns

**Recommended setting:** An off-time that is too high limits boost duty ratio, which limits conversion ratio. Calculate required boost duty ratio at target switching frequency, and select off-time to make possible duty ratio higher than required value.

Example: $V_{IN}$ = 9 V, $V_{OUT}$ = 35 V, switching frequency = 2.2 MHz

- Required duty ratio = (35 – 9) / 35 = 74.3%
- T of 2.2 MHz = 454 ns
- If setting is 00b = 131 ns, maximum duty ratio = (454 – 131) / 454 = 71.1%, so this setting cannot be selected.
- If setting is 01b = 68 ns, maximum duty ratio = (454 – 68) / 454 = 85%, so this setting can be selected; however, actual efficiency will be less than 100%, and this increases the required duty ratio, so a shorter off-time setting (38 ns) is a safer choice.

TI recommends using one step shorter off-time setting than the calculated value. However, avoid using the minimum off-time setting (24 ns). This setting often violates the conditions of maximum duty ratio of boost, and the operation can be unstable.

### 1.7 EEPROM Address 0x75[5:4] – BOOST_BLANKTIME_SEL

EEPROM Address 0x75[5:4] sets the minimum on-time of every boost switching period to control the minimum duty ratio of boost:

00 = 162 ns

01 = 88 ns

10 = 63 ns

11 = 40 ns

**Recommended setting:** Blank time that is too high limits lowest output voltage. Calculate the minimum required boost duty ratio at target switching frequency and select blank-time value to make the possible duty ratio lower than the required value.

Example: $V_{IN}$ = 18 V, $V_{OUT}$= 25 V, switching frequency = 2.2 MHz

- Required duty ratio = (25 – 18) / 25 = 28%
- T of 2.2 MHz = 454 ns
- If setting is 00b = 162 ns, minimum on duty ratio = 162 / 454 = 35.7%, so this setting cannot be selected.
- If setting is 01b = 63 ns, minimum on duty ratio = 63 / 454 = 13.9%, so this setting can be selected.

Avoid using minimum blank-time setting (40 ns). This short blank time may cause incorrect boost current sensing during transient period. 63 ns or 88 ns are good enough for most of application conditions.

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (September 2017) to A Revision | Page |
|---|---|
| • Updated the BOOST_SEL_I and BOOST_SEL_P section | 5 |
| • Updated application report for clarity | 5 |

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