

TPS38-Q1 Wide V_{IN} 65 V Dual Channel Overvoltage or Undervoltage (OV or UV) Detector with Programmable Sense and Reset Function for Automotive

1 Features

- AEC-Q100 qualified with the following results:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$ ambient operating temperature T_A
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C7B
- Wide supply voltage range: 2.7 V to 65 V
- Functional Safety-Capable targeted
 - Documentation available to aid functional safety system design
- SENSE and RESET pins are 65 V graded
- Low quiescent current: 1 μA (typical)
- Flexible and wide voltage threshold options
 - Table 10-1
 - 2.7 V to 36 V (1.5% maximum accuracy)
 - 800 mV option (1% maximum accuracy)
- Built-in hysteresis (V_{HYS})
 - Percentage options: 2% to 13% (1% steps)
 - Fixed options: $V_{TH} < 8\text{ V} = 0.5\text{ V}, 1\text{ V}, 1.5\text{ V}, 2\text{ V}, 2.5\text{ V}$
- Programmable reset time delay
 - 10 nF = 12.8 ms, 10 μF = 12.8 s
- Programmable sense time delay
 - 10 nF = 1.28 ms, 10 μF = 1.28 s
- Manual Reset ($\overline{\text{MR}}$) feature
- Output topology:
 - Channel 1: Open-Drain or Push-Pull
 - Channel 2: Open-Drain

2 Applications

- Telematics control unit
- Emergency call system
- Audio amplifier
- Head unit and cluster
- Sensor fusion and cameras
- Body control module

3 Description

The TPS38-Q1 is a 65 V input voltage detector with 1 μA I_{DD} , 1% accuracy, and with a fast 10 μs detection time. This device can be connected directly to 12 V / 24 V automotive battery system for continuous monitoring of over (OV) or under (UV) voltage conditions; with its internal resistor divider, it offers the smallest total solution size. Wide hysteresis voltage options are available to ignore cold crank, start-stop and various car battery voltage transients. Built-in hysteresis on the SENSE pins prevents false reset signals when monitoring a supply voltage rail.

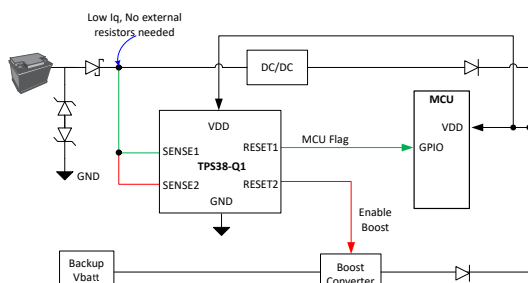
The separate VDD and SENSE pins allow redundancy sought by high-reliability automotive systems and SENSE can monitor higher and lower voltages than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pins. CTSx and CTRx pins allow delay adjustability on the rising and falling edges of the RESET signals. Also, CTSx functions as a debouncer by ignoring voltage glitches on the monitored voltage rails; CTRx operates as a manual reset ($\overline{\text{MR}}$) that can be used to force a system reset.

The TPS38-Q1 is available in WSON or SOT-23 package. The WSON package has wettable flanks allowing the facilitation for Automatic Optical Inspection (AOI) and low resolution X-ray inspection. The central pad is non-conductive to increase the creepage between VDD and GND per guidelines in IEC60664.

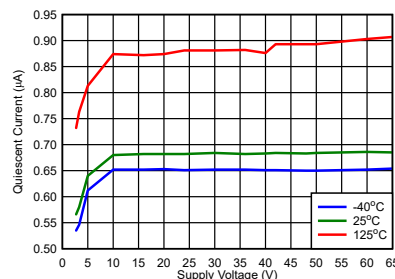
Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|-----------------|
| TPS38-Q1 | WSON (10) (DSK) | 2.5 mm × 2.5 mm |
| TPS38-Q1 | SOT-23 (14) (DYY) | 4.1 mm × 1.9 mm |

- (1) For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Application Circuit



Typical I_{DD} vs V_{DD}



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| | |
|---|-------------|
| Changes from Revision D (July 2023) to Revision E (August 2023) | Page |
| • Added Hysteresis accuracy diagram..... | 10 |
| • Updated the typical characteristic curves..... | 13 |
| Changes from Revision C (December 2021) to Revision D (July 2023) | Page |
| • Deleted Product Preview for the DYY package through data sheet..... | 1 |
| Changes from Revision B (September 2021) to Revision C (December 2021) | Page |
| • Advance Information to Production Data release..... | 1 |

5 Device Comparison

Contact TI sales representatives or consult [TI's E2E forum](#) for details and availability; minimum order quantities may apply.

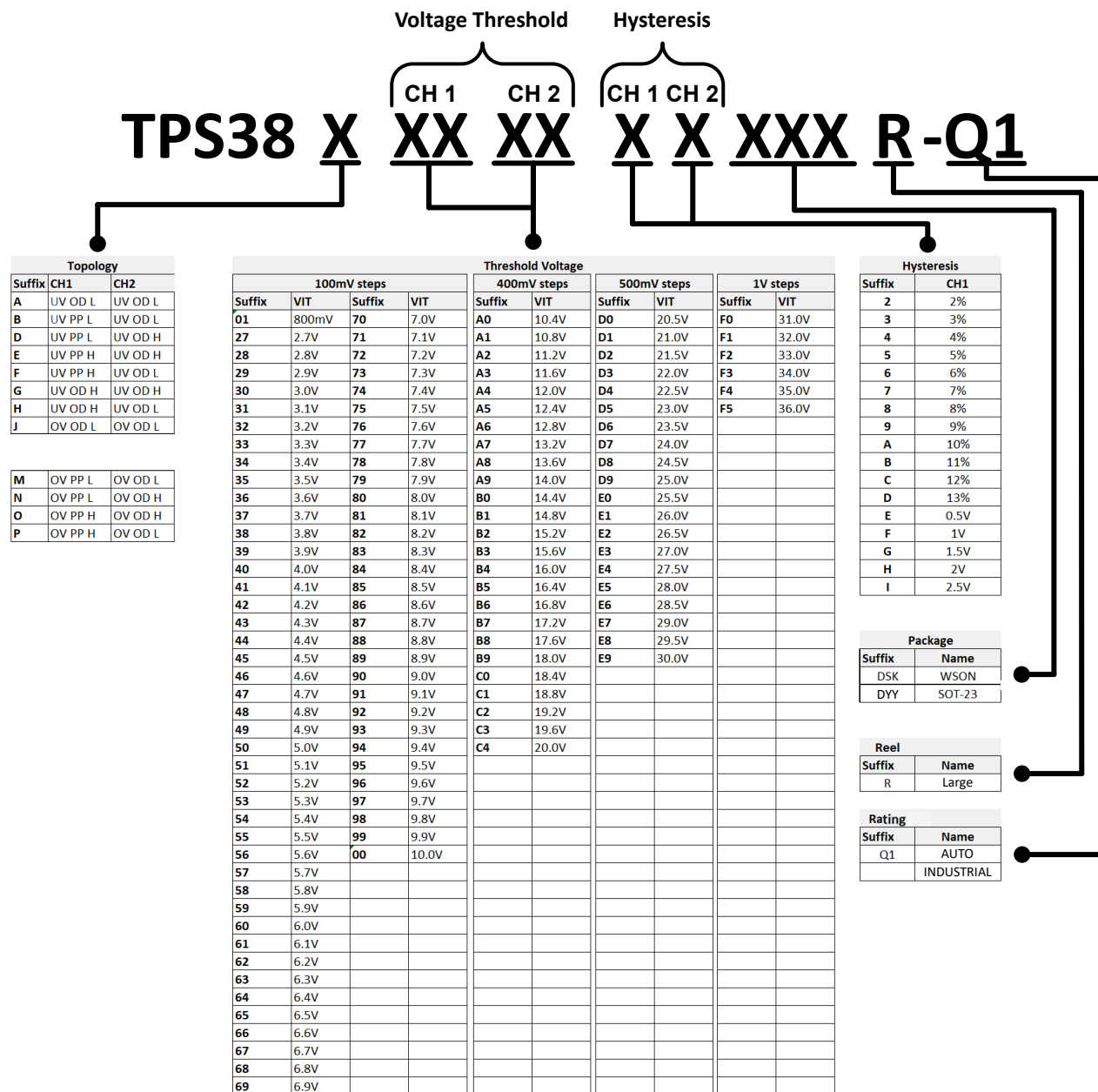
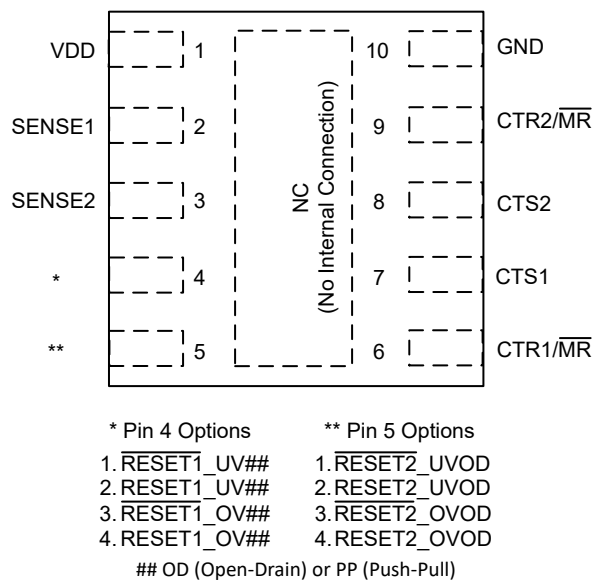


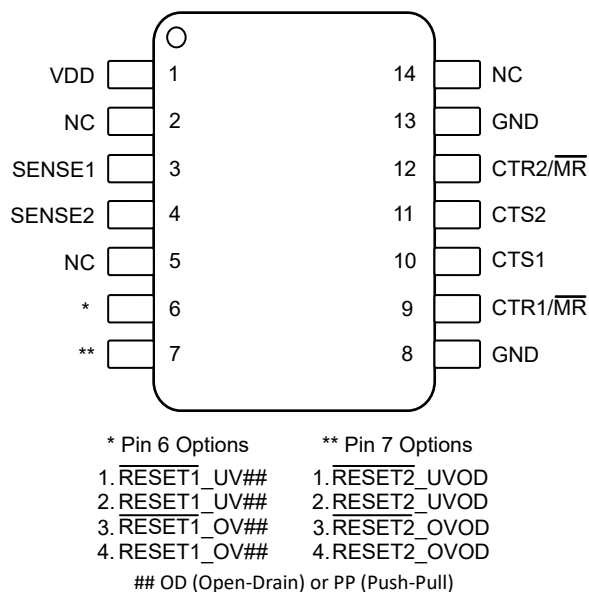
Figure 5-1. Device Nomenclature

1. Sense logic: OV = overvoltage; UV = undervoltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.7 V to 8 V threshold options

6 Pin Configuration and Functions



**Figure 6-1. DSK Package,
10-Pin WSON,
TPS38-Q1 (Top View)**



**Figure 6-2. DYY Package,
14-Pin SOT-23,
TPS38-Q1 (Top View)**

Table 6-1. Pin Functions

| PIN NAME | WSN (DSK) | SOT23 (DYY) | I/O | DESCRIPTION |
|--|--------------|----------------|-----|--|
| | PIN NUM. | PIN NUM. | | |
| VDD | 1 | 1 | I | Input Supply Voltage: Bypass with a 0.1 μ F capacitor to GND. |
| SENSE1 | 2 | 3 | I | This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. Depending on the SENSE1 sensing configuration, when the voltage on SENSE1 pin detects an undervoltage (UV) or an overvoltage (OV) fault, $\overline{\text{RESET1}}$ /RESET1 asserts after the sense time delay, set by CTS1. When the voltage on the SENSE1 pin transitions back to an unfaulty UV or OV state, $\overline{\text{RESET1}}$ /RESET1 deasserts after the reset time delay, set by CTR1. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance. |
| SENSE2 | 3 | 4 | I | This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. Depending on the SENSE2 sensing configuration, when the voltage on SENSE2 pin detects an undervoltage (UV) or an overvoltage (OV) fault, $\overline{\text{RESET2}}$ /RESET2 asserts after the sense time delay, set by CTS2. When the voltage on the SENSE2 pin transitions back to an unfaulty UV or OV state, $\overline{\text{RESET2}}$ /RESET2 deasserts after the reset time delay, set by CTR2. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance. |
| $\overline{\text{RESET1}}$ / RESET1 | 4 | 6 | O | Output Reset Signal For Channel 1: See Section 5 for output topology options. $\overline{\text{RESET1}}$ /RESET1 asserts when SENSE1 detects an undervoltage or overvoltage fault condition. $\overline{\text{RESET1}}$ /RESET1 remains asserted for the reset time delay period after SENSE1 transitions out of an UV or OV fault condition. For active low open-drain reset output, an external pullup resistor is required. Do not place external pullup resistors on push-pull outputs. Reset output signal for: SENSE1 Sensing Topology: Undervoltage (UV) or Overvoltage (OV) Output topology: Open Drain or Push Pull, Active Low or Active High |
| $\overline{\text{RESET2}}$ / RESET2 | 5 | 7 | O | Output Reset Signal For Channel 2: See Section 5 for output topology options. $\overline{\text{RESET2}}$ /RESET2 asserts when SENSE2 detects an undervoltage or overvoltage fault condition. $\overline{\text{RESET2}}$ /RESET2 remains asserted for the reset time delay period after SENSE2 transitions out of an UV or OV fault condition. For active low open-drain reset output, an external pullup resistor is required. Reset output signal for: SENSE2 Sensing Topology: Undervoltage (UV) or Overvoltage (OV) Output topology: Open Drain, Active Low or Active High |
| CTR1/ $\overline{\text{MR}}$ | 6 | 9 | - | Channel 1 RESET Time Delay: User-programmable reset time delay for $\overline{\text{RESET1}}$ /RESET1. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. Manual Reset: If this pin is driven low, the $\overline{\text{RESET1}}$ /RESET1 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high. |
| CTR2/ $\overline{\text{MR}}$ | 9 | 12 | - | Channel 2 RESET Time Delay: User-programmable reset time delay for $\overline{\text{RESET2}}$ /RESET2. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. Manual Reset: If this pin is driven low, the $\overline{\text{RESET2}}$ /RESET2 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high. |
| GND | 10 | 8, 13 | - | Ground. All GND pins must be electrically connected to the board ground. |
| NC | PAD | 2, 5, 14 | - | The PAD for the DSK package is not internally connected, the PAD can be connected to GND or be left floating. For the DYY package, NC stands for "No Connect". The pins are to be left floating. |
| CTS1 | 7 | 10 | O | Channel 1 SENSE Time Delay: Capacitor programmable sense delay: CTS1 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET1}}$ /RESET1 delay time to assert. |
| CTS2 | 8 | 11 | O | Channel 2 SENSE Time Delay: Capacitor programmable sense delay: CTS2 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET2}}$ /RESET2 delay time to assert. |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted ⁽¹⁾

| | | MIN | MAX | UNIT |
|----------------------------|---|------|-----|------|
| Voltage | V _{DD} , V _{SENSE1} , V _{SENSE2} , V _{RESET1} , V _{RESET2} , V _{RESET1} , V _{RESET2} | −0.3 | 70 | V |
| Voltage | V _{CTS1} , V _{CTS2} , V _{CTR1} , V _{CTR2} | −0.3 | 6 | V |
| Current | I _{RESET1} , I _{RESET2} , I _{RESET1} , I _{RESET2} | | 10 | mA |
| Temperature ⁽²⁾ | Operating junction temperature, T _J | −40 | 150 | °C |
| Temperature ⁽²⁾ | Operating Ambient temperature, T _A | −40 | 150 | °C |
| Temperature ⁽²⁾ | Storage, T _{stg} | −65 | 150 | °C |

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | ±750 | |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------|---|-----|-----|-----|------|
| Voltage | V _{DD} | 2.7 | | 65 | V |
| Voltage | V _{SENSE1} , V _{SENSE2} , V _{RESET1} , V _{RESET2} , V _{RESET1} , V _{RESET2} | 0 | | 65 | V |
| Voltage | V _{CTS1} , V _{CTS2} , V _{CTR1} , V _{CTR2} | 0 | | 5.5 | V |
| Current | I _{RESET1} , I _{RESET2} , I _{RESET1} , I _{RESET2} | 0 | | ±5 | mA |
| T _J | Junction temperature (free air temperature) | −40 | | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS38-Q1 | | UNIT |
|-------------------------------|--|----------|--------|------|
| | | DSK | DYY | |
| | | 10-PIN | 14-PIN | |
| R _{θJA} | Junction-to-ambient thermal resistance | 87.4 | 131.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 76.3 | 61.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 54.2 | 56.6 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 4.8 | 3.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 54.2 | 56.5 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 34.8 | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|---|--|--------------------|-------|-------|------|
| VDD | | | | | | |
| V _{DD} | Supply Voltage | | 2.7 | | 65 | V |
| UVLO ⁽¹⁾ | Undervoltage Lockout | V _{DD} Falling below V _{DD (MIN)} | | | 2.7 | V |
| V _{POR} | Power on Reset Voltage ⁽²⁾ RESET, Active Low (Open-Drain, Push-Pull) | V _{OL(MAX)} = 300 mV I _{OUT (Sink)} = 15 μA | | | 1.4 | V |
| V _{POR} | Power on Reset Voltage ⁽²⁾ RESET, Active High (Push-Pull) | V _{OH(MIN)} = 0.8 x V _{DD} I _{OUT (Source)} = 15 μA | | | 1.4 | V |
| I _{DD} | Supply current into VDD pin | V _{IT} = 800 mV V _{DD (MIN)} ≤ V _{DD} ≤ V _{DD (MAX)} | | 1 | 2.6 | μA |
| | | V _{IT} = 2.7 V to 36 V V _{DD (MIN)} ≤ V _{DD} ≤ V _{DD (MAX)} | | 1 | 2 | μA |
| SENSE (Input) | | | | | | |
| I _{SENSE} | Input current (SENSE1, SENSE2) | V _{IT} = 800 mV | | | 100 | nA |
| I _{SENSE} | Input current (SENSE1, SENSE2) | V _{IT} < 10 V | | | 0.8 | μA |
| I _{SENSE} | Input current (SENSE1, SENSE2) | 10 V < V _{IT} < 26 V | | | 1.2 | μA |
| I _{SENSE} | Input current (SENSE1, SENSE2) | V _{IT} > 26 V | | | 2 | μA |
| V _{ITN} | Input Threshold Negative (Undervoltage) | V _{IT} = 2.7 V to 36 V | -1.5 | | 1.5 | % |
| | | V _{IT} = 800 mV ⁽³⁾ | 0.792 | 0.800 | 0.808 | V |
| V _{ITP} | Input Threshold Positive (Overvoltage) | V _{IT} = 2.7 V to 36 V | -1.5 | | 1.5 | % |
| | | V _{IT} = 800 mV ⁽³⁾ | 0.792 | 0.800 | 0.808 | V |
| V _{HYS} | Hysteresis Accuracy ⁽⁴⁾ | V _{IT} = 0.8 V and 2.7 V to 36 V V _{HYS} Range = 2% to 13% (1% step) | -1.5 | | 1.5 | % |
| | | V _{IT} = 2.7 V to 8 V V _{HYS} = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V (V _{ITP} - V _{HYS}) ≥ 2.4 V, OV Only | -1.5 | | 1.5 | % |
| RESET (Output) | | | | | | |
| I _{lkg(OD)} | Open-Drain leakage (RESET1, RESET2) | V _{RESET} = 5.5 V V _{ITN} < V _{SENSE} < V _{ITP} | | | 300 | nA |
| | | V _{RESET} = 65 V V _{ITN} < V _{SENSE} < V _{ITP} | | | 300 | nA |
| V _{OL} ⁽⁵⁾ | Low level output voltage | 2.7 V ≤ V _{DD} ≤ 65 V I _{RESET} = 5 mA | | | 300 | mV |
| V _{OH_DO} | High level output voltage dropout (V _{DD} - V _{OH} = V _{OH_DO}) (Push-Pull only) | 2.7 V ≤ V _{DD} ≤ 65 V I _{RESET} = 500 uA | | | 100 | mV |
| V _{OH} ⁽⁵⁾ | High level output voltage (Push-Pull only) | 2.7 V ≤ V _{DD} ≤ 65 V I _{RESET} = 5 mA | 0.8V _{DD} | | | V |

7.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--------------------------|------|------|------|-------|
| Capacitor Timing (CTS, CTR) | | | | | | |
| R_{CTR} | Internal resistance ($CTR1 / \overline{MR}$, $CTR2 / \overline{MR}$) | | 877 | 1000 | 1147 | Kohms |
| R_{CTS} | Internal resistance ($CTS1$, $CTS2$) | | 88 | 100 | 122 | Kohms |
| Manual Reset (\overline{MR}) | | | | | | |
| $V_{\overline{MR_IH}}$ | $CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic high input | $V_{DD} = 2.7 \text{ V}$ | 2200 | | | mV |
| $V_{\overline{MR_IH}}$ | $CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic high input | $V_{DD} = 65 \text{ V}$ | 2500 | | | mV |
| $V_{\overline{MR_IL}}$ | $CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic low input | $V_{DD} = 2.7 \text{ V}$ | | | 1300 | mV |
| $V_{\overline{MR_IL}}$ | $CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic low input | $V_{DD} = 65 \text{ V}$ | | | 1300 | mV |

- (1) When V_{DD} voltage falls below UVLO, reset is asserted for Output 1 and Output 2. V_{DD} slew rate $\leq 100 \text{ mV} / \mu\text{s}$
- (2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR} , the output cannot be determined. $V_{DD} \text{ dv/dt} \leq 100 \text{ mV}/\mu\text{s}$
- (3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
- (4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
- (5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

7.6 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$ ⁽¹⁾, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5\text{V}$, and $C_{LOAD} = 10 \text{ pF}$. VDD and SENSE slew rate = $1\text{V} / \mu\text{s}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to either V_{ITN} or V_{ITP}).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|--|---|-----|-----|---------------------|
| Common timing parameters | | | | | |
| t_{CTR} | Reset release time delay ($CTR1/\overline{MR}$, $CTR2/\overline{MR}$) ⁽²⁾ | $V_{IT} = 2.7 \text{ V to } 36 \text{ V}$ $C_{CTR1} = C_{CTR2} = \text{Open}$ 20% Overdrive from Hysteresis | | 100 | μs |
| | | $V_{IT} = 800 \text{ mV}$ $C_{CTR1} = C_{CTR2} = \text{Open}$ 20% Overdrive from Hysteresis | | 40 | μs |
| t_{CTS} | Sense detect time delay ($CTS1$, $CTS2$) ⁽³⁾ | $V_{IT} = 2.7 \text{ V to } 36 \text{ V}$ $C_{CTS1} = C_{CTS2} = \text{Open}$ 20% Overdrive from V_{IT} | | 34 | 90 μs |
| | | $V_{IT} = 800 \text{ mV}$ $C_{CTS1} = C_{CTS2} = \text{Open}$ 20% Overdrive from V_{IT} | | 8 | 17 μs |
| t_{SD} | Startup Delay ⁽⁴⁾ | $C_{CTR1}/\overline{MR} = C_{CTR2}/\overline{MR} = \text{Open}$ | | 2 | ms |

- (1) C_{CTR1} = Reset delay channel 1, C_{CTR2} = Reset delay channel 2,
 C_{CTS1} = Sense delay channel 1, C_{CTS2} = Sense delay channel 2
- (2) **CTR Reset detect time delay:**
Overvoltage active-LOW output is measure from $V_{ITP} - HYS$ to V_{OH}
Undervoltage active-LOW output is measure from $V_{ITN} + HYS$ to V_{OH}
Overvoltage active-HIGH output is measure from $V_{ITP} - HYS$ to V_{OL}
Undervoltage active-HIGH output is measure from $V_{ITN} + HYS$ to V_{OL}
- (3) **CTS Sense detect time delay:**
Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
Active-high output is measured from V_{IT} to V_{OH}
 V_{IT} refers to either V_{ITN} or V_{ITP}
- (4) During the power-on sequence, VDD must be at or above $V_{DD(MIN)}$ for at least t_{SD} before the output is in the correct state based on V_{SENSE} .
 t_{SD} time includes the propagation delay ($C_{CTR1} = C_{CTR2} = \text{Open}$). Capacitor in C_{CTR1} or C_{CTR2} will add time to t_{SD} .

7.7 Timing Diagrams

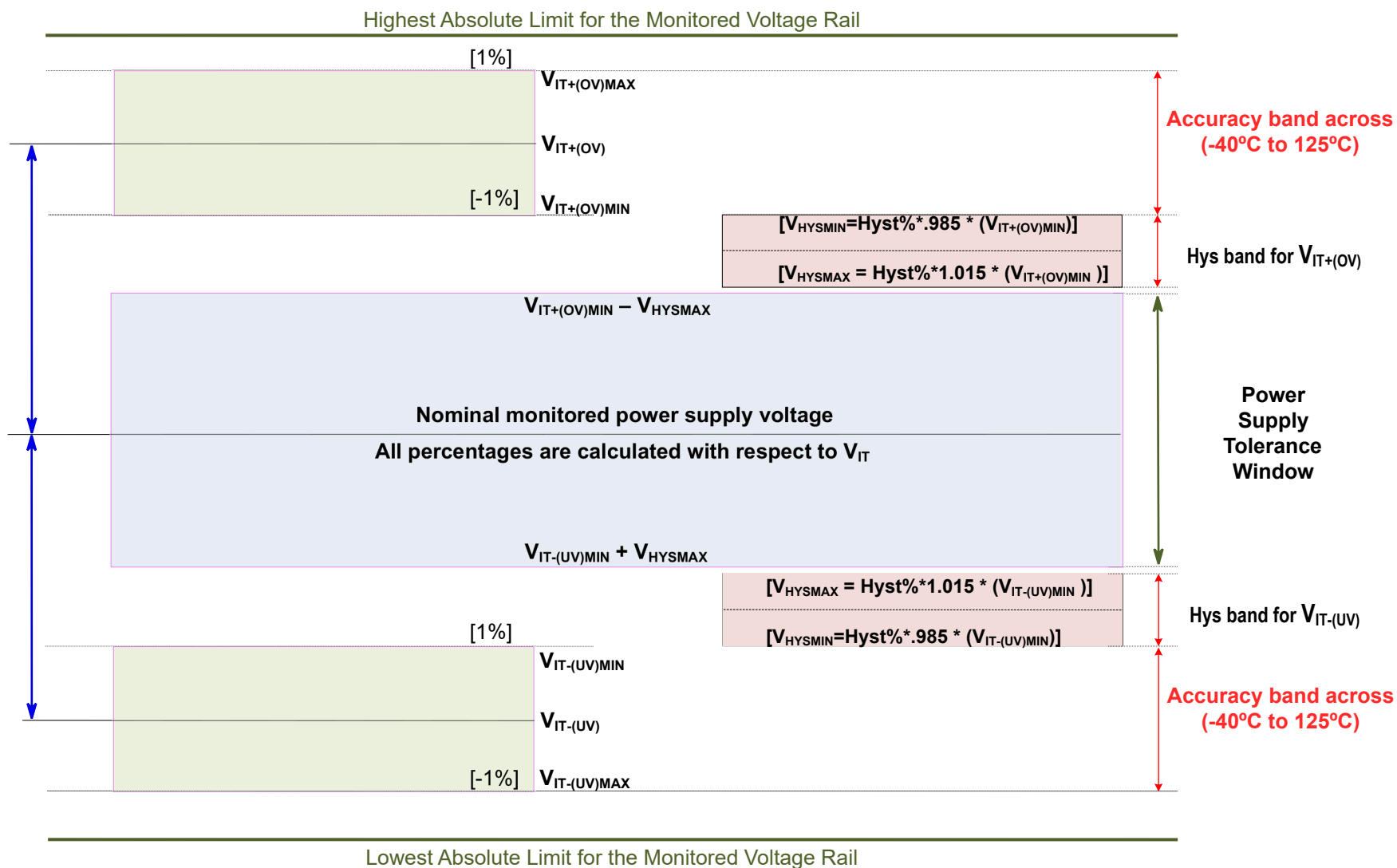
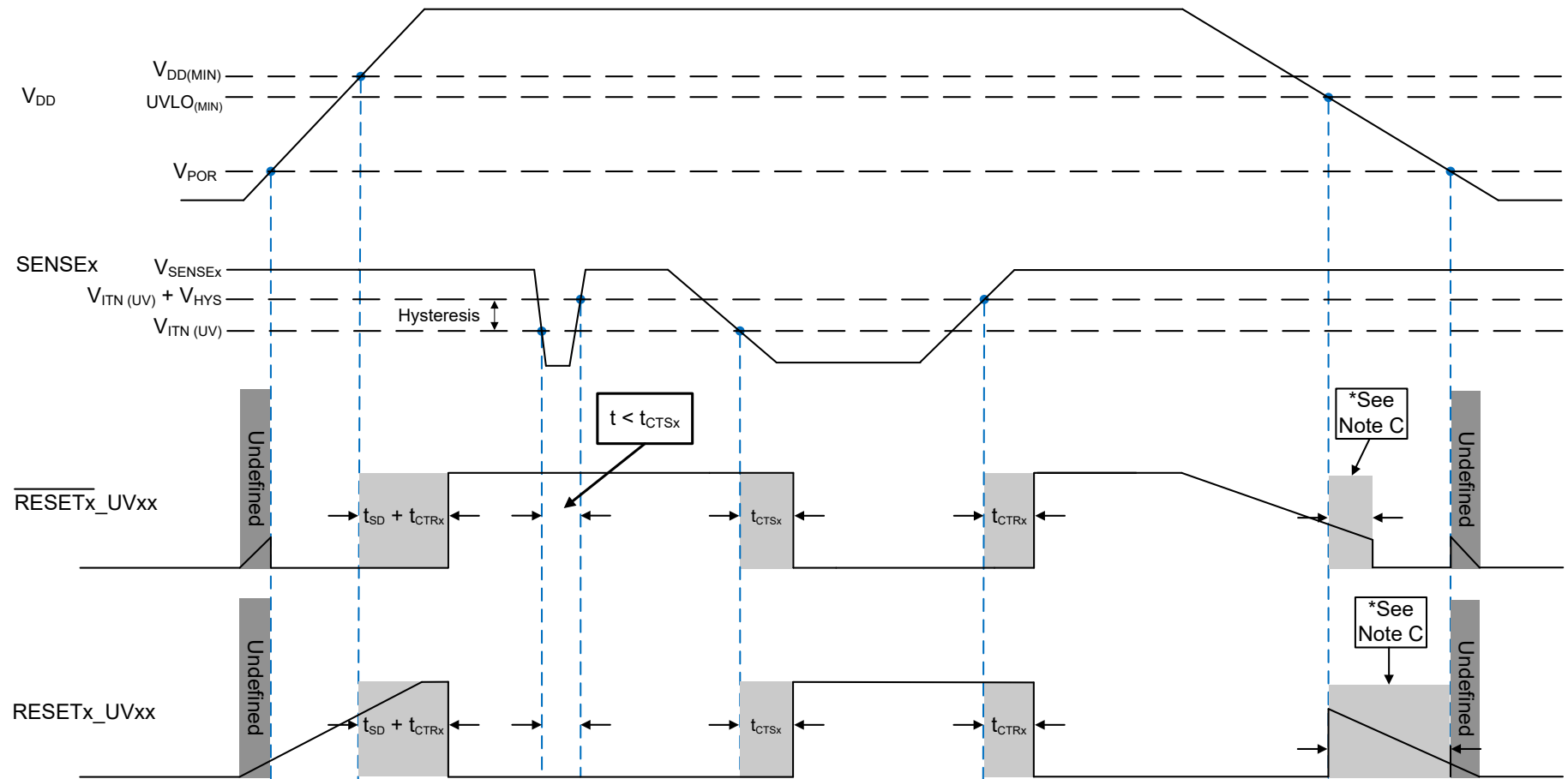
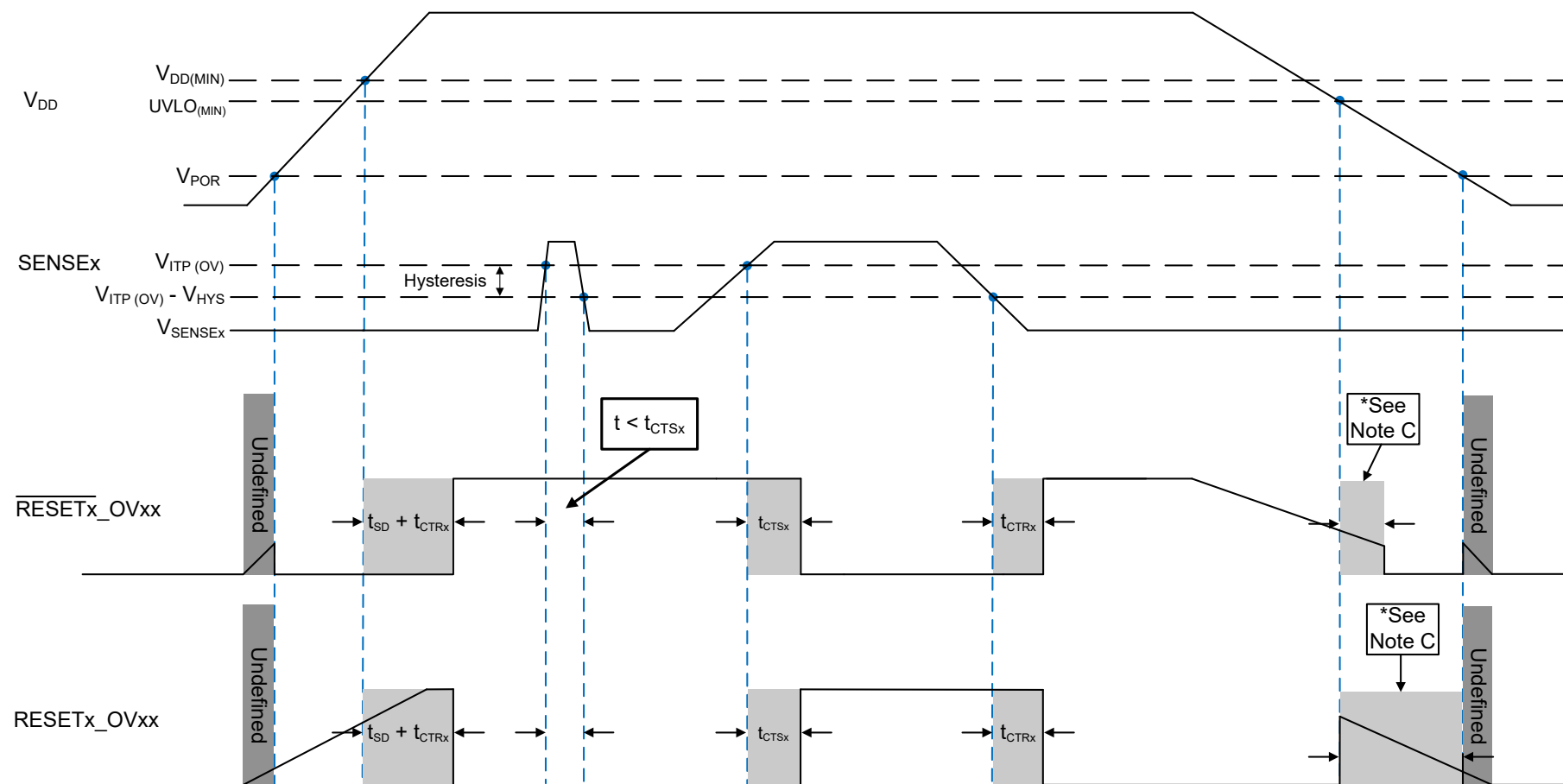


Figure 7-1. Voltage Threshold and Hysteresis Accuracy



- For open-drain output option, the timing diagram assumes the $\overline{\text{RESETx_UVOD}}$ / RESETx_UVOD pin is connected via an external pull-up resistor to VDD.
- Be advised that Figure 7-2 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTRx}) time.
- $\overline{\text{RESETx_UVxx}}$ / RESETx_UVxx is asserted when VDD goes below the UVLO_(MIN) threshold after the time delay, t_{CTRx}, is reached.

Figure 7-2. SENSEx Undervoltage (UV) Timing Diagram



- A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESETx_OVOD}}$ / RESETx_OVOD pin is connected via an external pull-up resistor to VDD.
- B. Be advised that Figure 7-3 shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTR_x}) time.
- C. $\overline{\text{RESETx_OVxx}}$ / RESETx_OVxx is asserted when VDD goes below the UVLO_(MIN) threshold after the time delay, t_{CTR_x} , is reached.

Figure 7-3. SENSEx Overvoltage (OV) Timing Diagram

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS38-Q1 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

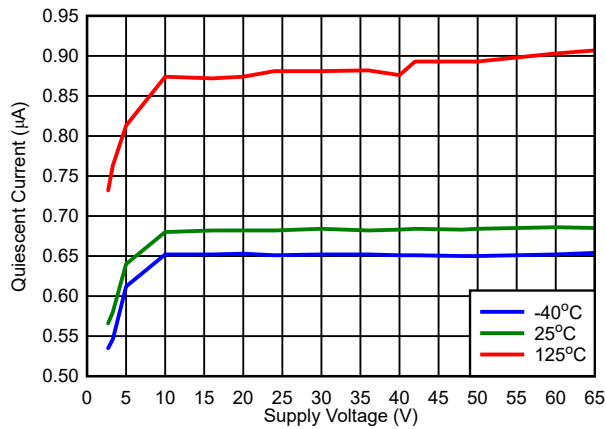


Figure 7-4. V_{DD} vs I_{DD} ($\overline{\text{RESET}}$ = High, $V_{IT} = 2.7\text{ V}$)

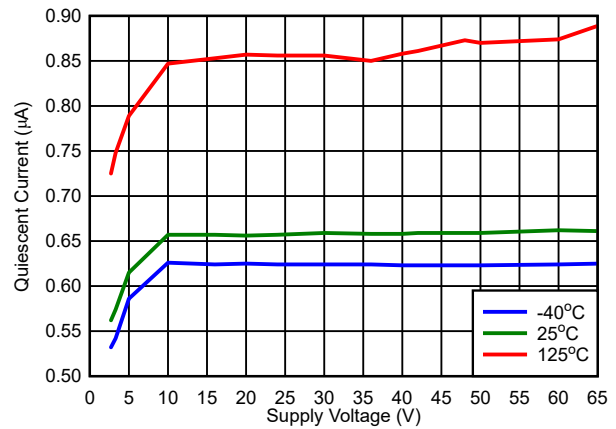


Figure 7-5. V_{DD} vs I_{DD} ($\overline{\text{RESET}}$ = Low, $V_{IT} = 2.7\text{ V}$)

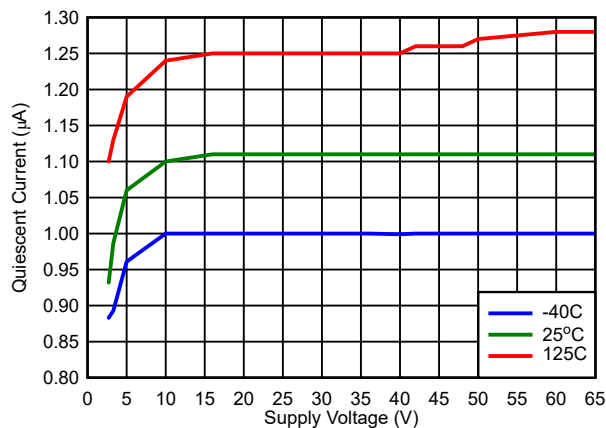


Figure 7-6. V_{DD} vs I_{DD} ($\overline{\text{RESET}}$ = High, $V_{IT} = 0.8\text{ V}$)

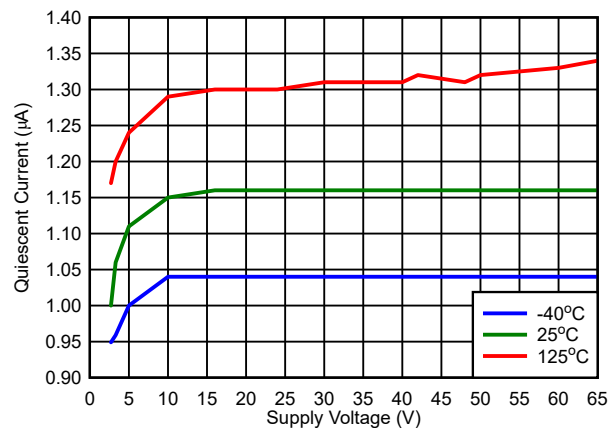


Figure 7-7. V_{DD} vs I_{DD} ($\overline{\text{RESET}}$ = Low, $V_{IT} = 0.8\text{ V}$)

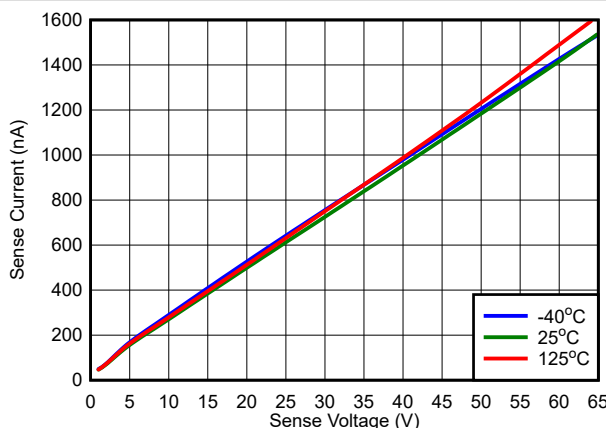


Figure 7-8. V_{SENSE} vs I_{SENSE}

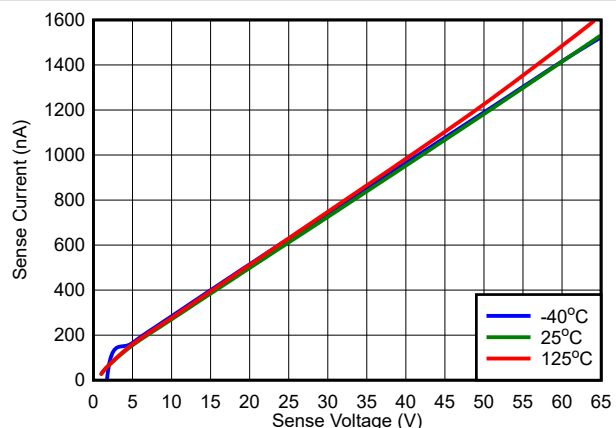


Figure 7-9. V_{SENSE} vs I_{SENSE}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS38-Q1 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

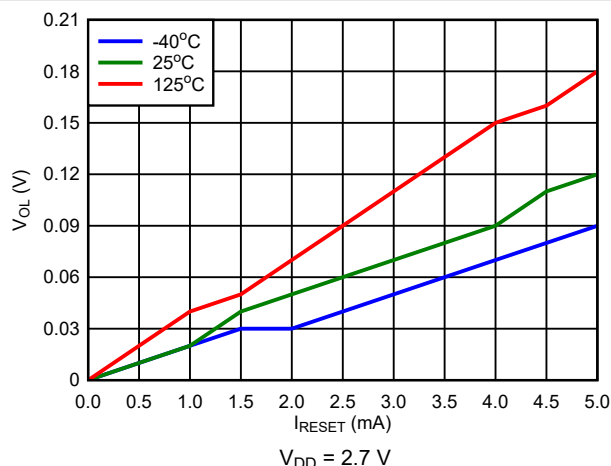


Figure 7-10. Open-Drain Active Low V_{OL} vs I_{RESET}

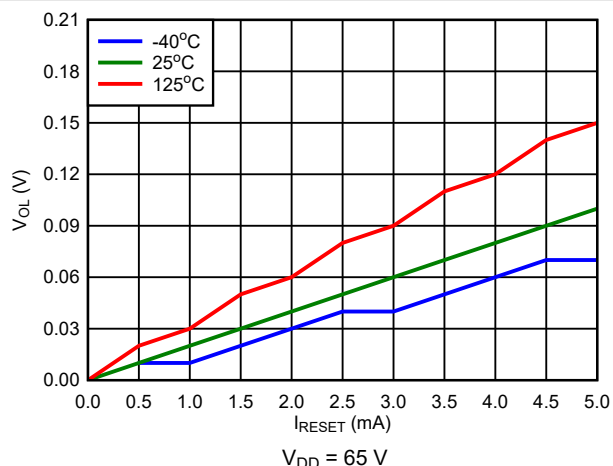


Figure 7-11. Open-Drain Active Low V_{OL} vs I_{RESET}

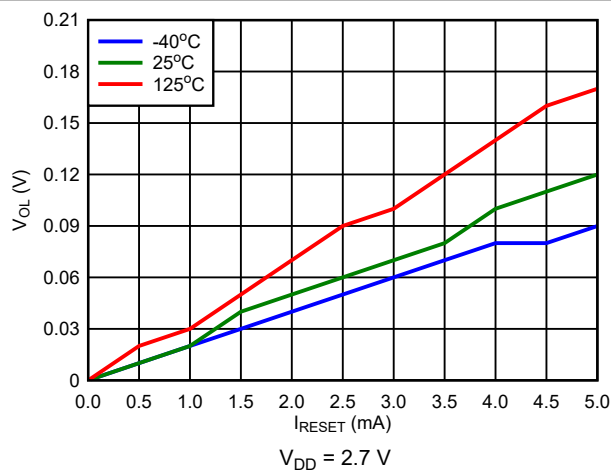


Figure 7-12. Open-Drain Active High V_{OL} vs I_{RESET}

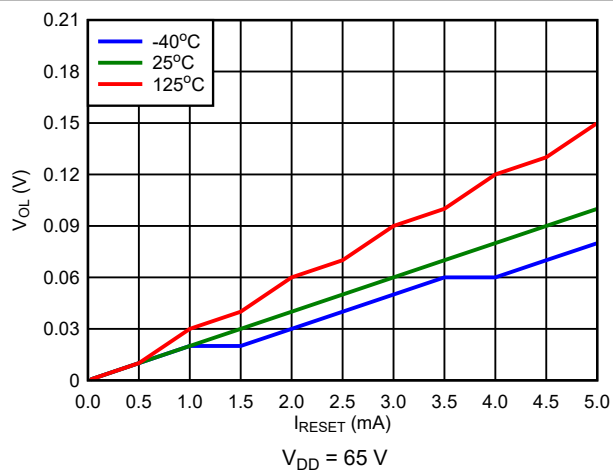


Figure 7-13. Open-Drain Active High V_{OL} vs I_{RESET}

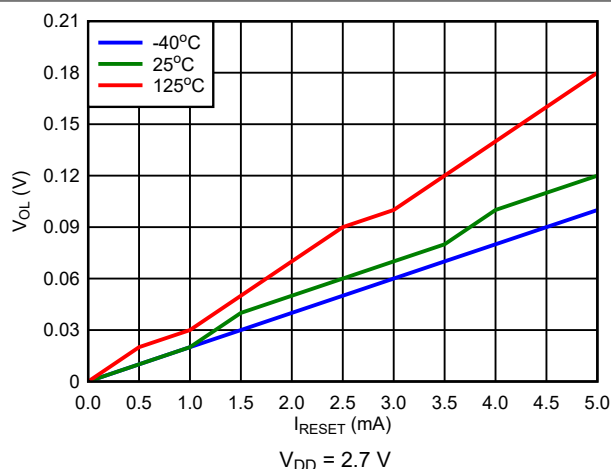


Figure 7-14. Push-Pull Active High V_{OL} vs I_{RESET}

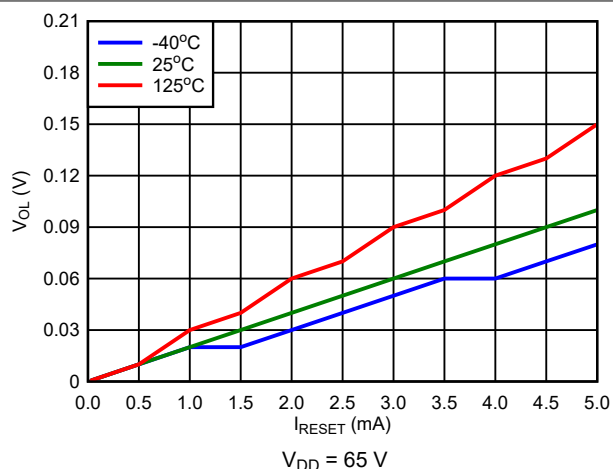


Figure 7-15. Push-Pull Active High V_{OL} vs I_{RESET}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS38-Q1 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

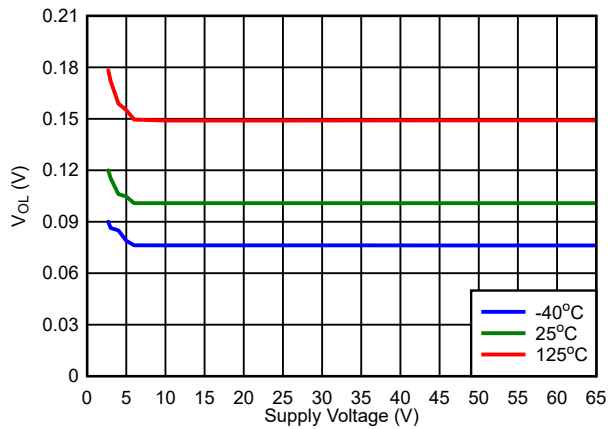


Figure 7-16. Open-Drain Active Low V_{OL} vs V_{DD}

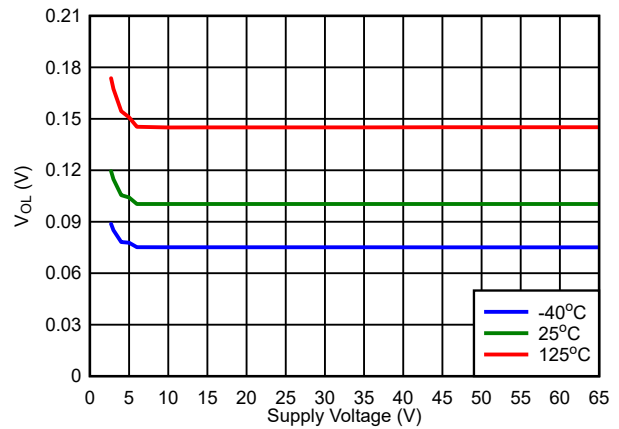


Figure 7-17. Open-Drain Active High V_{OL} vs V_{DD}

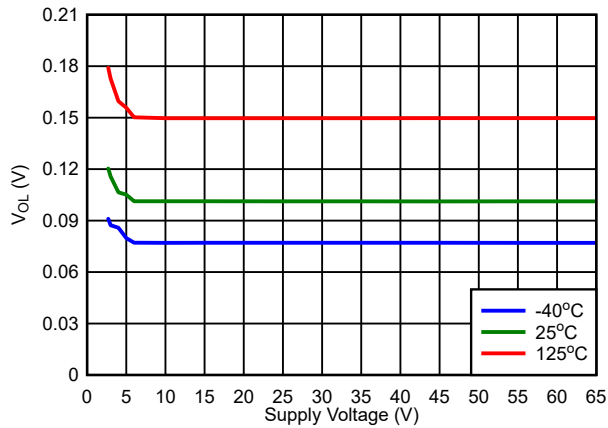


Figure 7-18. Push-Pull Active Low V_{OL} vs V_{DD}

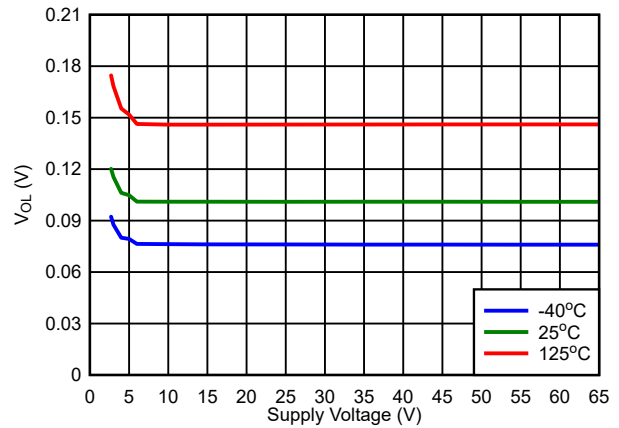


Figure 7-19. Push-Pull Active High V_{OL} vs V_{DD}

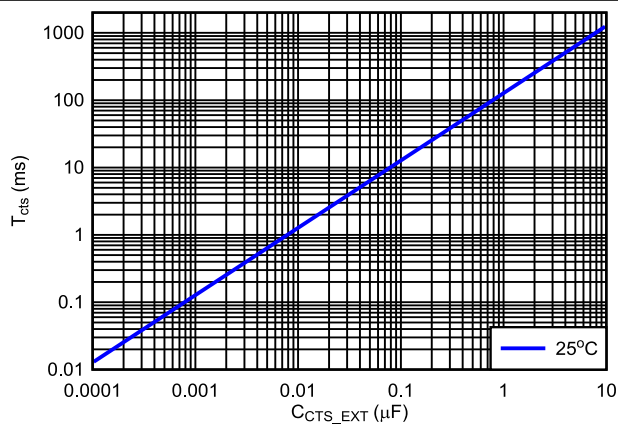


Figure 7-20. T_{CTS} vs C_{CTS}

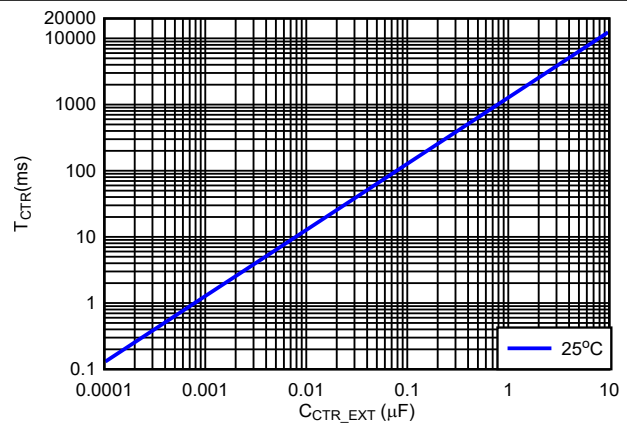


Figure 7-21. T_{CTR} vs C_{CTR}

8 Detailed Description

8.1 Overview

The TPS38-Q1 is a family of high voltage and low quiescent current reset IC with fixed threshold voltage. Voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support external resistor if required by application, the lowest threshold 800 mV (bypass internal resistor ladder) is recommended for external resistors use case to take advantage of faster detection time and lower I_{SENSE} current.

VDD, SENSE and RESET pins can support 65 V continuous operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage. One thing of note, the TPS38-Q1 does not have clamps within the device so external circuits or devices must be added to limit the voltages to the absolute max limit.

Additional features include programmable sense time delay (CTS1, CTS2) and reset delay time and manual reset (CTR1 / \overline{MR} , CTR2 / \overline{MR}).

8.2 Functional Block Diagram

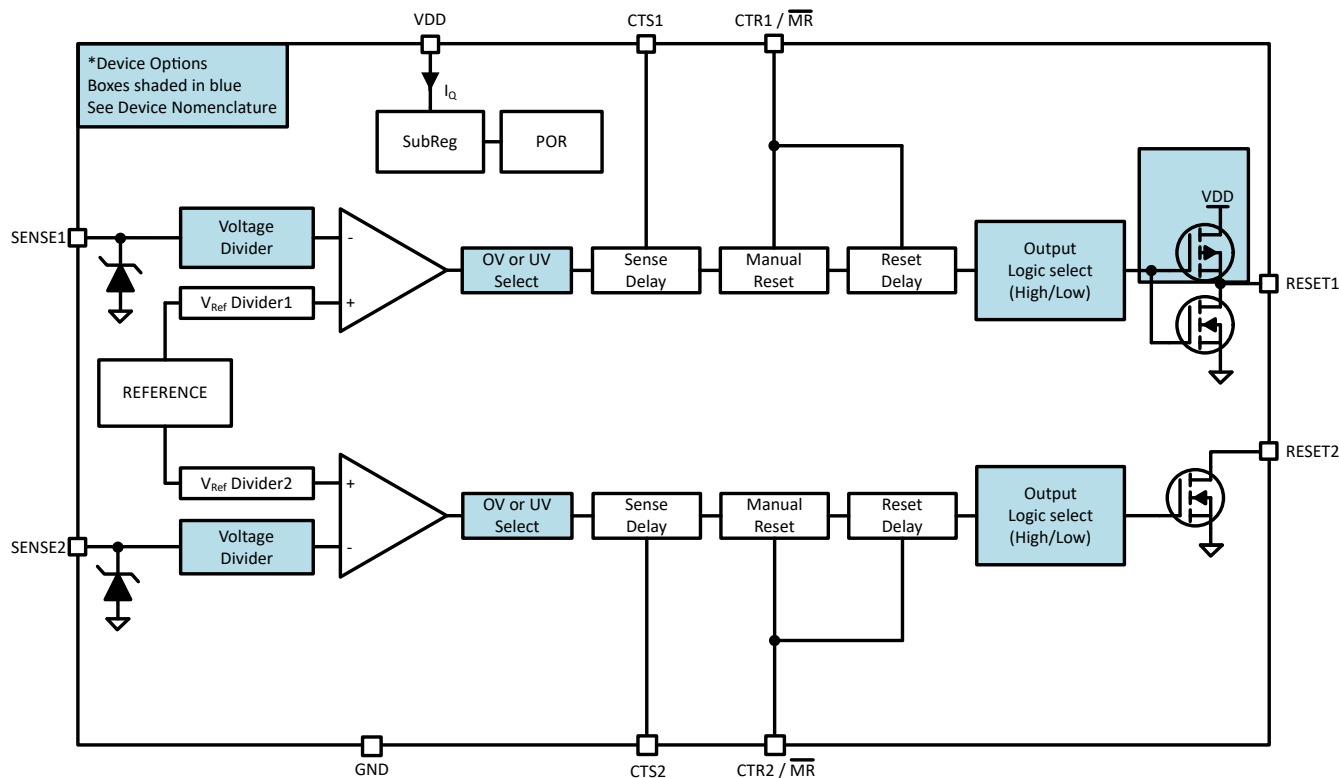


Figure 8-1. Functional Block Diagram

Refer to [Section 5](#) for complete list of topologies and output logic combinations.

8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 μ F capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET} , meaning that VDD can be higher or lower than the other pins.

8.3.1.1 Undervoltage Lockout ($V_{POR} < V_{DD} < UVLO$)

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the output pins will be in reset, regardless of the voltage at SENSE pins.

8.3.1.2 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

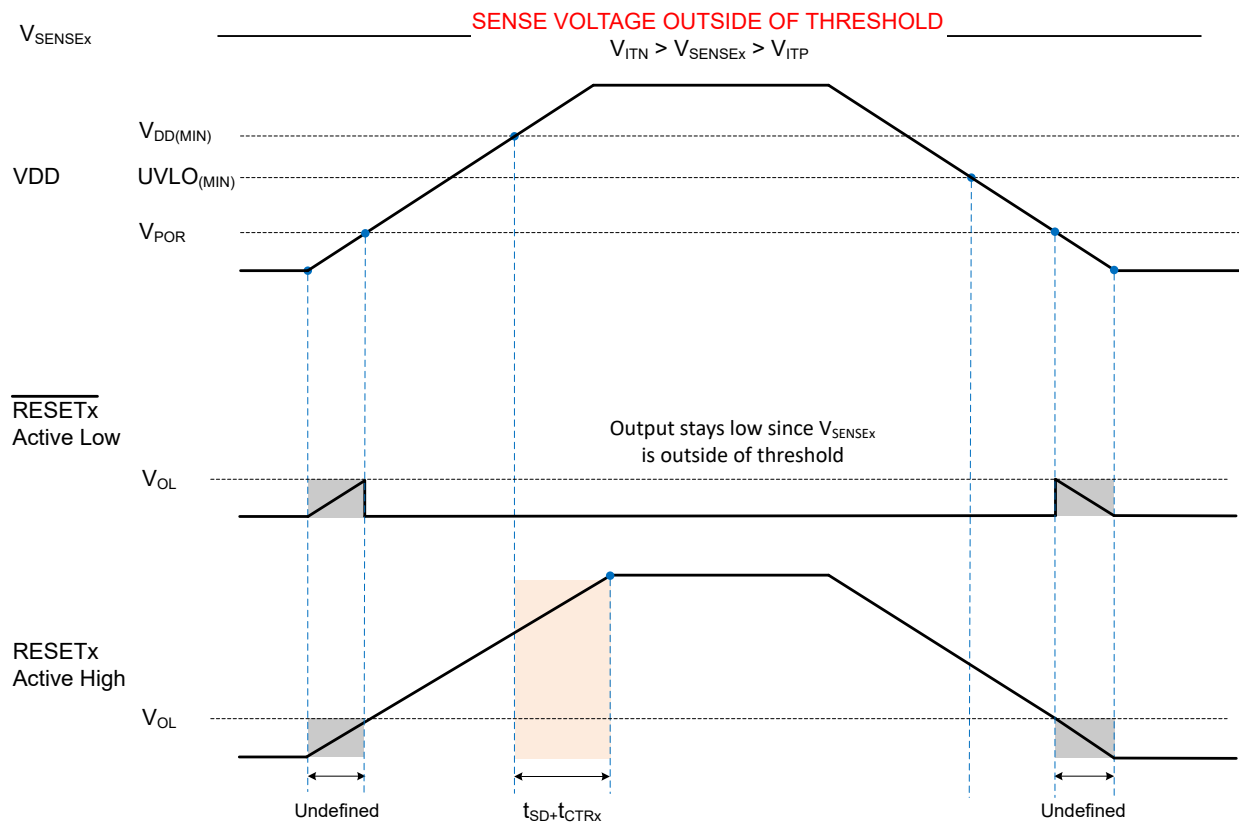


Figure 8-2. Power Cycle (SENSE Outside of Nominal Voltage)

Figure 8-2 assumes an external pull-up resistor is connected to the reset pin via VDD.

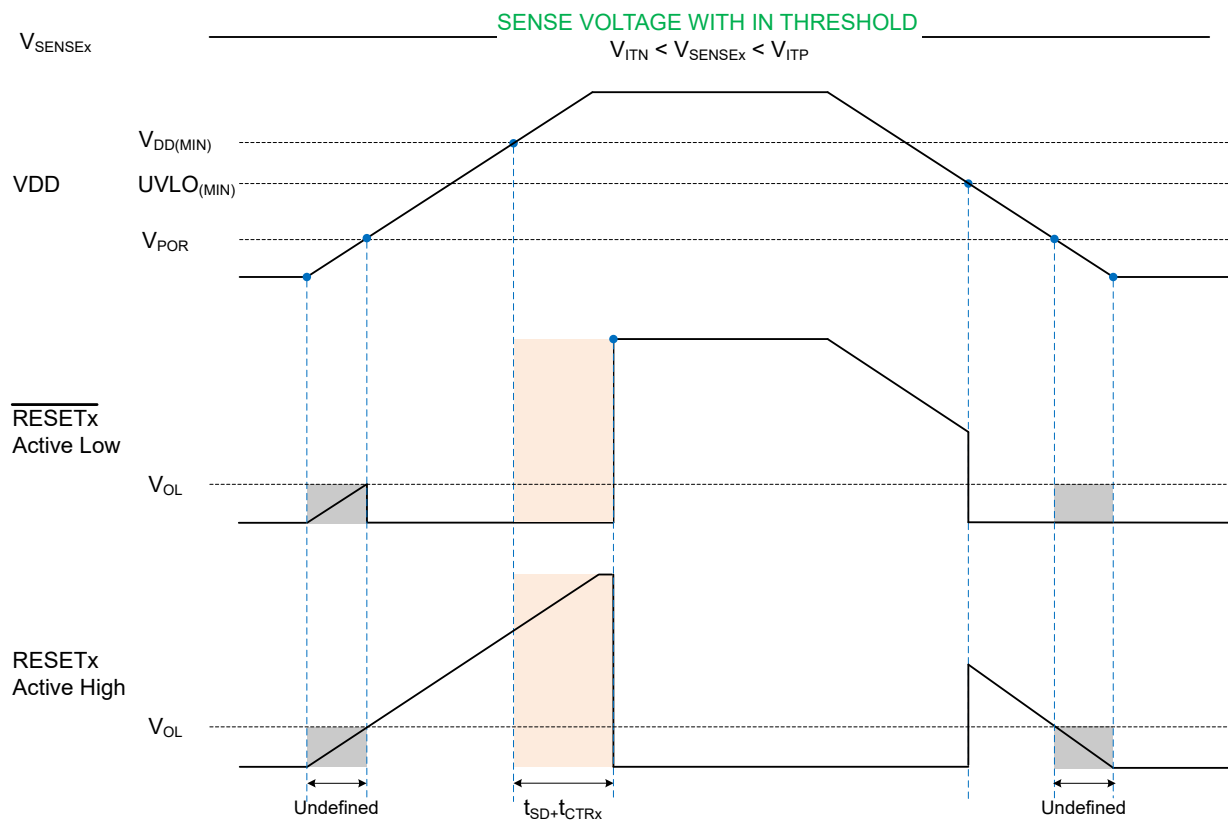


Figure 8-3. Power Cycle (SENSE Within Nominal Voltage)

Figure 8-3 assumes an external pull-up resistor is connected to the reset pin via VDD.

8.3.2 SENSE

The TPS38-Q1 high voltage family integrates two voltage comparators, a precision reference voltage and trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Channels are independent of each other, meaning that SENSE1 and SENSE2 and respective outputs can be connected to different voltage rails.

Although not required in most cases, for noisy applications good analog design practice is to place a 1 nF to 10 nF bypass capacitor at the SENSEx inputs in order to reduce sensitivity to transient voltages on the monitored signal. SENSE1 and SENSE2 pins can be connected directly to VDD pin.

8.3.2.1 SENSE Hysteresis

The TPS38-Q1 has built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

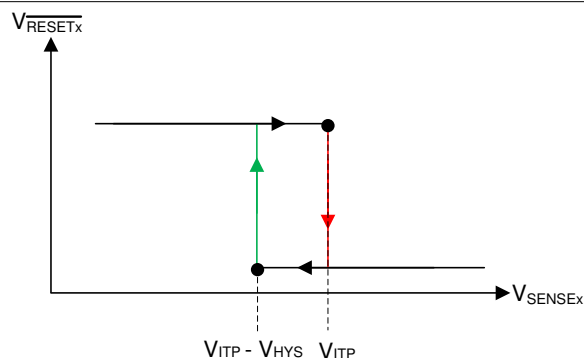


Figure 8-4. Hysteresis (Overvoltage Active-Low)

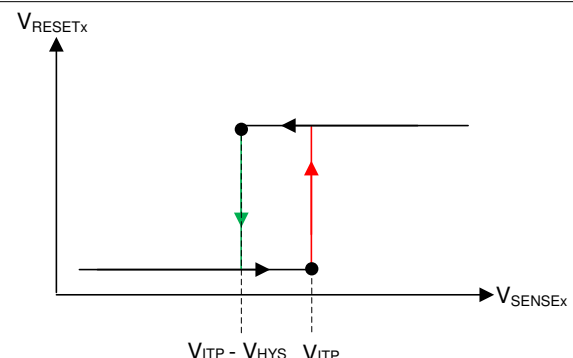


Figure 8-5. Hysteresis (Overvoltage Active-High)

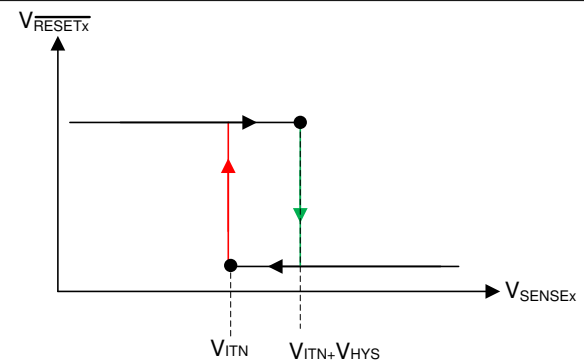


Figure 8-6. Hysteresis (Undervoltage Active-High)

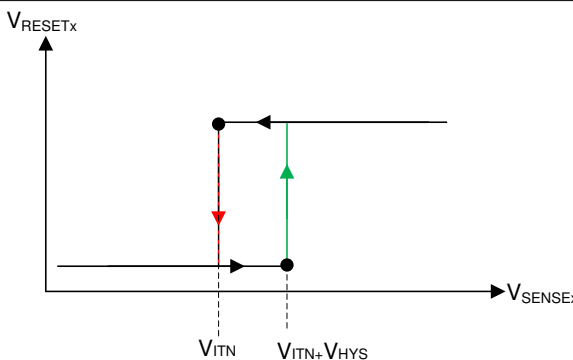


Figure 8-7. Hysteresis (Undervoltage Active-Low)

Table 8-1. Common Hysteresis Lookup Table

| TARGET | | | DEVICE ACTUAL HYSTERESIS OPTION |
|------------------|--------------|---------------------|---------------------------------|
| DETECT THRESHOLD | TOPOLOGY | RELEASE VOLTAGE (V) | |
| 18.0 V | Overvoltage | 17.5 V | -3% |
| 18.0 V | Overvoltage | 16.0 V | -11% |
| 17.0 V | Overvoltage | 16.5 V | -3% |
| 16.0 V | Overvoltage | 15.0 V | -6% |
| 15.0 V | Overvoltage | 14.0 V | -7% |
| 6.0 V | Undervoltage | 6.5 V | 0.5 V |
| 5.5 V | Undervoltage | 6 V | 0.5 V |
| 8 V | Undervoltage | 9 V | 1 V |
| 5 V | Undervoltage | 7.5 V | 2.5 V |

Table 8-1 shows a sample of hysteresis and voltage options for the TPS38-Q1. For threshold voltages ranging from 2.7 V to 8 V, one option is to select a fixed hysteresis value ranging from 0.5 V to 2.5 V in increments of 0.5 V. Additionally, a second option can be selected where the hysteresis value is a percentage of the threshold voltage. The percentage of voltage hysteresis ranges from 2% to 13%.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is $(V_{ITN(UV)} + V_{HYS})$ and for the overvoltage (OV) channel is $(V_{ITP(OV)} - V_{HYS})$. For a visual understanding of the UV and OV release voltage, see Figure 7-2 and Figure 7-3. The accuracy of the release voltage, or stated in the Section 7.5 as *Hysteresis Accuracy* is $\pm 1.5\%$. Expanding what is shown in Table 8-1, below are a few voltage hysteresis examples that include the hysteresis accuracy:

Undervoltage (UV) Channel

$$V_{ITN} = 0.8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 5\% = 40 \text{ mV}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 39.4 \text{ mV or } 40.6 \text{ mV}$$

$$\text{Release Voltage} = V_{ITN} + V_{HYS} = 839.4 \text{ mV to } 840.6 \text{ mV}$$

Overvoltage (OV) Channel

$$V_{ITP} = 8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 2 \text{ V}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 1.97 \text{ V or } 2.03 \text{ V}$$

$$\text{Release Voltage} = V_{ITP} - V_{HYS} = 5.97 \text{ V to } 6.03 \text{ V}$$

8.3.3 Output Logic Configurations

TPS38-Q1 has two channels with separate sense pins and reset pins that can be configured independently of each other. Channel 1 is available as Open-Drain and Push-Pull while channel 2 is only available as Open-Drain topology.

The available output logic configuration combinations are shown in Table [Table 8-2](#).

Table 8-2. TPS38-Q1 Output Logic

| DESCRIPTION | NOMENCLATURE | VALUE | |
|---|--------------|-----------|-----------|
| | | CHANNEL 1 | CHANNEL 2 |
| GPN Topology (OV and UV only) both channels are either OV or UV <ul style="list-style-type: none"> • UV = Undervoltage • OV = Overvoltage • PP = Push-Pull • OD = Open-Drain • L = Active low • H = Active high | TPS38A-Q1 | UV OD L | UV OD L |
| | TPS38B-Q1 | UV PP L | UV OD L |
| | TPS38D-Q1 | UV PP L | UV OD H |
| | TPS38E-Q1 | UV PP H | UV OD H |
| | TPS38F-Q1 | UV PP H | UV OD L |
| | TPS38G-Q1 | UV OD H | UV OD H |
| | TPS38H-Q1 | UV OD H | UV OD L |
| | TPS38J-Q1 | OV OD L | OV OD L |
| | TPS38M-Q1 | OV PP L | OV OD L |
| | TPS38N-Q1 | OV PP L | OV OD H |
| | TPS38O-Q1 | OV PP H | OV OD H |
| | TPS38P-Q1 | OV PP H | OV OD L |

8.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the (I_{lk}) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS38-Q1 open-drain output pin.

8.3.3.2 Push-Pull

Push-Pull output does not require an external resistor since is the output is internally pulled-up to VDD during V_{OH} condition and output will be connected to GND during V_{OH} condition.

8.3.3.3 Active-High (RESET)

RESET (active-high), denoted with no bar above the pin label. RESET remains low (V_{OL} , deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.3.4 Active-Low ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH} , deasserted) (open drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.4 User-Programmable Reset Time Delay

The TPS38-Q1 has an adjustable reset release time delay with external capacitors. Channel timing is independent of each other.

- A capacitor in CTR1 / $\overline{\text{MR}}$ program the reset time delay of Output 1.
- A capacitor in CTR2 / $\overline{\text{MR}}$ program the reset time delay of Output 2.
- No capacitor on these pins gives the fastest reset delay time indicated in the [Section 7.6](#).

8.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR1 pin and GND, CTR2 for channel 2. In this section CTRx represent either channel 1 or channel 2.

The relationship between external capacitor $C_{CTR_EXT} (typ)$ and the time delay $t_{CTR} (typ)$ is given by [Equation 1](#).

$$t_{CTR} (typ) = -\ln (0.28) \times R_{CTR} (typ) \times C_{CTR_EXT} (typ) + t_{CTR} (no\ cap) \quad (1)$$

$R_{CTR} (typ)$ = is in kilo ohms (kOhms)

$C_{CTR_EXT} (typ)$ = is given in microfarads (μF)

$t_{CTR} (typ)$ = is the reset time delay in (ms)

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in [Section 7.5](#), and a constant. The minimum and maximum variance due to the constant is show in [Equation 2](#) and [Equation 3](#):

$$t_{CTR} (min) = -\ln (0.31) \times R_{CTR} (min) \times C_{CTR_EXT} (min) + t_{CTR} (no\ cap) (min) \quad (2)$$

$$t_{CTR} (max) = -\ln (0.25) \times R_{CTR} (max) \times C_{CTR_EXT} (max) + t_{CTR} (no\ cap) (max) \quad (3)$$

The recommended maximum reset delay capacitor for the TPS38-Q1 is limited to 10 μF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

8.3.5 User-Programmable Sense Delay

TPS38-Q1 has adjustable sense release time delay with external capacitors. Channel timing are independent of each other. Sense delay is used as a de-glitcher or ignoring known transients.

- A capacitor in CTS1 program the excursion detection on SENSE1.
- A capacitor in CTS2 program the excursion detection on SENSE2.
- No capacitor on these pins gives the fastest detection time indicated in the [Section 7.6](#).

8.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS1 pin and GND, CTS2 for channel 2. In this section CTSx represent either channel 1 or channel 2.

The relationship between external capacitor C_{CTS_EXT} (typ) and the time delay t_{CTS} (typ) is given by [Equation 4](#).

$$t_{CTS} (typ) = -\ln (0.28) \times R_{CTS} (typ) \times C_{CTS_EXT} (typ) + t_{CTS} (no\ cap) \quad (4)$$

R_{CTS} = is in kilo ohms (kOhms)

C_{CTS_EXT} = is given in microfarads (μF)

t_{CTS} = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in [Section 7.5](#), and a constant. The minimum and maximum variance due to the constant is show in [Equation 5](#) and [Equation 6](#):

$$t_{CTS} (min) = -\ln (0.31) \times R_{CTS} (min) \times C_{CTS_EXT} (min) + t_{CTS} (no\ cap) (min) \quad (5)$$

$$t_{CTS} (max) = -\ln (0.25) \times R_{CTS} (max) \times C_{CTS_EXT} (max) + t_{CTS} (no\ cap) (max) \quad (6)$$

The recommended maximum sense delay capacitor for the TPS38-Q1 is limited to 10 μF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time between fault events to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or time duration between fault events needs to be greater than 10% of the programmed sense time delay.

8.3.6 Manual RESET (CTR1 / $\overline{\text{MR}}$) and (CTR2 / $\overline{\text{MR}}$) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section $\overline{\text{MR}}$ is a generic reference to (CTR1 / $\overline{\text{MR}}$) and (CTR2 / $\overline{\text{MR}}$). A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET1}}$ to assert on reset output. After $\overline{\text{MR}}$ is left floating, $\overline{\text{RESET1}}$ will release the reset if the voltage at SENSE1 pin is at nominal voltage. $\overline{\text{MR}}$ should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the $\overline{\text{MR}}$ cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in Figure 8-8.

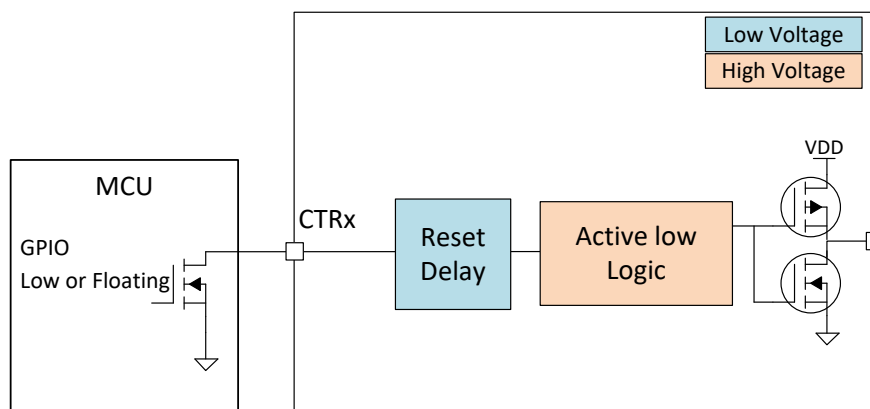


Figure 8-8. Manual Reset Implementation

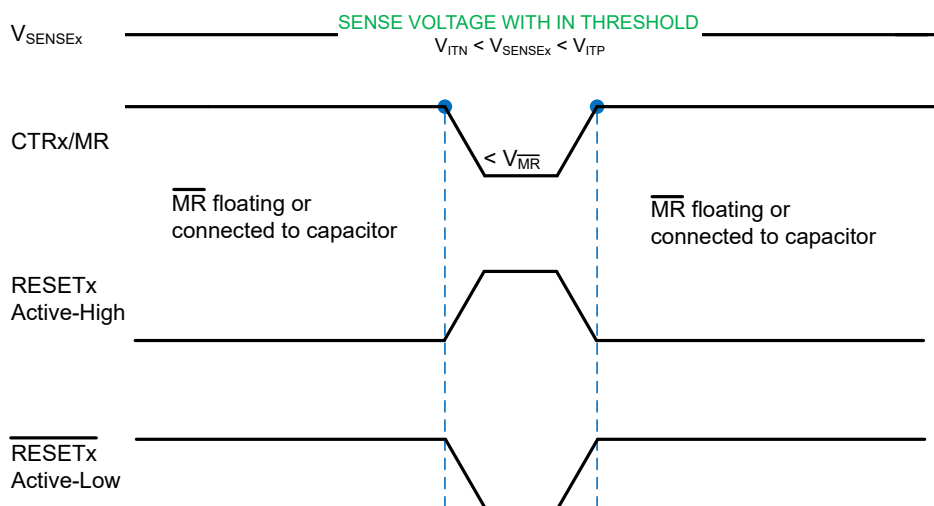


Figure 8-9. Manual Rest Timing Diagram

Table 8-3. $\overline{\text{MR}}$ Functional Table

| $\overline{\text{MR}}$ | SENSE ON NOMINAL VOLTAGE | RESET STATUS |
|------------------------|--------------------------|--|
| Low | Yes | Reset asserted |
| Floating | Yes | Fast reset release when SENSE voltage goes back to nominal voltage |
| Capacitor | Yes | Programmable reset time delay |
| High | Yes | NOT Recommended |

8.3.7 Adjustable Voltage Thresholds

[Equation 7](#) illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored V_{MON} for undervoltage (UV) using channel 1 of the TPS38A010122DSKRQ1 variant. Using [Equation 7](#) and shown in [Figure 8-10](#), R_1 is the top resistor of the resistor divider that is between V_{MON} and V_{SENSE2} , R_2 is the bottom resistor that is between V_{SENSE2} and GND, V_{MON} is the voltage rail that is being monitored and V_{SENSE2} is the input threshold voltage. The monitored UV threshold, denoted as V_{MON-} , where the device will assert a reset signal occurs when $V_{SENSE2} = V_{IT-(UV)}$ or, for this example, $V_{MON-} = 10.8V$ which is 90% from 12 V. Using [Equation 7](#) and assuming $R_2 = 10k\Omega$, R_1 can be calculated shown in [Equation 8](#) where I_{R1} is represented in [Equation 9](#):

$$V_{SENSE2} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

$$R_1 = (V_{MON-} - V_{SENSE2}) \div I_{R1} \quad (8)$$

$$I_{R1} = I_{R2} = V_{SENSE2} \div R_2 \quad (9)$$

Substituting [Equation 9](#) into [Equation 8](#) and solving for R_1 in [Equation 7](#), $R_1 = 125k\Omega$. The TPS38A010122DSKRQ1 is typically meant to monitor a 0.8 V rail with $\pm 2\%$ voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} would need to go above $V_{IT-} + V_{HYS}$. For this example, $V_{MON} = 11.016 V$ when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance R_{SENSE} can be calculated by the SENSE voltage V_{SENSE} divided by the SENSE current I_{SENSE} as shown in [Equation 11](#). V_{SENSE} can be calculated using [Equation 7](#) depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using [Equation 10](#).

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (10)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (11)$$

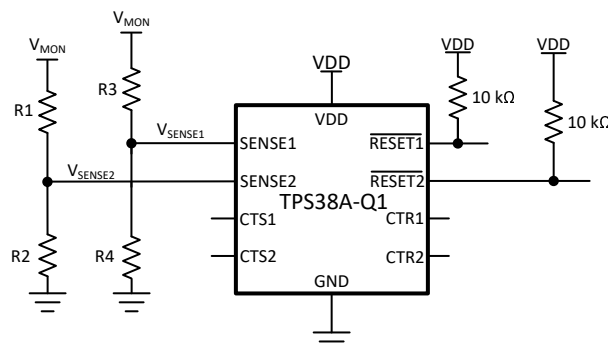


Figure 8-10. Adjustable Voltage Threshold with External Resistor Dividers

8.4 Device Functional Modes

Table 8-4. Undervoltage Detect Functional Mode Truth Table

| DESCRIPTION | SENSE | | CTR ⁽¹⁾ / MR PIN | VDD PIN | OUTPUT ⁽²⁾ (RESET PIN) |
|--|------------------------------|------------------------------------|-----------------------------|---|--------------------------------------|
| | PREVIOUS CONDITION | CURRENT CONDITION | | | |
| Normal Operation | SENSE > V _{ITN(UV)} | SENSE > V _{ITN(UV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | High |
| Undervoltage Detection | SENSE > V _{ITN(UV)} | SENSE < V _{ITN(UV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | Low |
| Undervoltage Detection | SENSE < V _{ITN(UV)} | SENSE > V _{ITN(UV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | Low |
| Normal Operation | SENSE < V _{ITN(UV)} | SENSE > V _{ITN(UV)} + HYS | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | High |
| Manual Reset | SENSE > V _{ITN(UV)} | SENSE > V _{ITN(UV)} | Low | V _{DD} > V _{DD(MIN)} | Low |
| UVLO Engaged | SENSE > V _{ITN(UV)} | SENSE > V _{ITN(UV)} | Open or capacitor connected | V _{POR} < V _{DD} < V _{DD(MIN)} | Low |
| Below V _{POR} , Undefined Output | SENSE > V _{ITN(UV)} | SENSE > V _{ITN(UV)} | Open or capacitor connected | V _{DD} < V _{POR} | Undefined |

(1) Reset time delay is ignored in the truth table

(2) Open-drain active low output. External pull-up resistor to high voltage

Table 8-5. Overvoltage Detect Functional Mode Truth Table

| DESCRIPTION | SENSE | | CTR ⁽¹⁾ / MR PIN | VDD PIN | OUTPUT ⁽²⁾ (RESET PIN) |
|--|------------------------------|------------------------------------|-----------------------------|---|--------------------------------------|
| | PREVIOUS CONDITION | CURRENT CONDITION | | | |
| Normal Operation | SENSE < V _{ITN(OV)} | SENSE < V _{ITN(OV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | High |
| Overvoltage Detection | SENSE < V _{ITN(OV)} | SENSE > V _{ITN(OV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | Low |
| Overvoltage Detection | SENSE > V _{ITN(OV)} | SENSE < V _{ITN(OV)} | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | Low |
| Normal Operation | SENSE > V _{ITN(OV)} | SENSE < V _{ITN(OV)} - HYS | Open or capacitor connected | V _{DD} > V _{DD(MIN)} | High |
| Manual Reset | SENSE < V _{ITN(OV)} | SENSE < V _{ITN(OV)} | Low | V _{DD} > V _{DD(MIN)} | Low |
| UVLO Engaged | SENSE < V _{ITN(OV)} | SENSE < V _{ITN(OV)} | Open or capacitor connected | V _{POR} < V _{DD} < UVLO | Low |
| Below V _{POR} , Undefined Output | SENSE < V _{ITN(OV)} | SENSE < V _{ITN(OV)} | Open or capacitor connected | V _{DD} < V _{POR} | Undefined |

(1) Reset time delay is ignored in the truth table

(2) Open-drain active low output. External pull-up resistor to high voltage

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Adjustable Voltage Thresholds

[Equation 12](#) illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored V_{MON} for undervoltage (UV) using channel 1 of the TPS38A010122DSKRQ1 variant. Using [Equation 12](#) and shown in [Figure 9-1](#), R_1 is the top resistor of the resistor divider that is between V_{MON} and V_{SENSE2} , R_2 is the bottom resistor that is between V_{SENSE2} and GND, V_{MON} is the voltage rail that is being monitored and V_{SENSE2} is the input threshold voltage. The monitored UV threshold, denoted as V_{MON-} , where the device will assert a reset signal occurs when $V_{SENSE2} = V_{IT-(UV)}$ or, for this example, $V_{MON-} = 10.8V$ which is 90% from 12 V. Using [Equation 12](#) and assuming $R_2 = 10k\Omega$, R_1 can be calculated shown in [Equation 13](#) where I_{R1} is represented in [Equation 14](#):

$$V_{SENSE2} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (12)$$

$$R_1 = (V_{MON-} - V_{SENSE2}) \div I_{R1} \quad (13)$$

$$I_{R1} = I_{R2} = V_{SENSE2} \div R_2 \quad (14)$$

Substituting [Equation 14](#) into [Equation 13](#) and solving for R_1 in [Equation 12](#), $R_1 = 125k\Omega$. The TPS38A010122DSKRQ1 is typically meant to monitor a 0.8 V rail with $\pm 2\%$ voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} would need to go above $V_{IT-} + V_{HYS}$. For this example, $V_{MON} = 11.016 V$ when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance R_{SENSE} can be calculated by the SENSE voltage V_{SENSE} divided by the SENSE current I_{SENSE} as shown in [Equation 16](#). V_{SENSE} can be calculated using [Equation 12](#) depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using [Equation 15](#).

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (15)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (16)$$

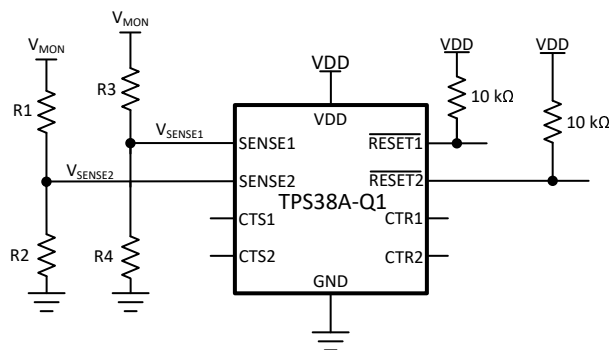


Figure 9-1. Adjustable Voltage Threshold with External Resistor Dividers

9.2 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.3 Typical Application

9.3.1 Design 1: Automotive Off-Battery Monitoring

The initial power stage in automotive applications starts with the 12 V battery. Variation of the battery voltage is common between 9 V and 16 V. Furthermore, if cold-cranking and load dump conditions are considered, voltage transients can occur as low as 3 V and as high as 42 V. In this design example, we are highlighting the ability for low power, direct off-battery voltage supervision. [Figure 9-2](#) illustrates an example of how the TPS38-Q1 is monitoring the battery voltage while being powered by it as well. For more information, read this [application report](#) on how to achieve low I_Q voltage supervision in automotive, wide- V_{IN} applications.

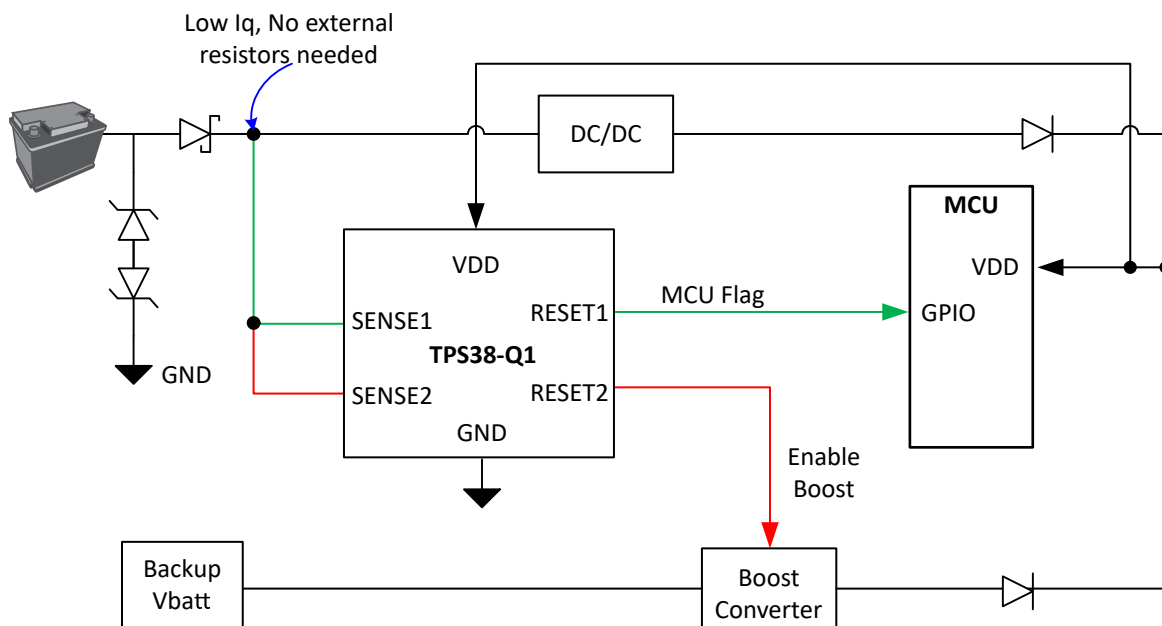


Figure 9-2. Fast Start Supervisor with Direct Off-Battery Monitoring

9.3.1.1 Design Requirements

This design requires voltage supervision on a 12-V power supply voltage rail with possibility of the 12-V rail rising up as high as 42 V. The undervoltage fault occurs when the power supply voltage drops below 7.7 V.

| PARAMETER | DESIGN REQUIREMENT | DESIGN RESULT |
|---|--|--|
| Power Rail Voltage Supervision | Monitor 12 V power supply for undervoltage condition, trigger a undervoltage fault at 7.7 V. | TPS38-Q1 provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations. |
| Maximum Input Power | Operate with power supply input up to 42 V. | The TPS38-Q1 can support a VDD of up to 65 V. |
| Output logic voltage | Open-Drain Output Topology | An open-drain output is recommended to provide the correct reset signal, but a push-pull can also be used. |
| Maximum system current consumption | 2 μ A max when power supply is at 12 V typical | TPS38-Q1 allows for I_Q to remain low with support of up to 65 V. This allows for no external resistor divider to be required. |
| Voltage Monitor Accuracy | Maximum voltage monitor accuracy of 1.5%. | The TPS38-Q1 has 1.5% maximum voltage monitor accuracy. |
| Delay when returning from fault condition | RESET delay of at least 420 ms when returning from a undervoltage fault. | $C_{CTR} = 0.33 \mu$ F sets 422 ms delay |

9.3.1.2 Detailed Design Procedure

The primary advantage of this application is being able to directly monitor a voltage on an automotive battery without needing external resistor dividers on the SENSEx inputs. This keeps the overall I_Q of the design low while still achieving the desired rail monitoring.

As shown in [Figure 9-2](#), rail monitoring is done by connecting SENSE1 and SENSE2 inputs directly to the battery rail after the TVS protection diodes. The TPS38-Q1 that is being used in this example is a fixed voltage variant where SENSE1 and SENSE 2 threshold voltages have been set internally by the factory. Word of caution, the TVS protection diodes must be chosen such that the transient voltages on the monitored rails do not exceed the absolute max limit listed in [Section 7.1](#).

To use this configuration, the specific voltage threshold variation of the device must be chosen according to the application. In this configuration, the '77' variation must be chosen for 7.7 V as shown in [Table 10-1](#).

The device being able to handle 65 V on VDD means the monitored voltage rail can go as high as 42 V for the application transients and not violate the recommended maximum for the supervisor as it usually would. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case. Good design practice recommends using a 0.1 μ F capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.

9.3.1.3 Application Curves

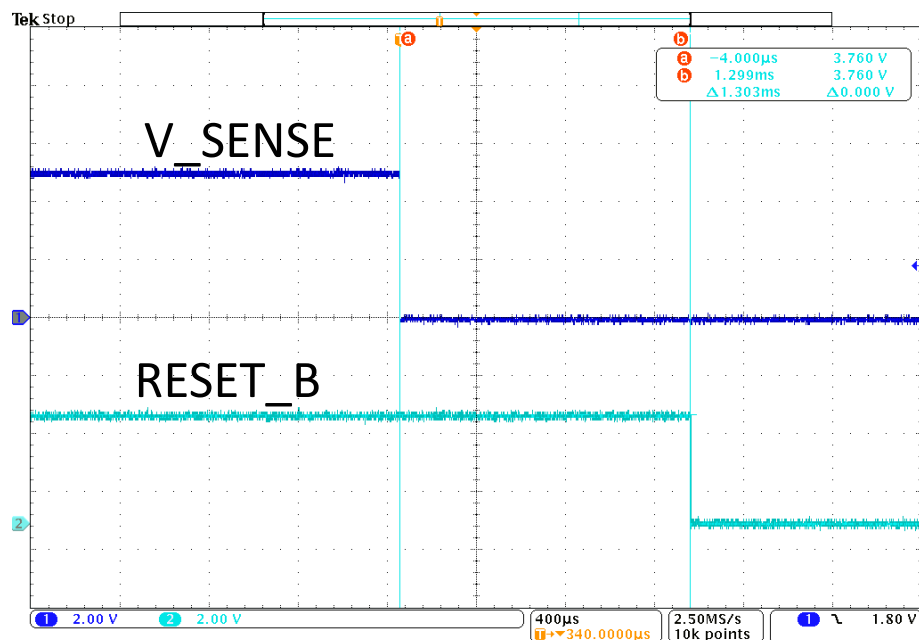


Figure 9-3. Undervoltage Reset Waveform

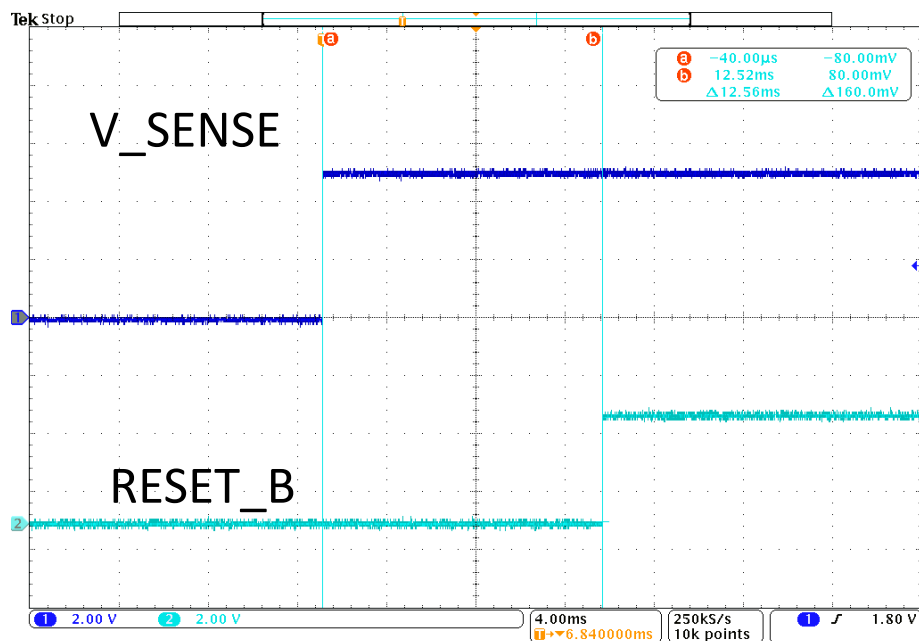


Figure 9-4. Undervoltage Recovery Waveform

9.4 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V (V_{POR}) to 65 V (max operation). Good analog design practice recommends placing a minimum 0.1 μ F ceramic capacitor as near as possible to the VDD pin.

9.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power

dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using [Equation 17](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (17)$$

The actual power being dissipated in the device can be represented by [Equation 18](#):

$$P_D = V_{DD} \times I_{DD} + P_{RESET} \quad (18)$$

P_{RESET} is calculated by [Equation 19](#) or [Equation 20](#)

$$P_{RESET} (PUSH/PULL) = V_{DD} - V_{RESET} \times I_{RESET} \quad (19)$$

$$P_{RESET} (OPEN-DRAIN) = V_{RESET} \times I_{RESET} \quad (20)$$

[Equation 17](#) and [Equation 18](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be de-rated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 21](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (21)$$

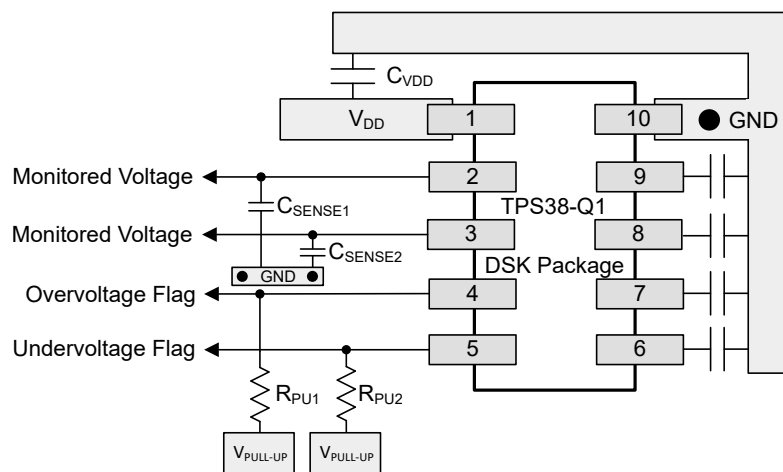
9.5 Layout

9.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 μF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSEx pins, placing a 1 nF to 10 nF capacitor between the SENSEx pins and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS1, CTS2, CTR1, or CTR2, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- For open-drain variants, place the pull-up resistors on $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins as close to the pins as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).
- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

9.5.2 Layout Example

The DSK layout example in [Figure 9-5](#) shows how the TPS38-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.



● Vias used to connect pins for application-specific connections

Figure 9-5. TPS38-Q1 DSK Package Recommended Layout

The DYY layout example in [Figure 9-6](#) shows how the TPS38-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.

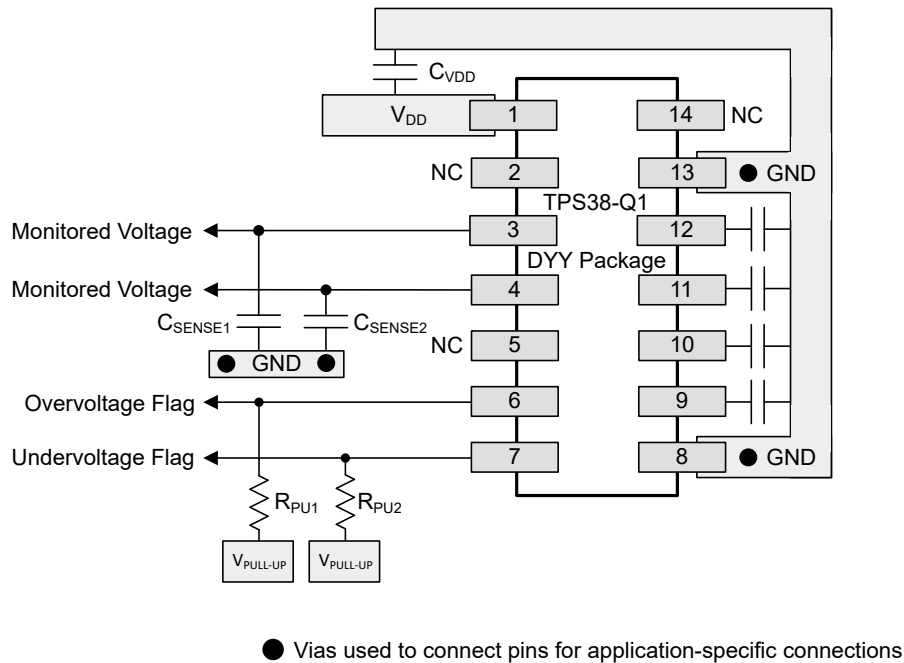


Figure 9-6. TPS38-Q1 DYY Package Recommended Layout

9.5.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in [Figure 9-7](#) the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

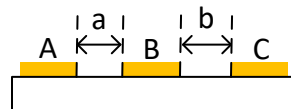


Figure 9-7. Creepage Distance

[Figure 9-7](#) details:

- A = Left pins (high voltage)
- B = Central pad (not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltage)
- Creepage distance = $a + b$

10 Device and Documentation Support

10.1 Device Nomenclature

Section 5 shows how to decode the function of the device based on its part number

Table 10-1 shows TPS38-Q1 possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

Table 10-1. Voltage Options

| 100 mV STEPS | | | | 400 mV STEPS | | 500 mV STEPS | | 1 V STEPS | |
|-------------------|-------------------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|
| NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS |
| 01 | 800 mV (divider bypass) | 70 | 7.0 V | A0 | 10.4 V | D0 | 20.5 V | F0 | 31.0 V |
| 27 | 2.7 V | 71 | 7.1 V | A1 | 10.8 V | D1 | 21.0 V | F1 | 32.0 V |
| 28 | 2.8 V | 72 | 7.2 V | A2 | 11.2 V | D2 | 21.5 V | F2 | 33.0 V |
| 29 | 2.9 V | 73 | 7.3 V | A3 | 11.6 V | D3 | 22.0 V | F3 | 34.0 V |
| 30 | 3.0 V | 74 | 7.4 V | A4 | 12.0 V | D4 | 22.5 V | F4 | 35.0 V |
| 31 | 3.1 V | 75 | 7.5 V | A5 | 12.4 V | D5 | 23.0 V | F5 | 36.0 V |
| 32 | 3.2 V | 76 | 7.6 V | A6 | 12.8 V | D6 | 23.5 V | | |
| 33 | 3.3 V | 77 | 7.7 V | A7 | 13.2 V | D7 | 24.0 V | | |
| 34 | 3.4 V | 78 | 7.8 V | A8 | 13.6 V | D8 | 24.5 V | | |
| 35 | 3.5 V | 79 | 7.9 V | A9 | 14.0 V | D9 | 25.0 V | | |
| 36 | 3.6 V | 80 | 8.0 V | B0 | 14.4 V | E0 | 25.5 V | | |
| 37 | 3.7 V | 81 | 8.1 V | B1 | 14.8 V | E1 | 26.0 V | | |
| 38 | 3.8 V | 82 | 8.2 V | B2 | 15.2 V | E2 | 26.5 V | | |
| 39 | 3.9 V | 83 | 8.3 V | B3 | 15.6 V | E3 | 27.0 V | | |
| 40 | 4.0 V | 84 | 8.4 V | B4 | 16.0 V | E4 | 27.5 V | | |
| 41 | 4.1 V | 85 | 8.5 V | B5 | 16.4 V | E5 | 28.0 V | | |
| 42 | 4.2 V | 86 | 8.6 V | B6 | 16.8 V | E6 | 28.5 V | | |
| 43 | 4.3 V | 87 | 8.7 V | B7 | 17.2 V | E7 | 29.0 V | | |
| 44 | 4.4 V | 88 | 8.8 V | B8 | 17.6 V | E8 | 29.5 V | | |
| 45 | 4.5 V | 89 | 8.9 V | B9 | 18.0 V | E9 | 30.0 V | | |
| 46 | 4.6 V | 90 | 9.0 V | C0 | 18.4 V | | | | |
| 47 | 4.7 V | 91 | 9.1 V | C1 | 18.8 V | | | | |
| 48 | 4.8 V | 92 | 9.2 V | C2 | 19.2 V | | | | |
| 49 | 4.9 V | 93 | 9.3 V | C3 | 19.6 V | | | | |
| 50 | 5.0 V | 94 | 9.4 V | C4 | 20.0 V | | | | |
| 51 | 5.1 V | 95 | 9.5 V | | | | | | |
| 52 | 5.2 V | 96 | 9.6 V | | | | | | |
| 53 | 5.3 V | 97 | 9.7 V | | | | | | |
| 54 | 5.4 V | 98 | 9.8 V | | | | | | |
| 55 | 5.5 V | 99 | 9.9 V | | | | | | |
| 56 | 5.6 V | 00 | 10.0 V | | | | | | |
| 57 | 5.7 V | | | | | | | | |
| 58 | 5.8 V | | | | | | | | |
| 59 | 5.9 V | | | | | | | | |
| 60 | 6.0 V | | | | | | | | |
| 61 | 6.1 V | | | | | | | | |

Table 10-1. Voltage Options (continued)

| 100 mV STEPS | | | | 400 mV STEPS | | 500 mV STEPS | | 1 V STEPS | |
|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|-------------------|--------------------|
| NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS | NOMEN- CLATURE | VOLTAGE OPTIONS |
| 62 | 6.2 V | | | | | | | | |
| 63 | 6.3 V | | | | | | | | |
| 64 | 6.4 V | | | | | | | | |
| 65 | 6.5 V | | | | | | | | |
| 66 | 6.6 V | | | | | | | | |
| 67 | 6.7 V | | | | | | | | |
| 68 | 6.8 V | | | | | | | | |
| 69 | 6.9 V | | | | | | | | |

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------------|---------------|----------------------|---------------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS38A010122DSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KJL |
| TPS38A010122DSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KJL |
| TPS38A0101DDDSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32GL |
| TPS38A0101DDDSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32GL |
| TPS38A5151IIDYYRQ1 | Active | Production | SOT-23-THIN (DYY) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 38A5151IIQ |
| TPS38A5151IIDYYRQ1.A | Active | Production | SOT-23-THIN (DYY) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 38A5151IIQ |
| TPS38A950122DSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32KL |
| TPS38A950122DSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32KL |
| TPS38B4848EEDSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KCL |
| TPS38B4848EEDSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KCL |
| TPS38B5858FFDSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KBL |
| TPS38B5858FFDSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KBL |
| TPS38J010122DSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32IL |
| TPS38J010122DSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 32IL |
| TPS38J010155DSKRQ1 | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KEL |
| TPS38J010155DSKRQ1.A | Active | Production | SON (DSK) 10 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2KEL |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS38-Q1 :

- Catalog : [TPS38](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS38A010122DSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38A0101DDDSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38A5151IIDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TPS38A950122DSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38B4848EEDSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38B5858FFDSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38J010122DSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |
| TPS38J010155DSKRQ1 | SON | DSK | 10 | 3000 | 180.0 | 8.4 | 2.8 | 2.8 | 1.0 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

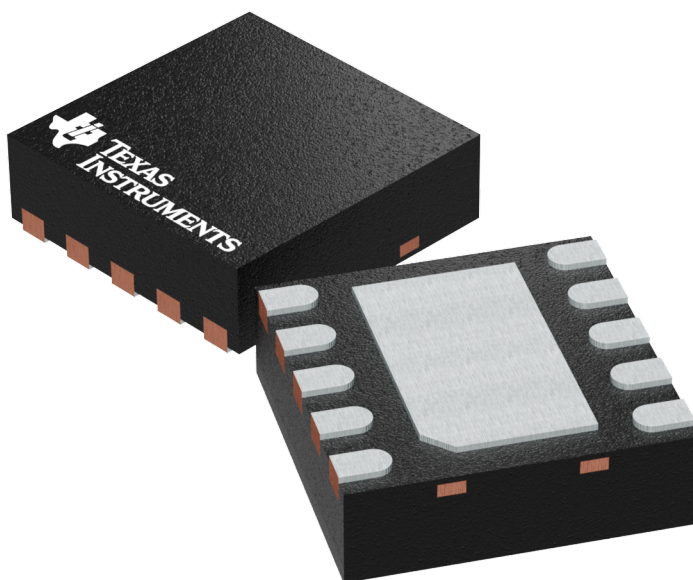
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS38A010122DSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38A0101DDDSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38A5151IIDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| TPS38A950122DSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38B4848EEDSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38B5858FFDSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38J010122DSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS38J010155DSKRQ1 | SON | DSK | 10 | 3000 | 210.0 | 185.0 | 35.0 |

DSK 10

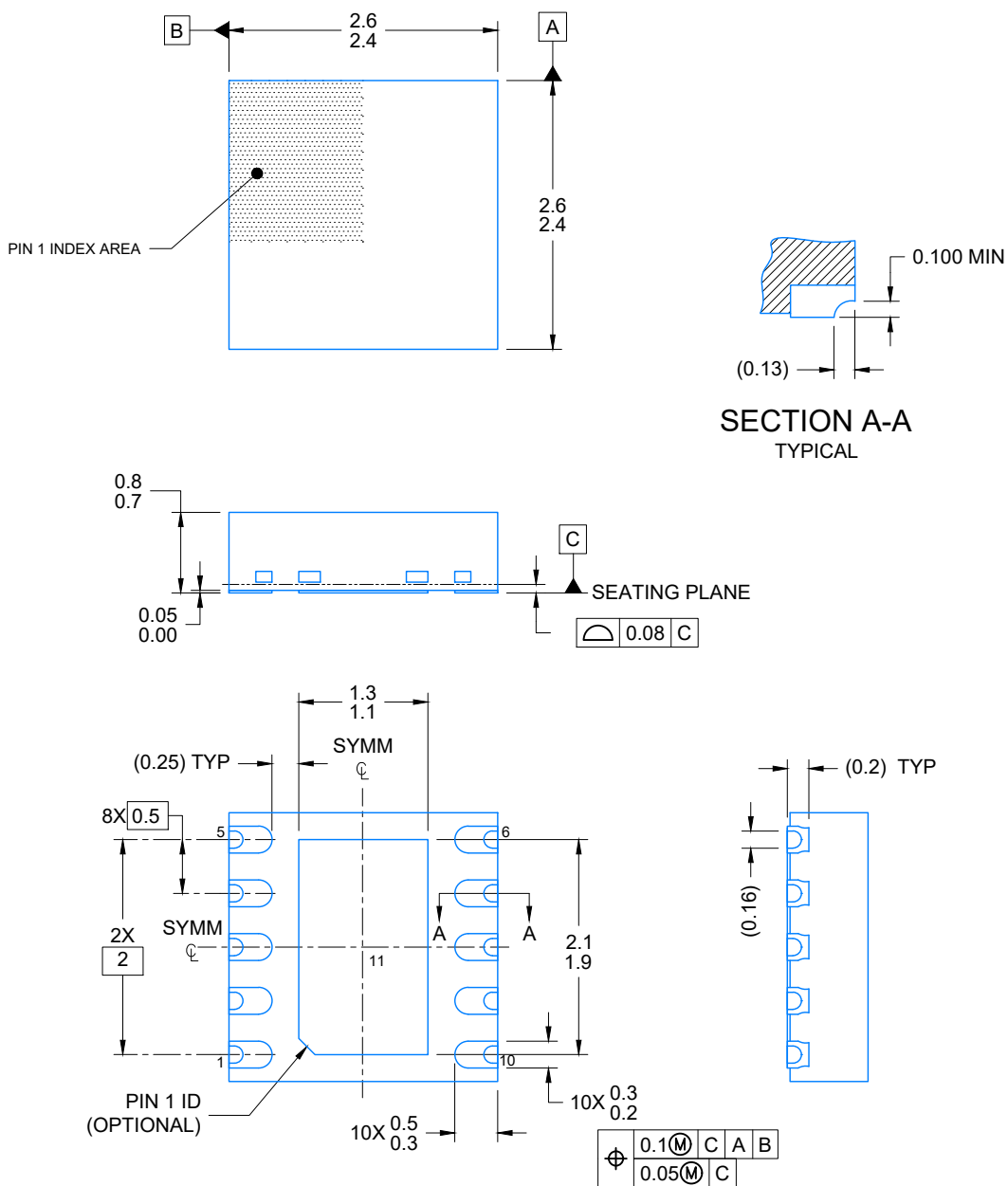
WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



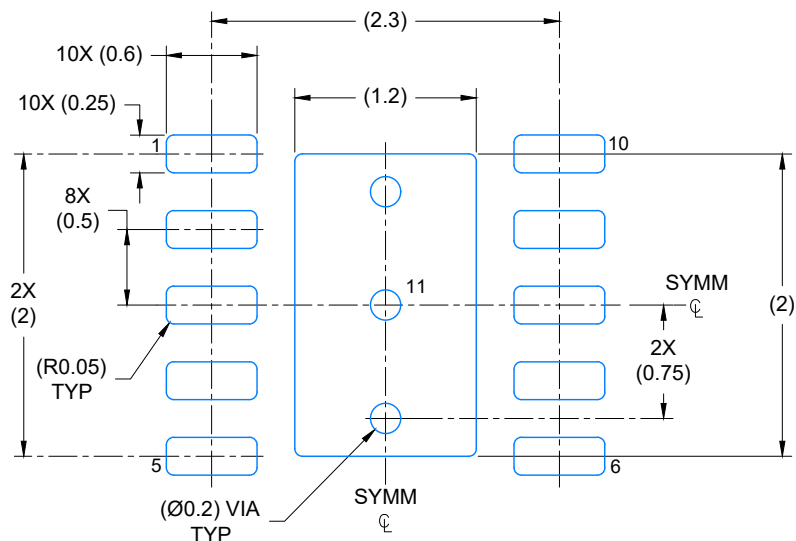
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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NOTES:

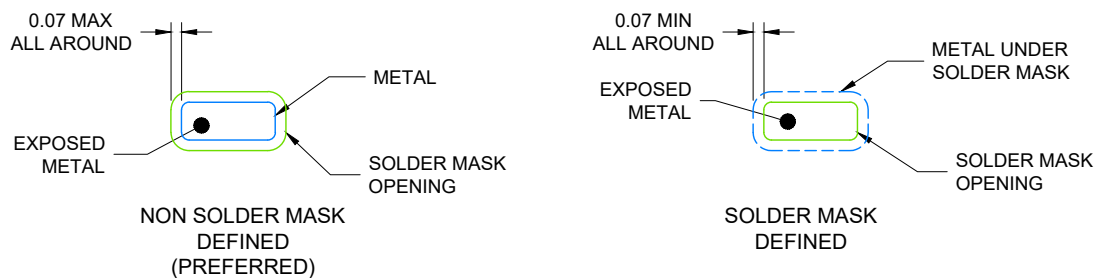
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X

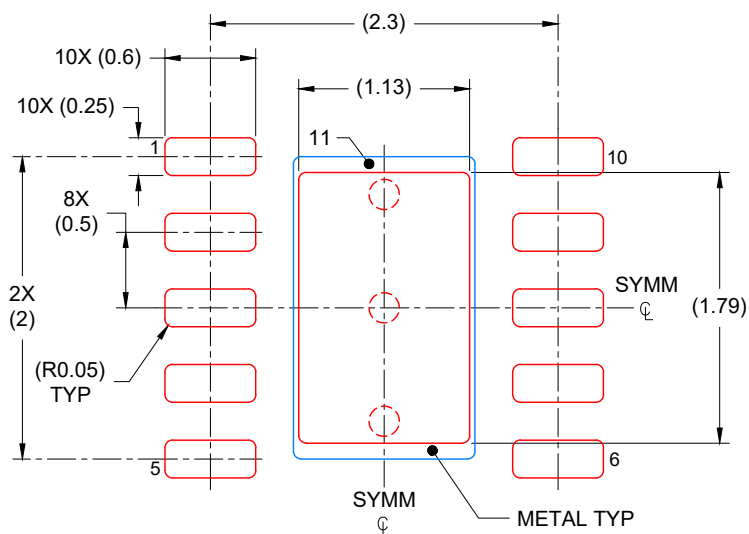


SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



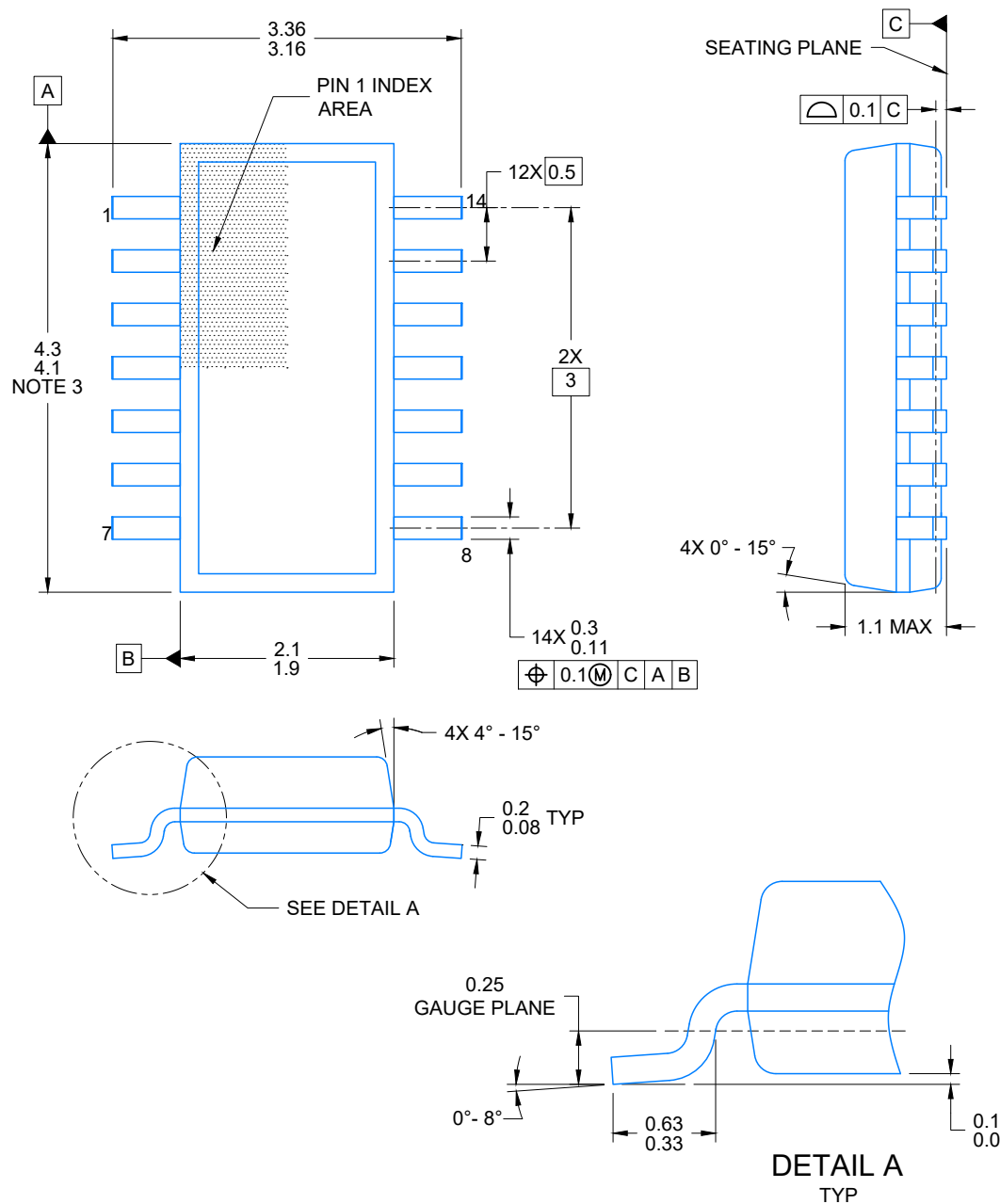
SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 84% PRINTED COVERAGE BY AREA
 SCALE: 20X

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NOTES: (continued)

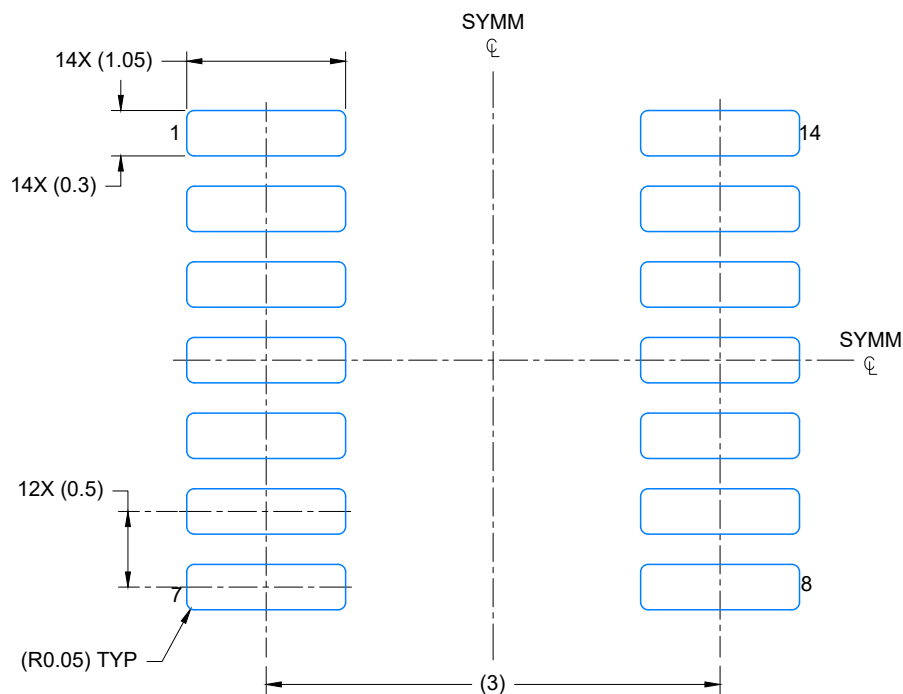
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

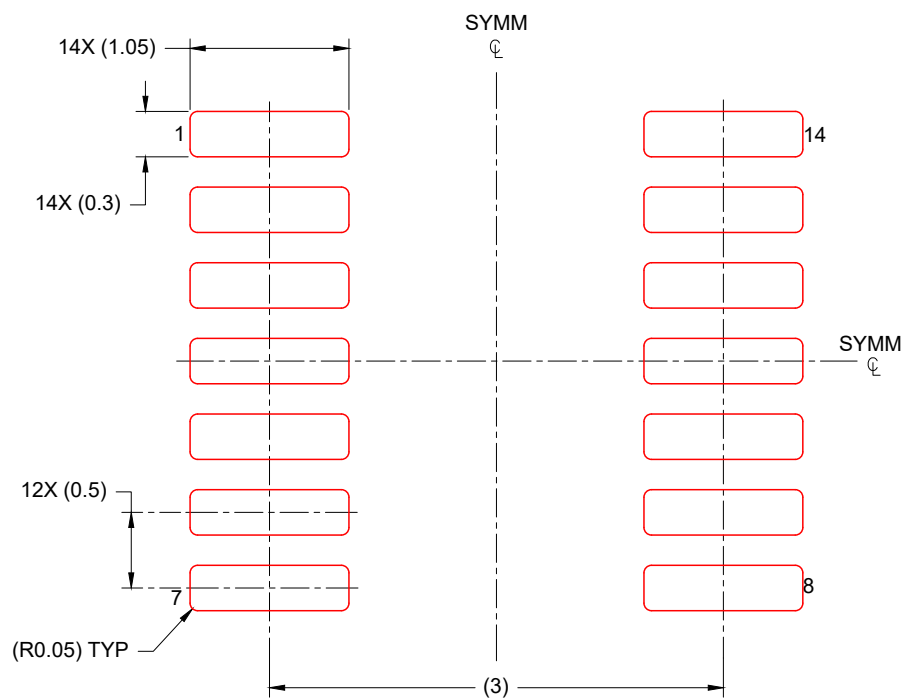


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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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