

TLV803EA29DPW-EVM 4-Pin Voltage Supervisor User Guide

This user's guide describes the TLV803EA29DPW-EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

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1 Introduction

The TLV803EA29DPW-EVM is an evaluation module (EVM) for the TLV803E voltage supervisor also called a Reset IC. The TLV803EA29DPW-EVM can be used with any TLV803ExxxDPW devices variants. The TLV803E has a supply voltage range of 1.7 V to 6 V, and offers connections for all device input and output pins. Test points are provided to give the user access to extra connections if needed for oscilloscope or multimeter measurements.

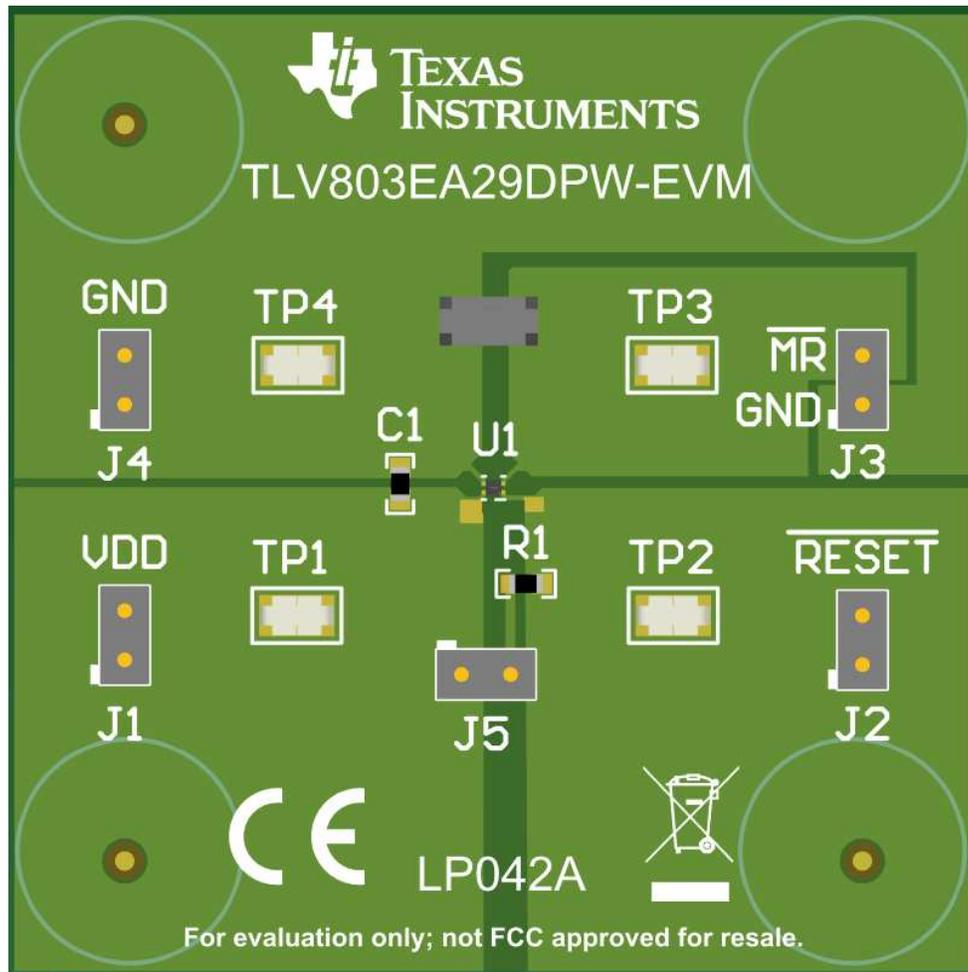


Figure 1. TLV803EA29DPW-EVM Board Top

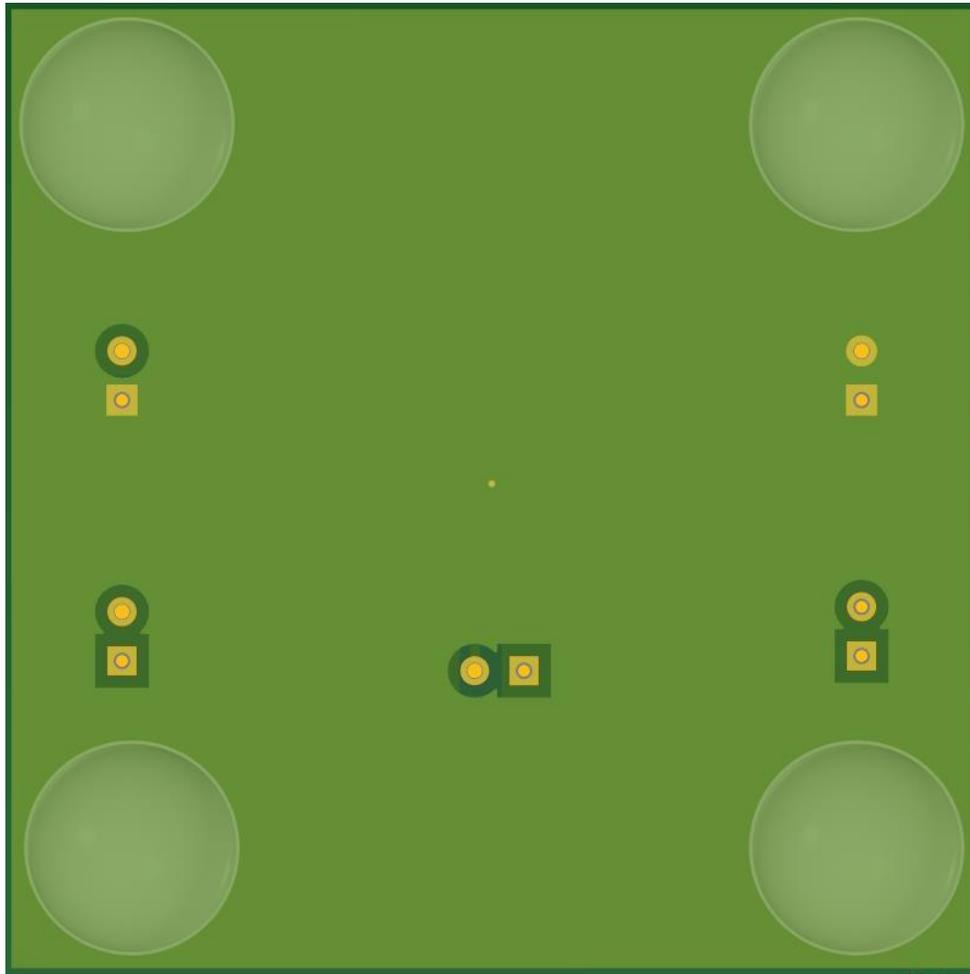


Figure 2. TLV803EA29DPW-EVM Board Bottom

1.1 **Related Documentation**

[TLV803E / TLV809E Datasheet](#)

1.2 **TLV803E Applications**

- Applications using DSPs, microcontrollers, or microprocessors
- Wireless communication systems
- Portable/battery-powered equipment
- Setup boxes and TVs
- Building automation
- Notebook/desktop computers, servers

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV803EA29DPW-EVM schematic, bill of materials (BOM), and layout.

2.1 TLV803EA29DPW-EVM Schematic

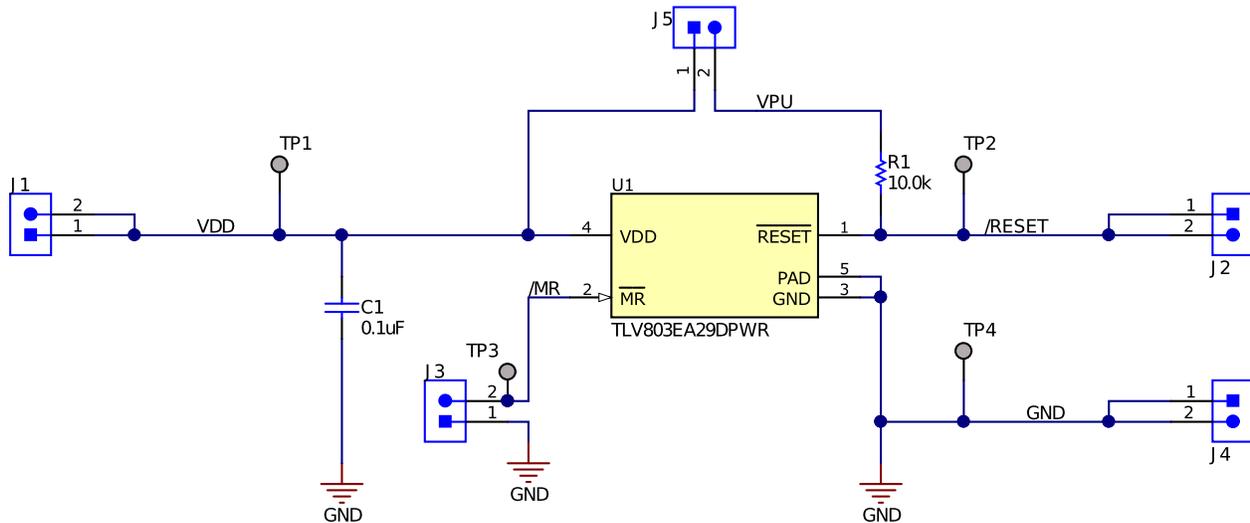


Figure 3. TLV803EA29DPW-EVM Schematic

2.2 TLV803EA29DPW-EVM Bill of Materials

Table 1. EVM BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		LP042	Any
C1	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J5	5		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
R1	1	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
SH-J1	1		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-T-H	Samtec
TP1, TP2, TP3, TP4	4		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Low Power 250-nA IQ and Small Size Supply Voltage Supervisor	X2SON	TLV803EA29DPWR	Texas Instruments

2.3 Layout and Component Placement

Figure 4 shows the top assembly of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 5 and Figure 6 show the top and bottom layouts, Figure 7 and Figure 8 show the top and bottom layers, and Figure 9 shows the top solder mask of the EVM.

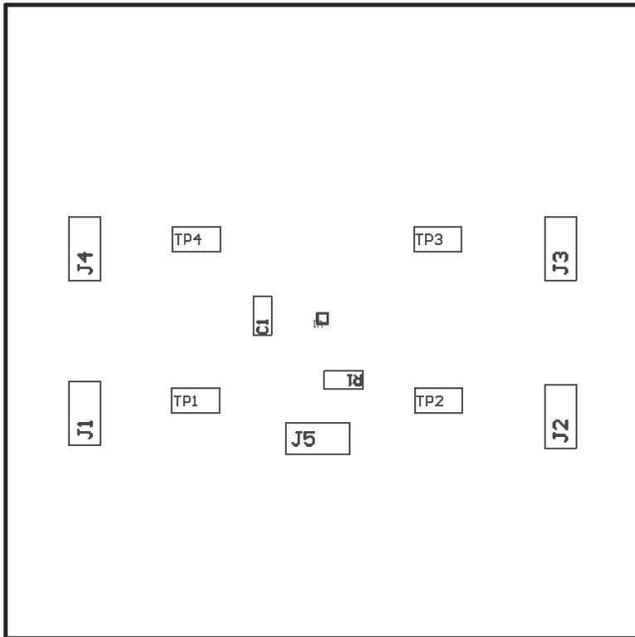


Figure 4. Component Placement—Top Assembly

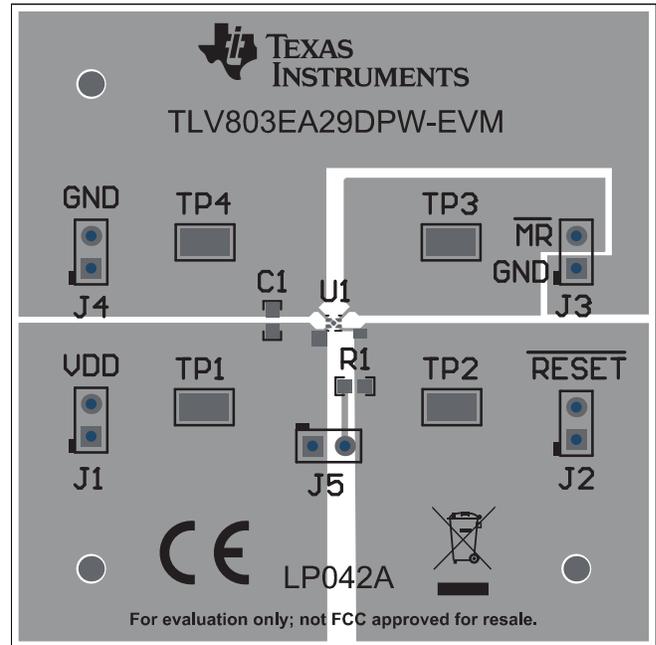


Figure 5. Layout—Top

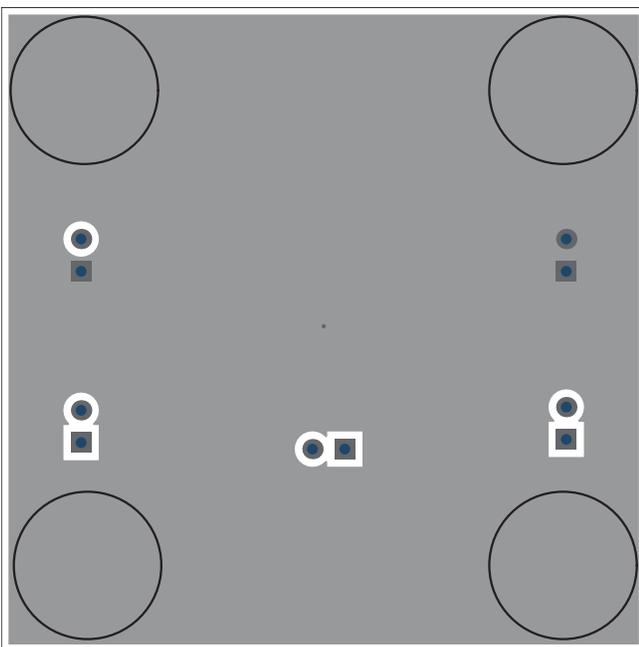


Figure 6. Layout—Bottom

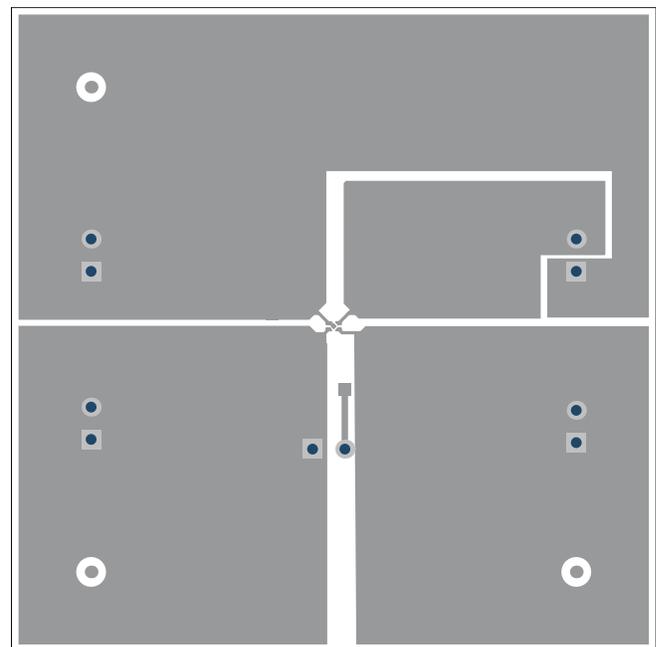


Figure 7. Top Layer

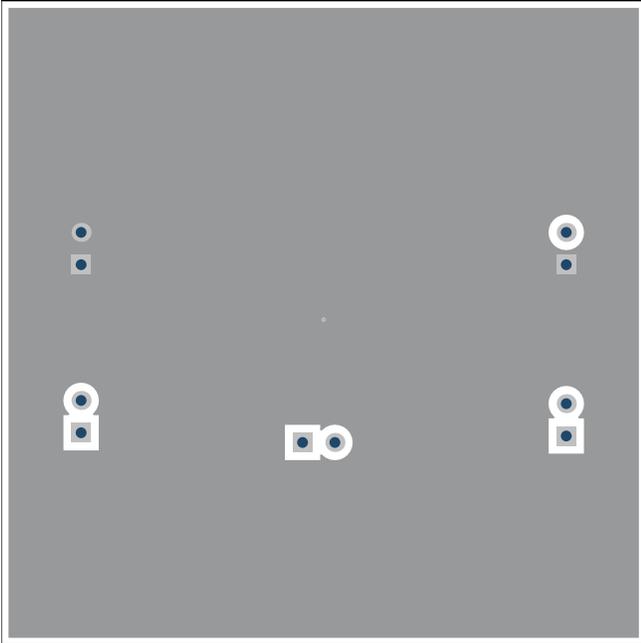


Figure 8. Bottom Layer

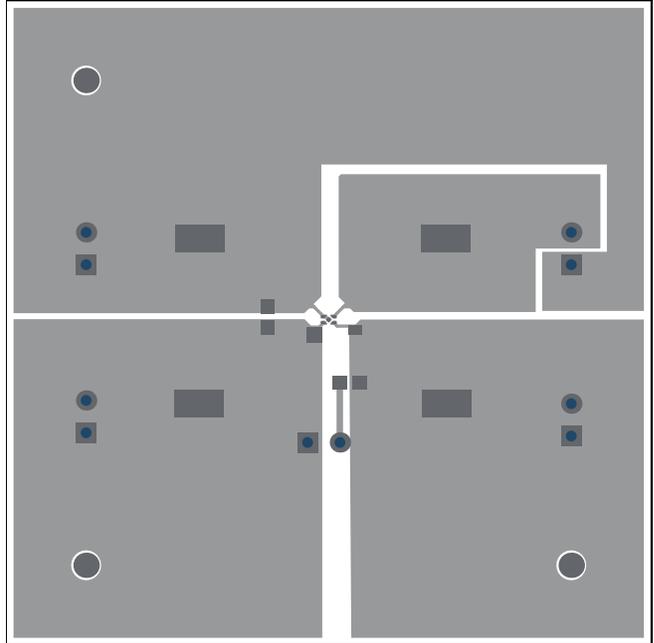


Figure 9. Top Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each EVM has an input power supply connection, and output **RESET** pin, and a ground pin.

3.1 EVM Test Points

[Table 2](#) lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 2. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	V _{DD}	Connection to V _{DD} pin	Allows user to monitor the V _{DD} pin. The V _{DD} pin connects to the input power supply.
TP2	RESET	Connection to RESET pin	Allows user to monitor the RESET pin. This pin changes logic state depending on the voltage on V _{DD} .
TP3	MR	Connection to MR pin	Allows user to connect to the manual reset pin to force a reset condition.
TP4	GND	Connection to GND pin	Allows user to connect to the GND pin.

3.2 EVM Jumpers

[Table 3](#) lists the jumpers on the TLV803EA29DPW-EVM. As ordered, the EVM will have 5 jumpers populated.

Table 3. List of Onboard Jumpers

JUMPER	DEFAULT CONNECTION	DESCRIPTION
J1	Shorted	Both pins on J1 are connected together. Connect one of the pins to the positive (V _{DD}) terminal of the power supply.
J2	Shorted	Both pins on J2 are connected together. Use either pin on jumper J3 to monitor the RESET output pin.
J3	Shorted	Both pins on J3 are connected together. Use either pin on jumper J4 as the ground connection.
J4	Shorted	Both pins on J4 are connected together. Use either pin on jumper J5 as the ground connection.
J5	Closed	Connect a shunt jumper to jumper J5 to use R1 as the pull-up resistor on the RESET output pin.

4 EVM Setup and Operation

This section describes the functionality and operation of the TLV803EA29DPW-EVM. The user must read the [TLV803E / TLV809E Datasheet](#) for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The V_{DD} supply is connected through the J1 header on board. Both pins of jumper J1 are connected together so power can be applied to either pin. Supply voltage is dependent on what the user wants to monitor, but the range is 0.7 V to 6 V. [Table 4](#) details the nominal supply and typical threshold voltage.

Table 4. Nominal Supply and Typical Threshold Voltages

DEVICE	NOMINAL SUPPLY VOLTAGE (V)	TYPICAL THRESHOLD VOLTAGE (V)
TLV803EA29DPWR	3.3	2.9 (+/- 2% MAX)

4.2 Monitoring Voltage on V_{DD}

The TLV803E device monitors voltage via the V_{DD} pin. The EVM provides jumper J1 and test point TP1 for connecting the power supply input to the V_{DD} pin. If the voltage on this pin drops below V_{IT-} , $\overline{\text{RESET}}$ is asserted low. The V_{DD} pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT-} , that corresponds to the chosen device variant. Please see the Device Comparison Table in the [TLV803E / TLV809E Datasheet](#) for more information on the different device variants.

Upon startup, the TLV803E requires V_{DD} to be above V_{POR} before the $\overline{\text{RESET}}$ output is in the correct logic state. [Figure 10](#) shows the propagation time delay high-to-low (t_{PDHL}) when a voltage fault occurs by V_{DD} falling below V_{IT-} to the time $\overline{\text{RESET}}$ transitions active low. [Figure 12](#) shows the reset time delay when the fault condition is removed by V_{DD} rising above V_{IT+} to the time $\overline{\text{RESET}}$ transitions inactive high. The TLV803E has built-in glitch immunity so falling voltage transients on V_{DD} are ignored if the falling pulse duration is less than the glitch immunity timing (t_{GI}). The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the [TLV803E / TLV809E Datasheet](#) for more detailed information.

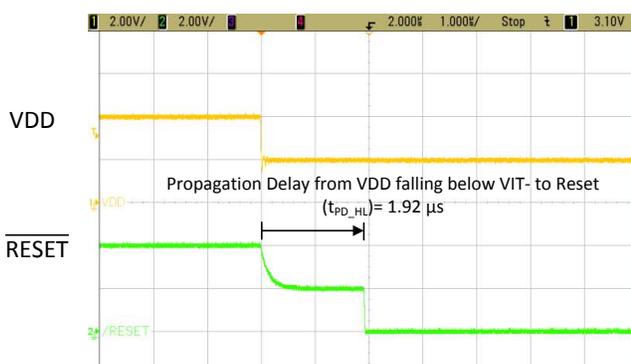


Figure 10. TLV803EA29DPW-EVM Propagation Delay Time High-to-Low (t_{PDHL})

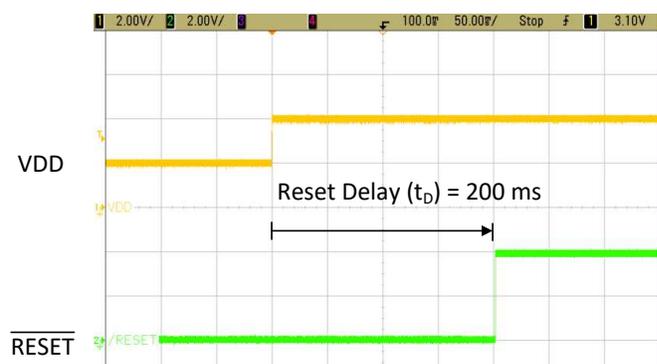


Figure 11. TLV803EA29DPW-EVM Reset Delay Time (t_R)

4.3 Reset Output (\overline{RESET})

The TLV803EA29DPW-EVM comes populated with TLV803EA29DPWR device variant which has open-drain, active-low output topology for the \overline{RESET} pin. The other device variants provide different output topologies and/or different voltage threshold options and can be used on this EVM. Note: if using a TLV809E device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J5 open. The EVM provides a jumper J2 and a test point TP2 connected directly to the \overline{RESET} pin for monitoring and/or interfacing to other devices. The reset signal will be asserted low when the voltage on the V_{DD} pin falls below V_{IT-} . When the voltage on V_{DD} rises higher than the hysteresis voltage above the threshold voltage ($V_{HYS} + V_{IT-}$, or also labeled V_{IT+}), the \overline{RESET} pin is pulled high to the inactive state indicating no fault condition. As Figure 13 shows, when returning from a fault condition, that is when V_{DD} rises above V_{IT+} , V_{DD} must be above V_{IT+} for longer than the reset delay (t_D) otherwise \overline{RESET} will not transition back to logic high inactive state. This is to prevent a premature signaling of no fault condition if V_{DD} briefly comes out of undervoltage condition before faulting again.

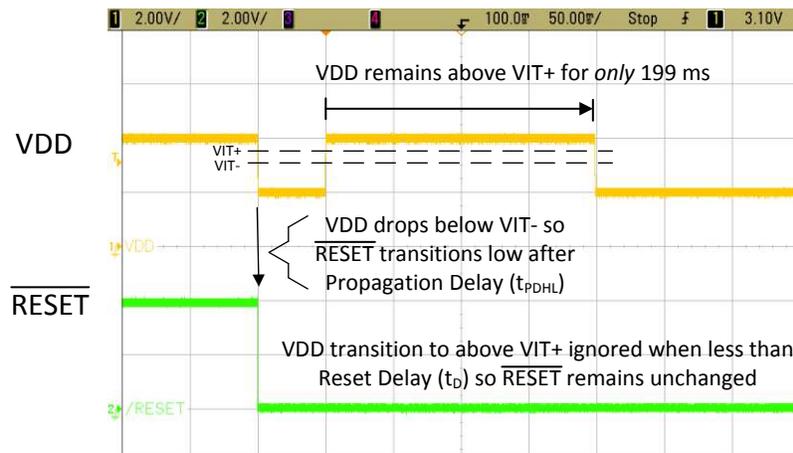


Figure 12. TLV803EA29DPW-EVM Return From Fault Glitch Immunity

4.4 Manual Reset (\overline{MR})

The manual reset (\overline{MR}) pin is a digital input that forces a reset if the input signal is less than 0.4 V and is inactive when above $0.8 \times V_{DD}$. The \overline{MR} pin has an internal 100 k Ω pull-up resistor connected to V_{DD} and can be directly connected to an MCU GPIO, external switch, or left floating if not being used. The device remains in reset condition as long as \overline{MR} is logic low. The \overline{RESET} output returns from reset condition after \overline{MR} remains logic high for the reset time delay (t_D).

Revision History

DATE	REVISION	NOTES
June 2020	*	Initial Release

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